InAs/InP/InSb Nanowires as Low Capacitance n-n Heterojunction Diodes

A. Pitanti,[1,*] D. Ercolani,[1] L. Sorba,[1] S. Roddaro,[1] F. Beltram,[1] L. Nasi,[2] G. Salviati,[2] and A. Tredicucci[1]
[1]*NEST, Scuola Normale Superiore and Istituto Nanoscienze - CNR, piazza San Silvestro 12, 56127 Pisa, Italy*
[2]*IMEM-CNR, Parco Area delle Scienze 37/A, I-43010 Parma, Italy*
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Nanowire diodes have been realized by employing an axial heterojunction between InAs and InSb semiconductor materials. The broken-gap band alignment (type III) leads to a strong rectification effect when the current-voltage (I-V) characteristic is inspected at room temperature. The additional insertion of a narrow InP barrier reduces the thermionic contribution, which results in a net decrease of leakage current in the reverse bias with a corresponding enhanced rectification in terms of asymmetry in the I-V characteristics. The investigated diodes compare favorably with the ones realized with *p*-*n* heterostructured nanowires, making InAs/InP/InSb devices appealing candidates to be used as building blocks for nanowire-based ultrafast electronics and for the realization of photodetectors in the THz spectral range.

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Since the first interesting results on the implementation of complex electronic devices with crossed semiconductor nanowires [1], great efforts have been devoted to the realization of heterojunctions within a single nanowire [2–8]. Such elements are crucial in the development of miniaturized, nanowire-based, ultrafast electronics and for the improvement of the performance of several photonic devices. The simplest operation of a heterojunction exploits its ability to rectify an electric signal applied over it, acting as an electrical diode. If the junction is realized along the nanowire axis, an extremely low device capacitance is expected due to the wire's nanometric cross section: this results in a greatly improved cutoff frequency and, consequently, a net increase in the diode operation speed. This aspect represents a key point for the realization of ultrafast electrical components; moreover, such nanostructures could be implemented in photonic devices, such as detectors, in which the electronic operation frequency can follow that of the incident electromagnetic radiation. Indeed, while some solutions to create a homojunction within a nanowire exist, such as modulation doping of group IV [2–4] (Si or Ge) or III-V [5] (GaN) semiconductors, heterostructured nanowire diodes were mainly realized with radial core-shell structures [6,7] or by employing the vertical alignment with a semiconductor substrate [9]. Clearly, while extremely interesting, most of these solutions do not allow one to exploit the low capacitance associated with the nanowire's small cross section. Very recently the growth of an axial InAs/GaSb heterojunction within a single nanowire has been reported [8]. Unfortunately, in that case, the properties of the GaSb nanowire segment growth were influenced by the presence of In in the chamber, thus making it necessary to resort to the introduction of a 25 nm GaInAs insert layer placed in between the InAs and GaSb materials. This makes the heterointerface region very broad, with a smooth band alignment profile all along the GaInAs insert layer.

In this paper, we instead make use of a two-material sharp axial heterojunction within a single wire, achieved by faceting two *n*-type materials, namely, InAs and InSb, whose band lineup is of type-III (broken gap—see, for example, [10]). It is interesting to note that, while InAs/InSb bulk heterostructures are difficult to grow due to the large lattice constant mismatch ($\sim 6\%$), the feasibility of heterostructured nanowires, indeed, has been demonstrated in the last few years [11–14]. Only the precursor of the group V element has to be switched during growth, with the possibility of growing very long nanowires without the need of any insertion layer and, when InSb is grown on an underlying InAs segment, of obtaining a sharp interface between the two materials. Moreover, the majority carriers are the same in both semiconductors (*n*-type) [15], granting good Ohmic contacts of two-terminal devices in a single lithographic step. This property is also appealing for high-speed operations as minority carriers are not expected to contribute significantly to charge transport, thus issues related to slow recombination times can be avoided. We show that the current-voltage (I-V) curves of such a device display good rectification behavior at room temperature, which is a key aspect toward the realization of nanowire-based diodes. Most important, since no insert layer is needed, we can put a third large-gap material, such as InP, in between the junction, in order to tune the diode behavior (both in terms of conductance and leakage current) as a function of inserted InP barrier thickness. This result is particularly interesting for the implementation of zero bias, rectifying diode detectors which could operate at speed up to the THz spectral range [16]. With a scheme similar to the one adopted successfully in InAs/AlSb/GaSb

*alessandro.pitanti@sns.it

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bulk diodes [17], a higher cutoff frequency is, in fact, expected due to the smaller junction capacitance.

The nanowires were grown on InAs (111)B substrates by the chemical beam epitaxy in a Riber Compact-21 system using Au catalyst nanoparticles. The system employs pressure control of the metal-organic (MO) precursors in the lines to vary their fluxes on the sample during its growth [18]. The MO precursors used are trimethylindium (TMIn), tertiarybutylarsine (TBAs), tertiarybutylphosphine (TBP), and tris(dimethylamino) antimony (TDMASb). While TMIn and TDMASb decompose directly at the sample surface, making elemental In and Sb available for growth, TBAs and TBP were precracked in the injector at 1000° C due to their high decomposition temperature.

A 0.5 nm thick, Au film was first deposited by thermal evaporation on the InAs wafer in a separate evaporator chamber and then transferred to the chemical beam epitaxy system. The wafer was then annealed at 520° C under TBAs flux in order to remove the surface oxide and generate Au nanoparticles by the thermal dewetting of the Au film.

The InAs segment was grown for 75 min at a temperature of (435 ± 10)°C, with MO line pressures of 0.3 and 1.0 Torr for TMIn and TBAs, respectively. Whenever inserted, the thin InP layer was grown at the same temperature, switching the V-group precursor from TBAs to 1 Torr of TBP for 30 or 15 sec, for thick or thin InP layers, respectively, followed by 120 min of InSb growth with 0.45 Torr of TMIn and 0.75 Torr of TDMASb. The optimal growth temperature for InSb is about 20° C lower than InAs and InP and it was ramped down with no interruption during the first 5 min of InSb growth. The growth was terminated by switching off all precursors and rapidly cooling down the sample to room temperature [18].

The samples were first morphologically characterized by scanning electron microscopy (SEM, see Fig. 1(a)]. Then, the presence of InP and, more generally, the structural characteristics of the nanowires were analyzed in depth. To this end, nanowires were deposited on a carbon-coated copper grid and investigated by high-resolution transmission electron microscopy (HRTEM), high-angle annular dark-field (HAADF) and energy-dispersive x-ray spectroscopy by using a JEOL 2200FS microscope working at 200 keV. Figure 1 reports the main results.

In particular, the HRTEM image of a nanowire in the [2-1-10]WZ || [110]ZB zone axis shows the InP barrier layer inserted between the lower InAs and upper InSb segments. We have found that InAs grows with the wurtzite (WZ) phase, while InSb and InP crystallographic structures belong to the zincblende (ZB) phase, as confirmed by the fast Fourier transform of the InP/InSb interface and InAs segment and reported in Fig. 1(c)–1(e). The crystallographic relationships [110]InSb, InP || [2-1-10]InAs, ⟨111⟩InSb, InP || ⟨0001⟩InAs were found. The presence of the InP layer is confirmed by both chemical and structural analyses and highlighted in the HAADF measurements of Fig. 1(f). The thickness of the InP layer, calculated by HRTEM images, the energy-dispersive x-ray spectroscopy analysis, and HAADF chemical profile, is about 5.5 ± 0.5 nm (2.5 nm) for thick-barrier (thin-barrier) wires.

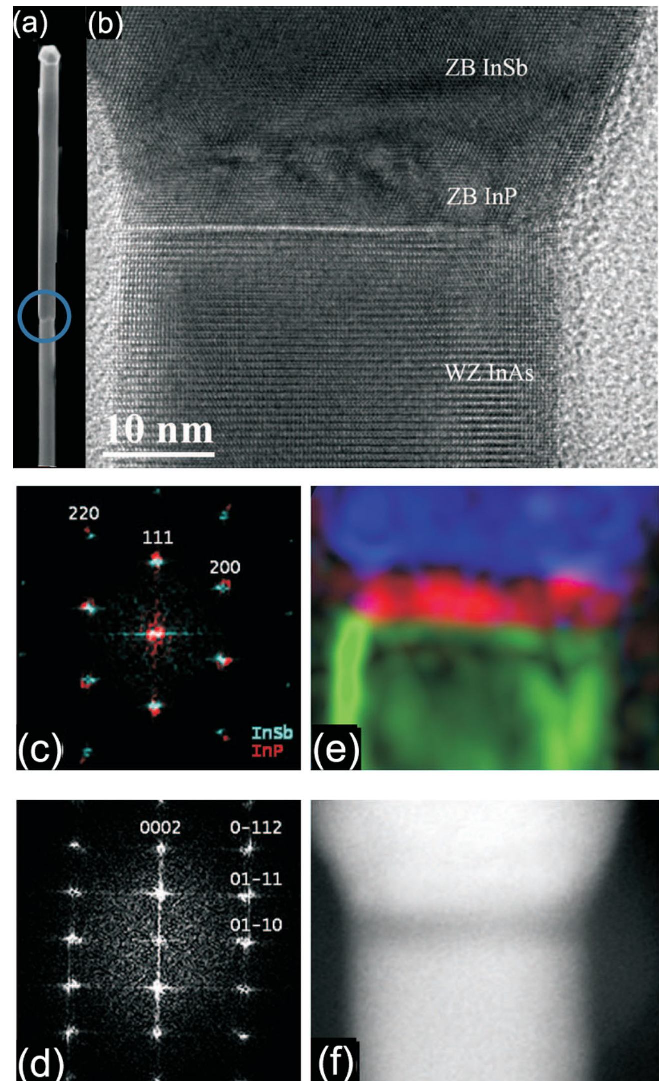

FIG. 1. (a) Scanning electron microscope image of heterostructured nanowires. The junction region is highlighted by the circle. (b): HRTEM image of a NW in the [2-1-10]WZ || [110]ZB zone axis. (c): Fast Fourier transform (FFT) of the interface between InSb and InP, which crystallize in the ZB structure. Two sets of diffraction spots can be distinguished, corresponding to InSb (cyan spots) and InP (red spots) in the [110] ZB zone axis. (d): FFT of the lower NW section showing the [2-1-10] WZ zone axis of InAs. (e): Inverse FFT color map of the region in (a), generated by selecting the different diffraction spots of the InSb ZB (blue), InP ZB (red), and InAs WZ (green) phases. (f): HAADF image taken in the same region as (a).

The devices were realized on a 500 nm SiO_2 buffer layer deposited on a *n*-type doped Si substrate, which acts as a back gate. After the definition of large contacts by optical

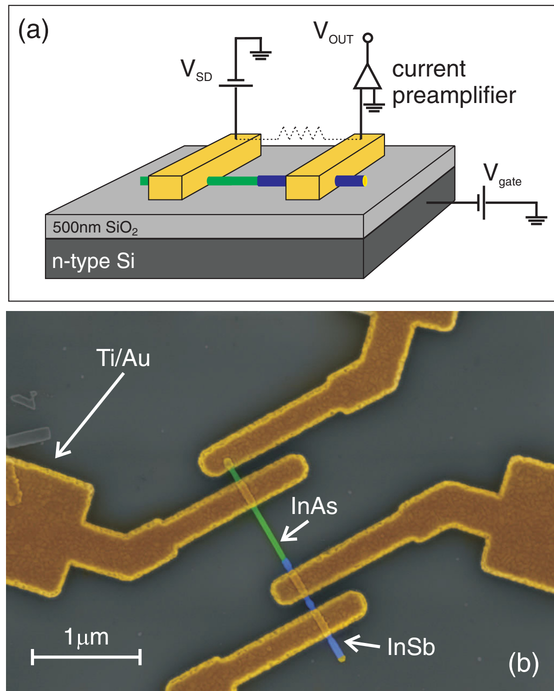

FIG. 2. (a): Schematic of the nanowire device and sketch of the experimental circuit realized to probe the device transport properties. (b): SEM image of a contacted nanowire. The colors are artificially added to enhance the picture clarity. Note that both the InAs/InSb junction and the gold catalyst are clearly recognizable.

lithography, the nanowires are mechanically transferred onto these samples and properly contacted by means of electron-beam lithography. A schematic of a two-terminal device is shown in Fig. 2(a) together with a sketch of the equivalent circuit used for electrical transport characterization.

Prior to Ti/Au(10/130 nm) evaporation, the nanowires were passivated with a $(NH_4)_2S_x$ diluted solution in order to improve the contact quality at the semiconductor/metal interface [19]. Usually the nanowires are long enough to get four contacts on the same device. This allows us to check separately the charge transport characteristics of both InAs and InSb segments and heterojunction. The distance between the two contacts is about 200 nm for the single-material segments, while it ranges from 500 nm to 1 μm for the junction.

A SEM image of a typical contacted device is shown in Fig. 2(b). The InAs/InSb junction can be easily recognized as the region where the nanowire size is increased, from about 50 nm (InAs) to 80 nm (InSb), respectively.

Before evaluating the junction-induced rectification, at first charge, the transport in single-material segments has been investigated; the main results of a typical measured nanowire are summarized in Fig. 3.

Panels (a) and (b) of Fig. 3 report the room-temperature I-V characteristics obtained by sweeping the source-drain voltage bias (V_{SD}) at zero gate voltage. The curves are in

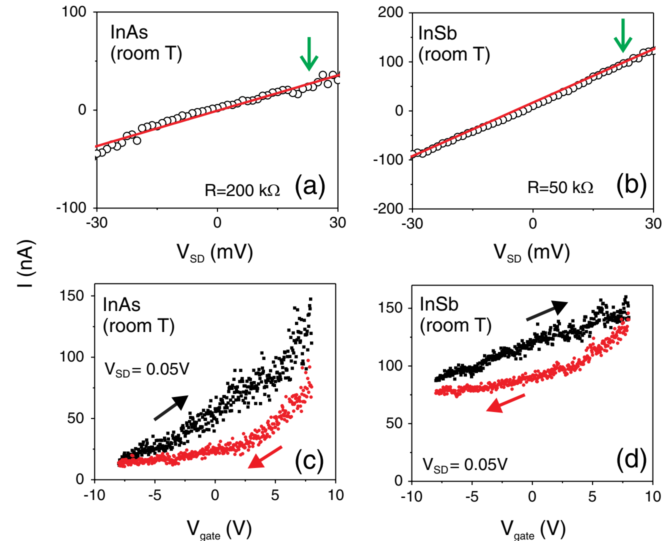

FIG. 3. (a)–(b): I-V characteristics of InAs and InSb segments at room temperature. (c)–(d): Gate sweep and hysteresis cycle for the same segments with a constant source-drain bias of 50 mV at room temperature. The hysteresis of the curves can be attributed to screening effects of surface-trapped charges [28].

good approximation Ohmic, showing a total resistance of about 200 kΩ for the InAs wire and 50 kΩ for the InSb one. Despite the fact that no external doping has been used, a majority of n-type carriers are present in both semiconductor materials, as recently reported in the literature [20]. To prove this assertion, Fig. 3(c) reports the current measured at fixed V_{SD} as a function of the gate bias for the InAs segment. Charges are injected/depleted at a positive/negative bias, confirming that electrons are majority carriers. From the results of Fig. 3(c) and, modeling the nanowire as a simple transistor [21], an electron concentration of 3×10^{17} cm^{-3} is obtained. Note that the intrinsic carrier concentration at room temperature [22] in bulk InAs is about 8×10^{14} cm^{-3}, compared to with respect to the electron concentration evaluated with the transistor model. Somewhat more complicated is the behavior of InSb segments, for which a typical gate sweep is reported in Fig. 3(d). Even if the material can be clearly recognized as n-type by the slope of the experimental curves, the source-drain current saturates at larger V_{gate} with respect to the InAs one. This is probably due to the smaller InSb band gap (195 meV) with respect to the InAs material (435 meV), which may result in the contribution of intrinsic carriers to the observed transport. 'Charge transport at cryogenic temperatures, to which the sample is cooled by dipping it in a liquid He bath, reveals a more complicated behavior (data not shown).

Indeed, the gate-voltage sweeps in all InAs wires show a net pinch-off at negative gate voltages, confirming the n-type nature of the nanowires. The same measurements in the InSb produce different results for different nanowires and applied V_{SD}, often presenting an ambipolar character.

The hole involvement in transport phenomena was indeed already observed in top-gated InSb nanowire transistors and attributed to interband tunneling effects [20]. Here we note also the possible formation of a *p*-type region at the heterointerface, whose tail could extend to influence the transport characteristic of the single InSb segment (we provide more on this later).

As reported in Fig. 4(a), our heterostructured nanowires show a clear room-temperature current-rectification effect. This is indeed expected, since in bulk InAs/InSb heterojunctions a broken-gap band alignment is realized [23]. In fact, though surprising, it is indeed possible to get strong transport asymmetry through *n*-*n* junctions when the proper band lineup is formed [24]. The band gap alignment, while not necessary, ensures that a strong charge-induced band bending, which, in our case, is of the order of the InSb gap, takes place, resulting in a relevant depletion region compensated by a charge accumulation on the other side of the interface. A triangular barrier is formed, which leads to the transport asymmetry, since, for one bias sign, the junction electric field increases, widening the depletion region and hindering transport, while the contrary occurs for the opposite bias sign. This is analogous to the known behavior of the Schottky barrier at a metal semiconductor interface. This kind of heterojunction (a broken gap in *n*-*n* materials) was studied some years ago in bulk systems with extremely good results in terms of electrical rectification [24]. While in our structure, strain effects and surface states can play an important role modifying the band alignment and, therefore, the transport through the heterojunction [25], a simpler, qualitative picture can be useful to understand the physical phenomena which lead to the observed rectification effect. To this end, we have performed simulations of one-dimensional heterojunctions employing a Schrödinger/Poisson equation solver [26], where most semiempirical parameters of the bulk system have been used [23]. The carrier concentration of InAs wires has been extracted from transport measurements in single-material segments, as shown in Fig. 3. Despite InSb being a *n*-type material, it is difficult to evaluate the exact chemical potential energy from our experimental data and thus, the exact triangular barrier shape formed in proximity of the heterojunction. Owing to this fact, simulations have been performed by choosing a range of reasonable carrier concentrations for the InSb. It is important to stress that the qualitative results are the same for each considered InSb carrier concentration. In fact, as reported in the room-temperature, zero-bias simulations in Fig. 4(b), triangular barriers with different widths in the conduction band appear in each case. Interestingly, a short region where holes are the majority carriers appear, realizing an effective *n*-*p*-*n* junction, as qualitatively reported for a chosen InSb donor concentration in Fig. 4(c). Note that the tail of the hole distribution can extend to several hundreds of nanometers, possibly influencing the transport properties of single InSb segments such as the one observed in Fig. 3(b) and 3(d). As discussed below, this does not seem to visibly affect the transport across the junction.

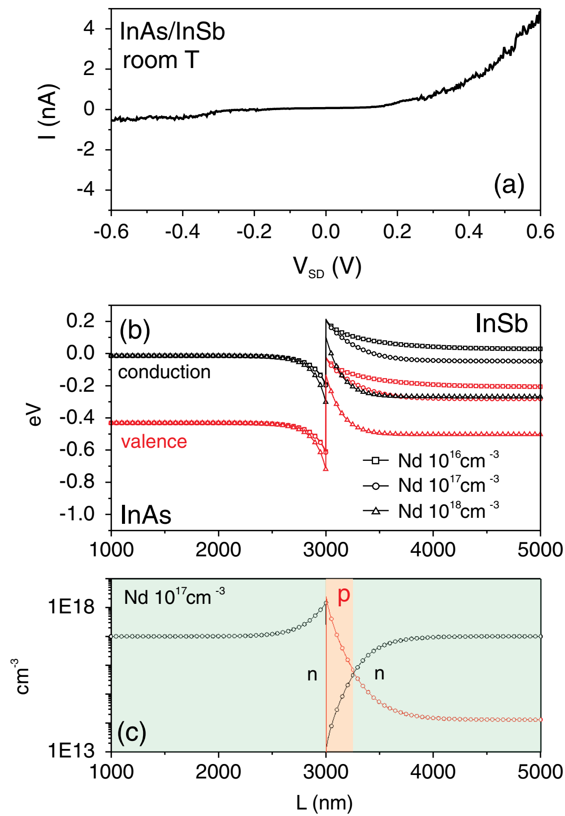

FIG. 4. (a): Rectification through an InAs/InSb junction at room temperature. (b): 1D band alignment (Schrödinger/Poisson) for the InAs/InSb bulk material junction with donor concentration determined from experiment (InAs) and chosen in a reasonable range (InSb). (c): Charge distribution for an InSb donor concentration of 10^{17} cm^{-3}. Note that a *p*-type region is formed on the InSb side close to the junction, forming a *n*-*p*-*n* alignment. Similar charge distributions are obtained for the other possible doping concentrations.

As in the Schottky devices, the transport in the diode is governed by majority carriers and, at low bias, is mostly dominated by thermionic emission; it is thus is strongly hampered at low temperatures. In fact, as can be seen in Fig. 5(a), a negligible leakage current is observed at 4 K. Note that to improve the visibility in the log scale, the data have been positively shifted by 0.5 nA, in such a way that the breakdown threshold is represented by a downward spike. Since the carrier concentration available for transport is reduced at a low temperature due to freeze-out effects, the back gate bias has here a strong effect, given by both an increase of direct conductance and a decrease of the breakdown voltage at positive voltages. This can be seen in Fig. 5(b), where a map of the measured current in the V_{SD}, V_{gate} parameter space is depicted. These data also confirm that diode transport is dominated by majority electrons. The breakdown voltage is highlighted here

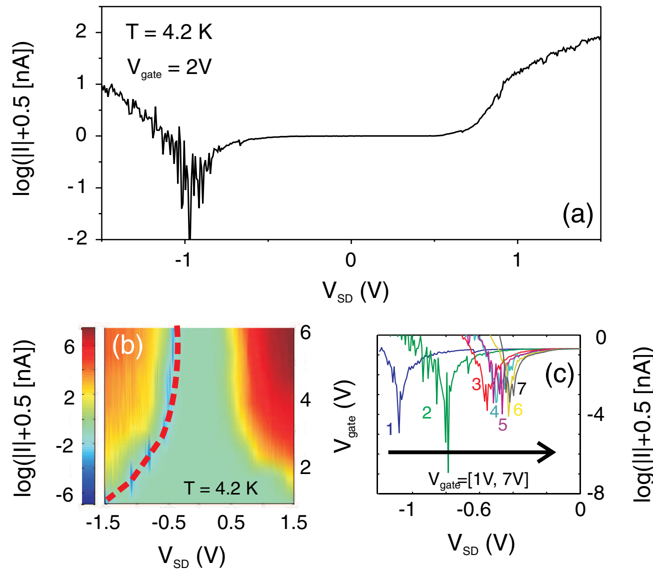

FIG. 5. (a): I-V characteristic of an InAs/InSb nanowire at cryogenic temperature. (b): Current map in the V_{SD}, V_{gate} parameter space (log scale). The red dashed line depicts the breakdown voltages. (c): Breakdown voltages for different gate biases. Note that, in all pictures, the data have been slightly shifted (+ 0.5 nA) in such a way that the breakdown is represented by the downward spikes.

by a dashed line. A cut of the current map is reported in Fig. 5(c) for the most interesting gate voltages. The possibility to control the breakdown voltages can represent a useful tool to improve the diode efficiency in rectifying electrical signals with large intensities.

It is possible to improve the diode rectification characteristics, suppressing even more the reverse-bias thermionic current, by inserting a barrier in between the heterojunction. The conduction band alignment of InP creates an electronic potential barrier with respect to both InAs and InSb semiconductors: a thin InP layer is then expected to greatly reduce the leakage current and thus improve the diode rectification curves. To understand this particular effect, we have realized nanodiodes with InAs/InP/InSb materials, with different InP barrier thicknesses. Since the nanowires are nominally undoped and of varying size, the charge concentration within the wires can fluctuate in a wide range, determining different band alignments and thus different rectification curves. To be able to fully compare different nanowires it is then necessary to apply some statistical analysis on different devices. To this end, we have defined a diode figure-of-merit (FOM) as the absolute value of the direct current divided by the reverse current at the same $|V_{SD}| = 500$ mV bias, at zero V_{gate}, and at room temperature. Figure 6(a) reports the obtained results for InAs/InSb wires with and without the InP insertion. In particular, devices with two different InP thicknesses have been realized, which are labeled as a thin (2.5 nm) and thick (5 nm) barrier, respectively. Indeed,

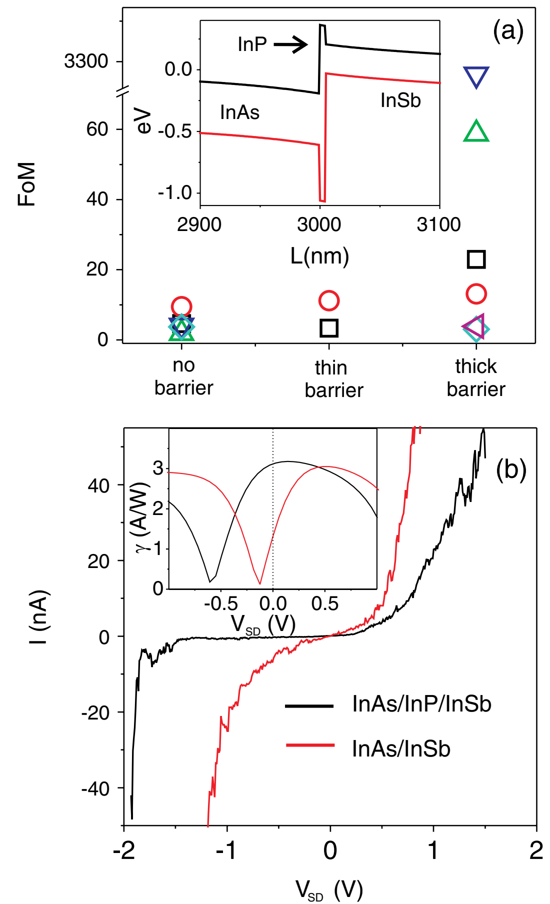

FIG. 6. (a): Figure-of-merit for InAs/InSb and InAs/InP/InSb nanowires, where thin (2.5 nm) and thick (5 nm) InP insertions have been considered Each symbol refers to a different sample. (b): Simulations of the expected band alignment are reported for an InSb carrier concentration of 10^{17} cm^{-3}. (c): Room-temperature rectification comparison for devices with and without InP (thick barrier). Inset: Second to first order current derivative ratio for the device with and without InP.

while the presence of the thin InP barrier does not lead to any statistical improvement in the FOM, most of the nanowires with the thick barrier show a better FOM, reaching extremely high values in a few individual, selected wires. It is worth stressing that the qualitative behaviors of both the InAs and InSb segments and the junction have been found to be the same in all the analyzed devices.

The main role of the InP layer should be represented by an increase of the barrier height, as reported in the band simulations of the inset of Fig. 6(a). The InP insertion suppresses the thermionic contribution, strongly reducing the leakage current of the reverse biased device. For direct bias, the InP effect is to partially hinder the tunneling current, resulting in a reduced high-bias conductance with respect to the InAs/InSb devices. This can be clearly seen for the zero gate voltage I-V characteristics of Fig. 6(b), where InAs/InSb and thick-barrier InAs/InP/InSb wires are measured at room temperature. Moreover,

the breakdown voltage results are strongly improved by the insertion of the InP barrier, shifting from about -1 V (InAs/InSb) to almost -2 V (InAs/InP/InSb) at zero V_{gate} bias. The ability to partially tune the rectification curve appeals to the use of nanowires as active elements in diode detectors, possibly up into the THz frequency range. In fact, as shown in the inset of Fig. 6(c), an estimate of the diode responsivity as a detector (defined as the ratio of the second to first order current derivative with respect to V_{SD}) from the room-temperature I-Vs of panel (b) shows the possibility of operating near zero bias in the nanowire with the InP barrier, which is extremely beneficial for the noise performance (we provide more on this later).

Figure 7(a)–7(c) reports low-temperature measurements, which confirm the room-temperature results. Comparing the measurements of panel (a) and (b) it is possible to appreciate that, while the diode breakdown does not appear in the selected V_{SD} range for the device with InP, it is clearly visible in the device with no InP insertion, reaching -0.5 V at the larger applied positive V_{gate}. As in the room-temperature case, this enhancement is accompanied by a small reduction in direct-biased nanowire conductance. For the sake of clarity, Fig. 7(c) reports the I-V characteristic at $V_{gate} = 8$ V of the two classes of devices, where all the peculiar features can be observed.

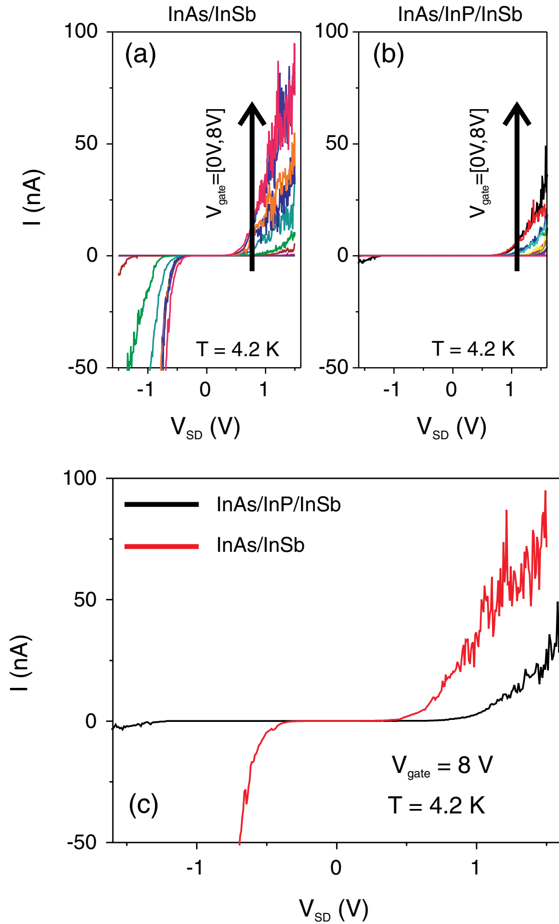

FIG. 7. (a): Low temperature I-V curves for InAs/InSb and InAs/InP/InSb nanowires, for a gate voltage of 8 V. (b)–(c): Low temperature I-V curves for the same wires for several gate biases in a range from 1 to 8 V. Note the different behavior of the breakdown voltages, which is greatly reduced in the device without an InP insertion.

The rectification curves of InAs/InP/InSb diodes are comparable (yet showing even larger breakdown voltages) to the ones presented in a recent report [8], in which *p-n* junction (InAs/GaAs/GaSb) nanowires were investigated. A further advantage of our devices is that gating is no required to obtain good room-temperature diode characteristics in simple two-terminal devices. This is particularly promising for the realization of rectifying detectors operating at zero bias. In this context, some interesting parameters can be easily extracted from the transport analysis.

The small capacitance of a single-wire diode can hardly be measured directly, although from measurements in similar nanowire systems [27] or from surface-rescaling of bulk systems constituted by similar materials [24], a capacitance of the order of few aF can be safely evaluated. With a series resistance of the order of 10–100Ω, a cutoff frequency ($f = 1/(2\pi RC)$) from tens to hundreds of THz is obtained, showing the potential of this system as an extremely fast diode detector. Moreover, a crude numerical estimation of the detector responsivity γ, defined as [16]

$$\gamma = \frac{\partial^2 I}{\partial V_{SD}^2}\left(\frac{\partial I}{\partial V_{SD}}\right)^{-1} \quad (1)$$

gives values of about 3–5 near zero bias, which is not too far from the values found in 2D tunnel diode systems. Most important, as seen in the inset of Fig. 6(c), γ peaks at almost zero bias for the device with thick InP layer insertion. This is particularly important since a zero-bias device shows a minimum noise, lacking the DC current contribution imposed by the applied V_{SD}. That is not the case for devices without an InP insertion: even if γ is not strongly modified, the working point is moved to $V_{SD} = 0.5$ V, with reduced performance and increased noise.

In conclusion, we have grown, processed, and experimentally investigated InAs/InSb heterostructured nanowires with or without a thin InP insertion layer. These nanostructures offer a new solution for nanowire-based electronic components. In particular, we have shown how the InAs/InSb *n-n* junction band alignment produces an extremely good current rectification effect. The insertion of an InP layer as additional barrier allow us to tune the rectification curve. With this approach we can achieve a voltage breakdown as high as -2 V with a leakage current that is 2 orders of magnitude lower than the direct one. The realization of this kind of device is promising as the main ingredient for THz rectifying detectors working at zero bias. Clearly, further developments are necessary in these devices to enhance the nonlinearity and reduce the device series resistance. For such purposes, improving contact

geometries, selective doping with Se, and the post-process to reduce the impact of surface traps represent particularly promising avenues.

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