Development of high power X-band semiconductor microwave switch for pulse compression systems of future linear colliders

Fumihiko Tamura and Sami G. Tantawi
Stanford Linear Accelerator Center, P.O. Box 4349, Stanford, California 94309
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We describe concepts for high power semiconductor rf switches, designed to handle signals at X-band with power level near 100 MW. We describe an abstract design methodology and derive a general scaling law for these switches. We also present a design and experimental work of a switch operating at the TE_{01} mode in overmoded circular waveguides. The switch is composed of an array of tee junction elements that have a *p-i-n* diode array window in the third arm.

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I. INTRODUCTION

In recent years there have been many suggestions for the rf pulse compression and power distribution systems for the Next Linear Collider [1]. One of the most attractive systems for high power pulse compression is the so-called SLED II system [2]. This system is based on storing the rf energy in resonant delay lines and switching, or discharging, it by means of phase manipulations. This system suffers from low efficiency at high compression ratios; the compression ratio being the ratio between the input pulse width and the output pulse width. Theoretical studies have shown that the efficiency of these systems can be improved if one discharges the system be means of an active switch [3].

The development of passive rf pulse compression systems has led to the invention of many novel rf components and systems which must handle up to 600 MW of pulsed power at X-band. These include passive waveguide components [4] and nonreciprocal devices [5]. The high power handling capabilities of these devices have been achieved by increasing the size of these components with respect to the operating wavelength, i.e., by overmoding these components. Similar attempts have been made to increase the power handling capabilities of bulk effect semiconductor components. Optically controlled semiconductor switches operating in overmoded waveguides have also been reported [6]. Here we report the development of a switch made from a *p-i-n* diode array operating in an overmoded waveguide carrying the TE_{01} mode.

The *p-i-n* diode rf switch was invented in the middle of the 20th century [7,8]. *p-i-n* diode switches have wide applications at the low to medium power levels. Various packaged *p-i-n* diodes are commercially available in the market. However, due to their small size, packaged *p-i-n* diodes cannot be used for switching very high power rf signals. Toward the end of the 1960s, a rectangular waveguide switch [9,10] was developed to handle higher power rf signals than packaged *p-i-n* diodes. The window switch was tested at the levels of 100 kW at X-band without problems. Thus, the power handling capability of a semiconductor rf switch has been at the levels of 100 kW; it is still low for the applications to the active pulse compression systems for future linear colliders.

A high power device can comprise an array of active elements arranged together so that the total electromagnetic fields are reduced and the power handling capabilities are increased. In this paper, we will discuss high power rf switches which consist of the active switching elements. The basic idea is to distribute the power into several elements so that the amount of the power to be handled by each element is reduced, in addition to the improvement of the maximum power of each element, by designing it in an overmoded structure.

In Sec. II we present the design methodology of the high power rf switch and the scaling law that governs the relation between the number of elements and the power handling capability. The design and implementation of a p-i-n/n-i-p diode array active window are described in Sec. III. We report on the results of low and high power experiments. We make some concluding remarks and point to future work in Sec. IV.

II. DESIGN METHODOLOGY OF HIGH POWER MICROWAVE SWITCHES

We will discuss the design methodology of high power microwave switches. We focus on SPDT (single pole double throw) switches, which have one input port and two output ports. Since one single active semiconductor device cannot handle very high power rf signals, the rf switch described here consists of several active switching elements. The load of the rf power is distributed to several elements; each element has to handle the reduced amount of the rf power.

A. Synthesis of the rf switch

The SPDT switch described here has two designs (see Fig. 1) [11–13]. Both designs consist of two 3 dB hybrids and two active modules. In the first design, the active module is an array of SPST (single pole single throw)

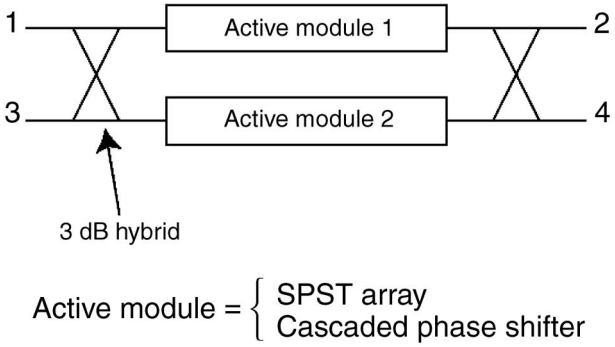

FIG. 1. Schematic diagram of the switch system.

switches. In the second design, the module is composed of a cascaded phase shifter.

In the case of the SPST array (see Fig. 2), the active modules have two statuses, i.e., the perfect reflection status and the perfect transmission status. When an rf signal is reflected perfectly at the modules, all power goes to port 3. Also, when the modules transmit 100% of power, the output is port 4.

In the case of the cascaded phase shifter (see Fig. 3), the phase difference between two active modules is chosen 0 and π. The output port is 4 and 2 with phase difference 0 and π, respectively.

Each cascaded element of the phase shifter and the SPST switch has a similar design: the *active element*. This element consists of a symmetrical three-port tee junction, a short plane in the third arm, and an active waveguide window placed in the third arm of the symmetrical tee junction. A schematic view of the active element is shown in Fig. 4.

The active window is a waveguide window that changes the reflection coefficient by the external control input.

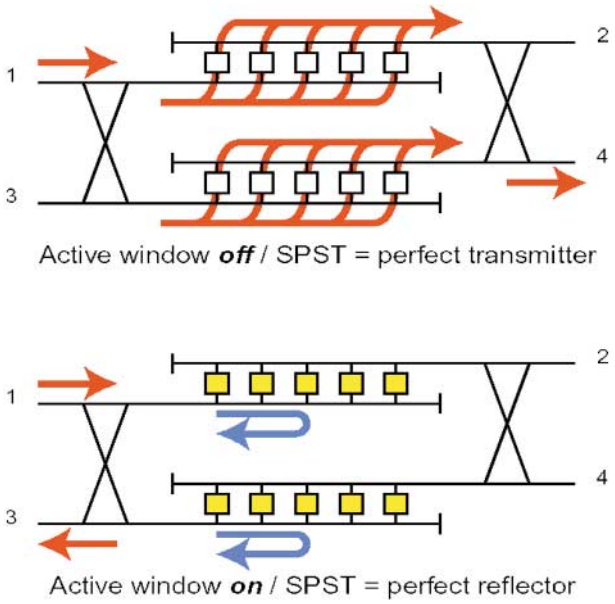

FIG. 2. (Color) Operating principle of SPST array.

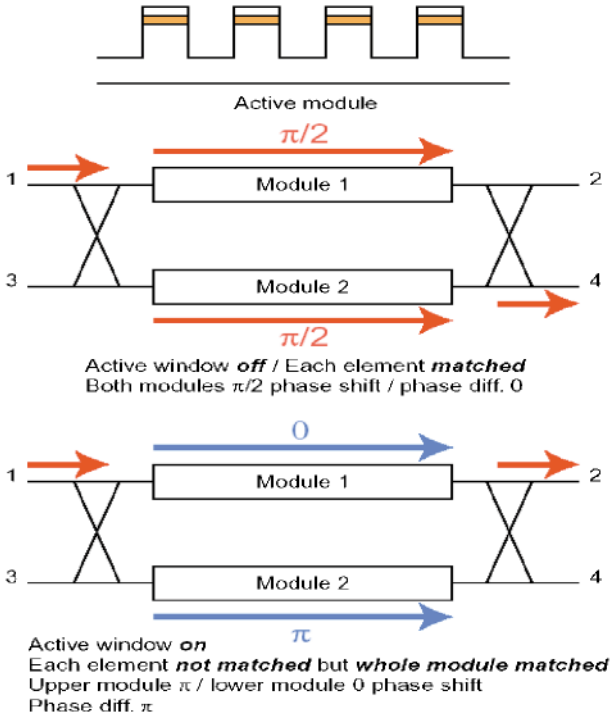

FIG. 3. (Color) Operating principle of cascaded phase shifter.

Here, the perfect transmission status of the active window is called *off* and the perfect reflection status is called *on*.

As a result of putting the short plane in the third arm, the active element is a two-port network. The basic idea of the active element is to change the S matrix of the two-port network by changing the reflection phase in the third arm. As shown in Fig. 4, when the active window is on, the signal in the third arm is reflected at the active window. The situation is equivalent to putting a short plane at the position of the active window. Thus, the S matrix of the two-port network changes.

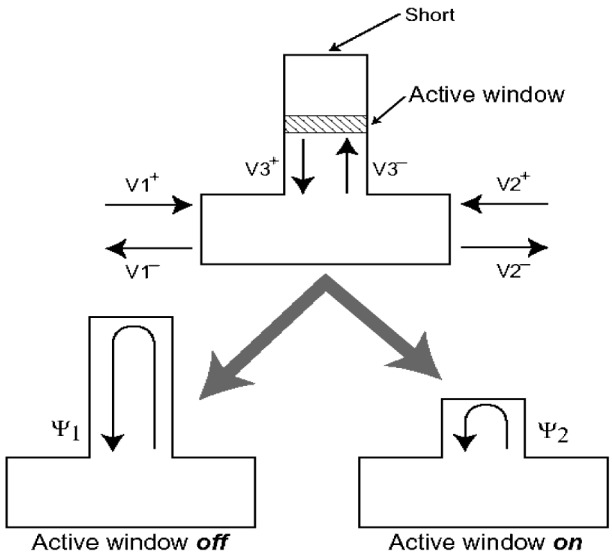

FIG. 4. The active element.

B. The three-port network as a control element

A symmetrical tee junction of an arbitrary shape is illustrated in Fig. 5. The S matrix of the lossless symmetrical tee junction may be parameterized [6] by defining an adequate reference plane. It is given by

$$\underline{\underline{S}} = \begin{pmatrix} \frac{e^{j\phi}-\cos\theta}{2}\, e^{j\alpha} & \frac{-e^{j\phi}-\cos\theta}{2}\, e^{j\alpha} & \frac{\sin\theta}{\sqrt{2}}\, e^{j\alpha} \\ \frac{-e^{j\phi}-\cos\theta}{2}\, e^{j\alpha} & \frac{e^{j\phi}-\cos\theta}{2}\, e^{j\alpha} & \frac{\sin\theta}{\sqrt{2}}\, e^{j\alpha} \\ \frac{\sin\theta}{\sqrt{2}}\, e^{j\alpha} & \frac{\sin\theta}{\sqrt{2}}\, e^{j\alpha} & \cos\theta \end{pmatrix}, \quad (1)$$

where the parameters ϕ and θ determine the coupling between the ports of the tee junction, and α is a parameter which specifies the location of the reference planes of ports 1 and 2. The scattered rf signals $\underline{V}^-$ are related to the incident rf signals $\underline{V}^+$ by $\underline{V}^- = \underline{\underline{S}}\underline{V}^+$, where $V_i^{\pm}$ represents the incident/reflected rf signal from the ith port.

When a short plane terminates the third arm, the wave reflected at the short plane has the same amplitude, and has the phase advance Ψ, which is determined by the distance d between the reference plane and the short plane. The voltage of the reflected wave is given by

$$V_3^+ = V_3^- e^{2j\beta_3 d} = V_3^- e^{j\Psi}, \quad (2)$$

where β_3 is the wave number in the third arm and Ψ is the reflection phase advance. The scattering matrix parameters for the symmetric two-port network formed by the shorted three-port network can be calculated from Eqs. (1) and (2) and are given by

$$\underline{\underline{S}} = \begin{pmatrix} \cos(\frac{\zeta-\phi}{2})e^{j[(\phi/2)+(\zeta/2)+\alpha]} & j\sin(\frac{\zeta-\phi}{2})e^{j[(\phi/2)+(\zeta/2)+\alpha]} \\ j\sin(\frac{\zeta-\phi}{2})e^{j[(\phi/2)+(\zeta/2)+\alpha]} & \cos(\frac{\zeta-\phi}{2})e^{j[(\phi/2)+(\zeta/2)+\alpha]} \end{pmatrix}, \quad (3)$$

where ζ is defined by

$$e^{j\zeta} \equiv \frac{\cos\theta - e^{j\psi}}{\cos\theta e^{j\psi} - 1}. \quad (4)$$

Since the tee junction is a lossless network, the wave in the third arm is a pure standing wave. The maximum standing wave voltage in the third arm at the distance ξ from the short plane is obtained as

$$|V_3| = |V_3^-||1 - e^{2j\beta_3\xi}| = 2|V_3^-||\sin\beta_3\xi|. \quad (5)$$

The amplitude of the normalized voltage in the third arm is given by

$$|V_3^+| = |V_3^-| = \frac{1 + \cos^2\theta + 2\cos\theta\cos\zeta}{2\sin^2\theta}|V_1^+ + V_2^+|. \quad (6)$$

Hence, the maximum electric field of the standing wave in the third arm $E_{\max}$ at the distance ξ from the short plane is given by

$$E_{\max} = 2\left(\frac{1 + \cos^2\theta + 2\cos\theta\cos\zeta}{2\sin^2\theta}\right)^{1/2} \times |\sin\beta_3\xi|\left(\frac{P_{\text{in}}Z}{AG}\right)^{1/2}, \quad (7)$$

where P_{in} is the input power which is equal to $|V_1^+ + V_2^+|^2$, Z_g is the waveguide impedance, A is the cross sectional area of the third arm waveguide, and G is a geometrical factor that depends on the mode and the waveguide shape of the third arm.

When the short plane has a surface resistivity R_s, the loss P_l dissipated into the short plane is given by $4|V_3^-|^2\frac{R_s}{Z_g}$. Using Eq. (6) the loss dissipated into the short plane in the third arm is explicitly given by

$$P_l = 4\,\frac{1 + 2\cos\theta\cos\zeta + \cos^2\theta}{2\sin^2\theta}\,\frac{R_s}{Z_g}\,P_{\text{in}}. \quad (8)$$

C. SPST array

The operating principle of the SPST array is shown in Fig. 2. In the SPST array configuration, the 3 dB hybrid

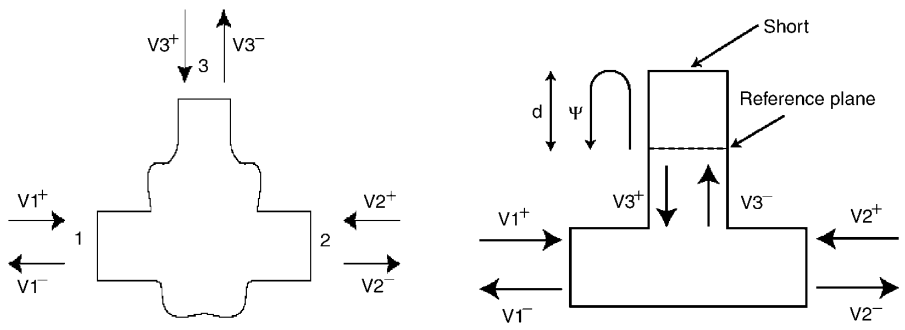

FIG. 5. (a) Symmetrical tee-junction element. (b) The three-port network as a control element.

and the power dividers divide the input power, then the power is guided to each SPST switch. The SPST switches described here work as a perfect transmitter and a perfect reflector when the active windows are off and on, respectively. When the active windows are off, each divided power goes through the SPST switches and is combined in the power divider. The recombined power goes to port 4 through the 3 dB hybrid. Also, when the active windows are on, each SPST switch reflects the power perfectly, and then all power goes to port 3.

From the S matrix of the two-port network Eq. (3), the matching condition of the SPST switches, i.e., $S_{11} = 0$, is given by

$$\zeta_0 = \phi + (2N + 1)\pi , \tag{9}$$

where N is an integer. Hence, the short plane is placed at the position where Ψ_0 satisfies the following condition:

$$e^{j\Psi_0} = \frac{e^{j\phi} - \cos\theta}{-1 + e^{j\phi}\cos\theta} . \tag{10}$$

Also, the perfect reflector condition, i.e., $S_{11} = 1$, is given by

$$\zeta_1 = \phi + 2N\pi . \tag{11}$$

In this case, the active window is placed at the position where Ψ_1 satisfies the following condition:

$$e^{j\Psi_1} = \frac{e^{j\zeta_1} + \cos\theta}{1 + e^{j\zeta_1}\cos\theta} . \tag{12}$$

In the SPST array configuration, each active element handles $1/n$ of the total input power, where n is the number of elements. The maximum electric field at the active window when the active window is off and $\zeta_0 = \phi + \pi$ is given by

$$E_{\max} = 2\left(\frac{1 + \cos^2\theta - 2\cos\phi\cos\theta}{n\sin^2\theta}\right)^{1/2} \times \left|\sin\frac{\Delta\psi}{2}\right| \left(\frac{P_{\text{in}}Z_3}{A_3G_3}\right)^{1/2} , \tag{13}$$

where $\Delta\psi = \psi_0 - \psi_1$ and can be calculated from Eqs. (10) and (12), and the suffix 3 in the last term refers to quantities that define the properties of the third arm and have the same definitions as in Eq. (7).

The total loss P_l dissipated into the active windows when the active window is on and $\zeta_1 = \phi$ is given by

$$P_l = 2\,\frac{1 + \cos^2\theta + 2\cos\phi\cos\theta}{\sin^2\theta}\,\frac{R_s}{Z_3}\,P_{\text{in}} . \tag{14}$$

D. Cascaded phase shifter

The operating principle of the cascaded phase shifter is illustrated in Fig. 3. In the case of the cascaded phase shifter, the active modules have two states. The phase difference between the two active modules is 0 or π. We may choose the total phase shift of the modules as follows: (i) The total phase shift in each of the upper and lower active modules in Fig. 3 is $\pi/2$. The phase difference between the two modules is 0. The output port is port 4 in Fig. 3. This status is realized when the active windows in the active elements are off and *each element is matched by itself*. (ii) Total phase shift in each of the upper and lower active modules is 0 and π, respectively. The phase difference between the two modules is π. The output port is port 2. This status is realized when the active windows in the active elements are on. *Each element is not matched by itself*, but the whole module is matched by cascading.

In the status of phase difference 0, each active element is set to be matched by itself. The matching condition of the active elements is $\zeta_0 = \phi + \pi$, the phase Ψ_0 is given by Eq. (10).

Substituting into Eq. (3), we find that the phase advance of each element is $\phi + \alpha + \pi$. Each active module consists of $n/2$ elements and has the total phase shift $\pi/2$. The total number of elements in two modules is n. This means $(\phi + \alpha + \pi)n/2 = \pi/2$; that is, $\alpha = \pi/n - \pi - \phi$. The reference plane of ports 1 and 2 of the active element is chosen so that this condition is satisfied.

When the active window is on, each element is not matched by itself, but the whole module is matched. The matching condition is given by following the procedure.

We may introduce the transfer matrix A of a two-port network [11,14]. Each active module consists of $n/2$ active elements. When the active module is matched and the total phase shift across the module is π, the transfer matrix must satisfy $A^{n/2} = -I$, where I is the identity matrix. Hence, the eigenvalues of A are $e^{\pm j[(4m+2)\pi/n]}$, where m is an integer. Similarly, when the phase shift of the module is 0, the transfer matrix satisfies $A^{n/2} = I$ with eigenvalues given by $e^{\pm j[(4m+4)\pi/n]}$.

From these eigenvalues of the transfer matrix, we can derive the condition of ζ_1. Explicitly,

$$\zeta_1 = \phi - 2\tan^{-1}\left(\frac{\sin\frac{\pi}{n}}{\cos\frac{\pi}{n} - \cos\frac{M\pi}{n}}\right), \tag{15}$$

where M is an integer given by

$$M = \begin{cases} 4m + 4, & \text{total phase shift is } 0 , \\ 4m + 2, & \text{total phase shift is } \pi . \end{cases} \tag{16}$$

By noting that each active window handles one-half of the total input power, the maximum field at the active window when it is off can be explicitly calculated,

$$E_{\max} = \left(\frac{1 + \cos^2\theta - 2\cos\phi\cos\theta}{\sin^2\theta}\right)^{1/2} \times \left|\sin\frac{\Delta\psi}{2}\right| \left(\frac{P_{\text{in}}Z_3}{A_3G_3}\right)^{1/2} , \tag{17}$$

where $\Delta\psi = \psi_0 - \psi_1$ and can be calculated from Eqs. (10) and (12) with the appropriate value for ζ_1 given by Eq. (15). Note that with increasing the number of elements n, the phase $\Delta\psi$ becomes smaller, hence, the maximum voltage at the window is reduced.

The loss dissipated into the active window in each active element when the active window is on is given by

$$P_l(\text{each}) = 2\,\frac{1 + \cos^2\theta + 2\cos\phi\cos\theta}{\sin^2\theta}\,\frac{R_s}{Z_3}\,|V_1^+ + V_2^+|^2. \tag{18}$$

Since each element is not matched by itself, there is a standing wave in the waveguides between the elements. Thus, the normalized voltage $|V_1^+ + V_2^+|$ when the active window is on is always more than 1 and it depends on the position of the element in the module. With increasing the number of elements, $|V_1^+ + V_2^+|$ becomes closer to the minimum value, near 1. Assuming the number of elements is large enough and $|V_1^+ + V_2^+|$ is near 1, the total loss dissipated into the active windows is approximated by

$$P_l(\text{total}) = \frac{n(1 + \cos^2\theta + 2\cos\phi\cos\theta)}{\sin^2\theta}\,\frac{R_s}{Z_3}\,P_{\text{in}}\,. \tag{19}$$

E. Scaling law

We will discuss the scaling law, which governs the relation between the power handling capability and the number of active elements. Since we are interested in switching rf signals at very high power levels, it is important to estimate the number of elements required to handle a certain amount of power. The criteria that determine the number of elements are (i) the maximum electric field at the active window must be kept below the maximum electric field limit of the semiconductor device and (ii) the loss dissipated into the active window must be kept within a priory given value that depend on the application. On most rf pulse compression systems the switch is required to have losses below 2%.

We have derived expressions for the maximum electric field at the active window when the active window is off, and the loss dissipated into the active window when the active window is on, in the cases of both the SPST array and the cascaded phase shifter. By relating these expressions, we will derive the scaling law. First we notice that the scattering matrix S for the three-port network contains two variables, θ and ϕ. Indeed, for any choice of ϕ, one can find a value for θ such that Eqs. (13), (14), (17), and (19) preserve their values. Hence the choice of the angle ϕ is arbitrary. For simplicity we will set $\phi = 0$.

Let us start with the case of the SPST array. We assume that the active element is matched by itself when the active window is off, and it is a perfect reflector when the active window is on. Let us define L_0 as the acceptable *relative* loss determined from external requirements Then, at the limit, $P_l(\text{total})/P_{\text{in}} = L_0$. With the previous assumption about ϕ, one can write

$$L_0 \equiv P_l(\text{total})/P_{\text{in}} = 2\,\frac{R_s}{Z_g}\tan^2\frac{\theta}{2}\,, \tag{20}$$

where R_s is the surface resistance and Z_g is the waveguide impedance in the third arm. Using the above equation one can write Eq. (13) as

$$E_{\max} = 2\left(\frac{R_s P_{\text{in}}}{nL_0AG}\right)^{1/2}. \tag{21}$$

Similarly, for the cascaded phase shifter one can relate the losses to the peak field. In the case of the cascaded phase shifter, the active element is matched by itself when the active window is off and the total change of the phase advance of the active module is $\pm\pi/2$. We assume that the total number of active elements n is large enough so that the phase shift of each element when the active window is on is fairly small. With this assumption, the reflection phase change $\Delta\psi \ll 1$ and it would not disturb the matching condition. Also, we can neglect the effect of the standing waves between each active element. With these assumptions one can show that the losses are given by

$$L_0 = \frac{2\pi R_s}{\Delta\psi Z_g}\,. \tag{22}$$

With the help of this equation and the above assumptions, Eq. (17) becomes

$$E_{\max} = \pi\left(\frac{R_s P_{\text{in}}}{nL_0AG}\right)^{1/2}. \tag{23}$$

From Eqs. (21) and (23) one can write the scaling law for both the SPST array and the cascaded phase shifter array,

$$n = C^2\,\frac{P_{\text{in}}}{L_0}\,\frac{1}{AG}\,\frac{R_s}{E_{\max}^2}\,, \tag{24}$$

where P_{in} is the total input power, R_s is the surface resistance of the active window when it is on, L_0 is the acceptable relative loss determined by external requirements, n is the total number of active elements, A is the cross sectional area of the waveguide, and G is a geometrical factor that depends on the mode and the shape of the waveguide. In the above equation, C is a constant, π for the cascaded phase shifter and 2 for the SPST switch array. This means that the case of the SPST array is better than that of the cascaded phase shifter. However, the case of the cascaded phase shifter might offer an easier implementation since it does not require the set of splitters to distribute the power as in the SPST array case.

It is now appropriate to make some remarks about this scaling law. (i) The SPST array configuration needs less active elements than the cascaded phase shifter. (ii) The number of elements is proportional to the surface resistance, and inversely proportional to the acceptable loss. Hence, we should employ the active window with low loss when the window is on. (iii) The number of elements is inversely proportional to the square of the peak electric field limit. Thus, it is necessary to choose the material and the device which can endure high electric fields, as the active window. (iv) The number of elements is independent of the waveguide impedance Z_g. The effects of Z_g on the

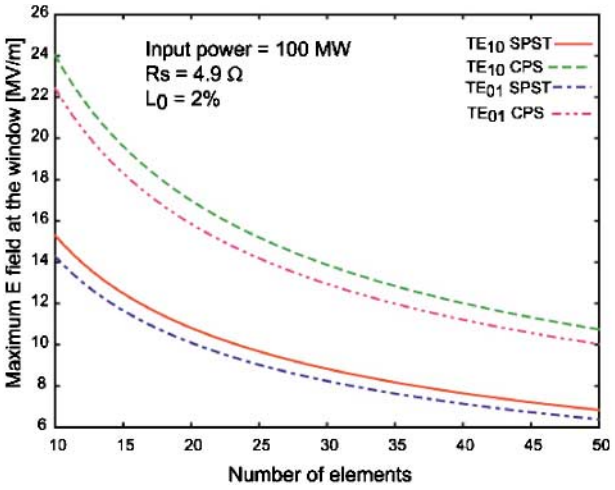

FIG. 6. (Color) Number of elements versus maximum electric field of the active window.

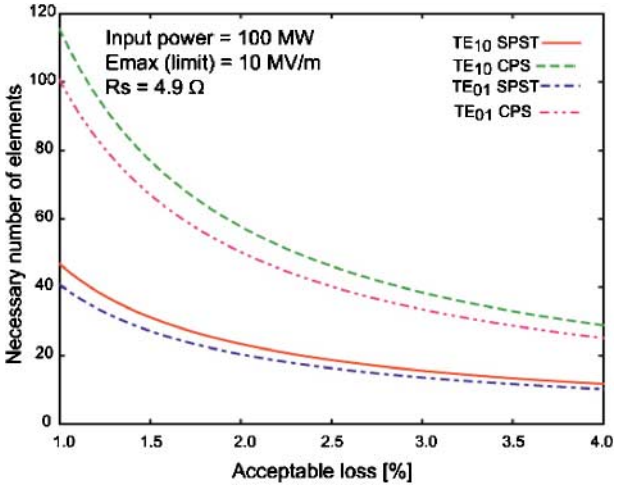

FIG. 8. (Color) Acceptable loss versus necessary number of elements.

increase of electric field and the decrease of loss cancel each other.

In the derivation of the scaling law, we did not use any device-specific characteristics. Hence, this scaling law is quite general, it can be used not only for the p-i-n/n-i-p diode switches described in the following sections, but also for the optically driven switches [6] or other kinds of active switches, such as magnetic switches [5].

Now we can estimate the required number of elements for a given application. For example, we use the p-i-n/n-i-p diode array active window, described in the following sections, with the following assumptions: (i) the operating frequency is 11.424 GHz; (ii) the maximum field limit on the silicon window is 10 MV/m [7]; (iii) the acceptable loss L_0 when the active window is on is 2%, which is required for the application to the pulse compression systems [3]; (iv) the surface resistance R_s obtained by a maximum carrier density of 10^{17} cm^{-3} is 4.9 Ω; and (v) the total input power is 100 MW.

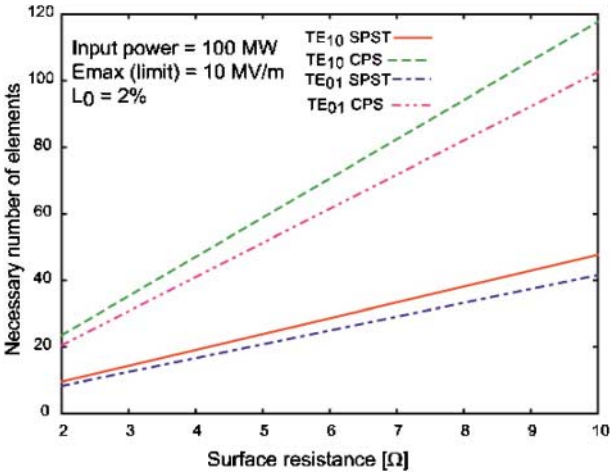

FIG. 7. (Color) Surface resistance versus necessary number of elements.

If we employ TE_{10} mode active windows in WR90 rectangular waveguides, we find from Eq. (24) that 24 and 58 elements are needed for the SPST array and the cascaded phase shifter, respectively. With TE_{01} mode active windows in 1.3-in. diameter circular waveguides, 21 and 51 elements are needed, respectively. The correlation between the number of elements and the maximum electric field at the active window is shown in Fig. 6. In the figure, the input power, the acceptable loss, and the surface resistance are fixed. From the figure, we can clearly see that we must employ the material and the device that has a high field limit as the active window to save the number of elements. Also, in Figs. 7 and 8 the correlations between the number of elements and the parameters concerning the loss at the window, the surface resistance, and the acceptable loss are shown. As described above, the number of elements is proportional to the surface resistance when the active window is on; we must choose the window that has a high conductivity when the window is on. If the external requirements allow a larger loss for the total system, the number of elements becomes less. However, the local heating at the window will be an issue. Independent of the scaling law, this issue must be handled carefully.

III. DESIGN AND IMPLEMENTATION OF p-i-n/n-i-p DIODE ARRAY ACTIVE WINDOW

A new active window, p-i-n/n-i-p diode array active window which is operated at TE_{01} mode in the circular waveguide was proposed and developed. Our active window is designed and built to avoid the difficulties of the TE_{10} mode rectangular waveguide window switch and handle X-band rf signals at multimegawatt levels. This is achieved by using an overmoded structure hence increasing the cross sectional area and reducing the power density. Since the TE_{01} mode in circular waveguide does not have any electric field at the waveguide wall, this makes the design more robust by avoiding edge effects.

In this section, the design of our p-i-n/n-i-p diode array active window will be described.

A. The silicon window

The conceptual view of our active window is illustrated in Fig. 9. The base material of the window is highly pure silicon. This window is located in a circular waveguide, which is operated at the TE_{01} mode. As shown in Fig. 9, the p-i-n/n-i-p diode structure is a set of radial lines. Each line is heavily doped by p-type and n-type impurities on the topside and back side surfaces, respectively. Each diode line is covered by a metal line, which supplies bias voltage and current to the diode line. The electric field of TE_{01} is shown in Fig. 9. All electric field lines of the TE_{01} mode are in the azimuthal direction; i.e., the diode lines are perpendicular to the electric field of the rf signal. This means that the reflection caused by the diode structure and the metal lines is very small when the active window is reverse or zero biased; the rf signal sees only the dielectric contribution of the bulk silicon material. This is the off status of the active window. To minimize the reflection from the lines, the *coverage factor*, which is defined as the ratio of the area of the diode structure to that of the whole active region of the window, is chosen to be 10%. The p lines on the topside and the n lines on the back side are arranged to alternate with each other (see Fig. 9). A side-cut view of the active window illustrates the idea; see Fig. 10. When forward bias is applied, a massive number of injected carriers go across the i region. Since the p and n lines are alternating, the injected carriers fill the i region; the incident rf signal is reflected. This is the on status of the active window. The thickness of the active window, which is the same as the i region width in this design, must be small enough so that the carriers injected from the heavily doped p and n lines by the forward bias can diffuse through the high receptivity i region to the heavily doped lines on the other side. This is a very important point to achieve good rf isolation at the on status. The carrier lifetime in the high resistivity silicon material is closely related to the diffusion length of the carriers. Namely, $L_D = (\tau D_{AP})^{1/2}$, where L_D is the diffusion length of the carriers, τ is the carrier lifetime in the silicon material, and D_{AP} is the diffusion coefficient. The diffusion coefficient in silicon is $D_{AP} = 15.6\ \mathrm{cm}^2/\mathrm{s}$, then we get $L_D \approx 40[\tau(\mu\mathrm{sec})]^{1/2}\ \mu\mathrm{m}$. Hence, the base material of the active window must be very pure silicon and must have long carrier lifetime to achieve good conductivity modulation with forward bias. While this puts an upper limit on the window thickness, there is a lower limit for this thickness. If the window is much thinner than the skin depth, good isolation of the rf signal would not be obtained. If we assume the carrier density to be $10^{17}\ \mathrm{cm}^{-3}$ in the i region with forward bias, then the skin depth δ_s can be calculated by the knowledge of the carrier motilities of silicon. At a frequency of 11.424 GHz, $\delta_s \approx 100\ \mu\mathrm{m}$.

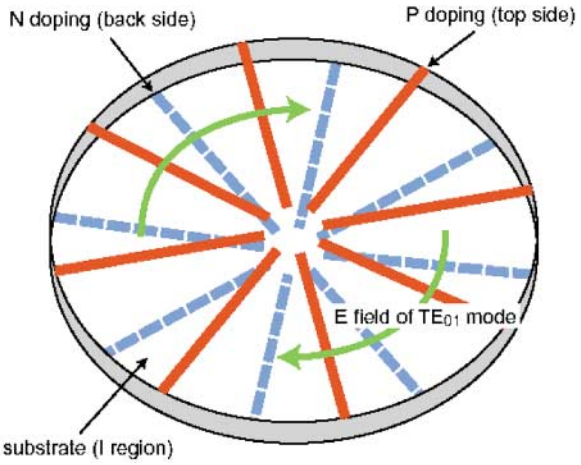

FIG. 9. (Color) Conceptual view of p-i-n/n-i-p diode active window.

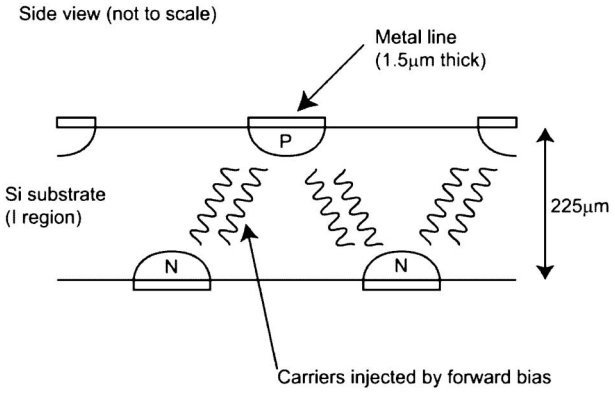

FIG. 10. Side view of p-i-n/n-i-p diode active window.

In the actual design of our active window, the diode structure consists of 400 radial lines each on the topside and the back side. The width of the radial lines are tapered, it is 25 μm near the waveguide surface and 2 μm near center of the active window. This line width and the number of lines are chosen so that the coverage factor is 10%. This active window is operated at 11.424 GHz. The diameter of the active region of the window is 1.299 in. Also, the thickness of the window is 225 μm. If the carrier density achieved $10^{17}\ \mathrm{cm}^{-3}$, this thickness is more than the skin depth of the intrinsic region for X-band rf signals.

At a carrier density of $10^{17}\ \mathrm{cm}^{-3}$ the surface resistance $R_s \approx 4.8\ \Omega$ at 11.424 GHz. In our design, the diameter of the active region and waveguide is 1.299 in., so that the waveguide impedance is 4.16 times the impedance of vacuum. Hence, the loss dissipated into the window, when the window is on, is given by $L_0 \equiv P_l(\mathrm{total})/P_{\mathrm{in}} = 4\frac{R_s}{Z_g} \approx 1.23\%$.

B. Process flow

The processing of the p-i-n/n-i-p diode array active windows was done by the author at the Stanford

Nanofabrication Facility [15] of Stanford University. As shown in the previous section, the carrier lifetime is strongly related to the carrier density in the intrinsic region when forward bias is applied. Since the i region width is long [the same as the wafer thickness (225 μm)], a pure material with very high resistivity is needed to achieve high density of the carriers injected by forward bias. Our starting material, silicon wafers, is doped approximately 10^{12} cm^{-3}, and the resistivity is more than 5000 Ω cm. The minority carrier lifetime in the material is more than a millisecond.

The complete process flow is shown in Table I. The process of the p-i-n/n-i-p diode structure is based on a common and standard integrated circuit (IC) fabrication process. The method is illustrated in Fig. 11. The initial oxidation process makes the silicon dioxide layers on the surfaces of the wafers. The target thickness of the oxide layer is 4000 Å. The oxide thickness is checked by the noncontact spectroreflectometry measurement. Boron and phosphorus are chosen as the p-type and n-type impurities, respectively. They are implanted at 100 keV into the silicon substrate through the holes of the oxide layer. These holes of the oxide layer are formed by the wet etching process in hydrofluoric acid.

The aligner manufactured by Karl Suss used to define the lines and the holes is a contact aligner and has resolution better than 0.75 μm for both topside and back side alignments; this aligner is accurate enough to define our diode structures. The dose shown in the table is for the 10^{16} cm^{-3} version of the doping density. For the 10^{17} cm^{-3} version, 10 times heavier dose is used. After the implantation of the impurities, the high temperature drive-in process is done to diffuse the impurities into the silicon substrate. The depth of the diffusion is about 5 μm after 16 h of the drive-in process at 1150 °C. In the same process, a 2000 Å thick oxide layer is formed on the hole used for the implantation of the impurities.

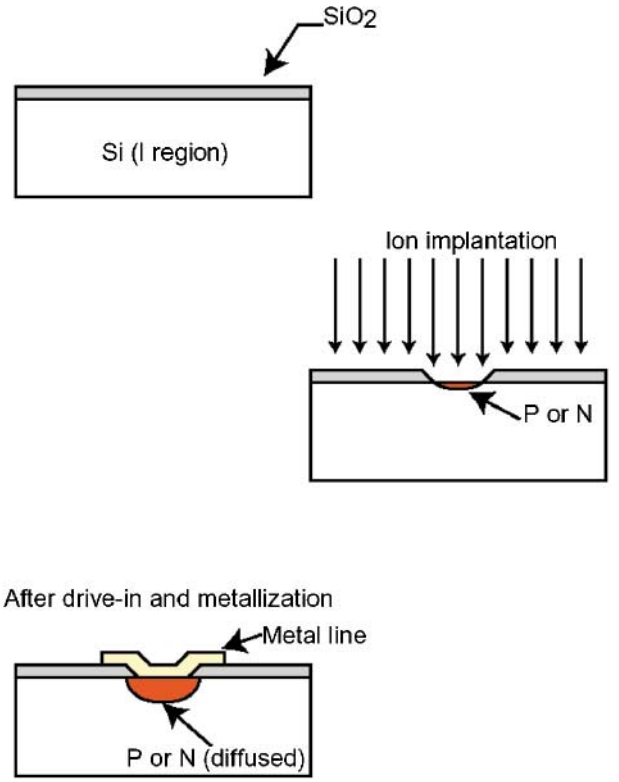

FIG. 11. (Color) Fabrication method.

Then, the contact holes are formed over the diffusion lines by a wet etching process so that the metal lines and

TABLE I. Process flow for p-i-n/n-i-p diode array active window.

Mask	Purpose and parameters
	Starting material: ⟨100⟩ n-type 5000-cm 4 in. Si wafers
	Initial oxide growth 0.4 μm in steam at 1000 °C for 1 h
Mask 1 (top)	p-doping definition
	Oxide etch topside
	Implant topside: boron 100 keV 6×10^{13} cm^{-2}
Mask 1 (back)	n-doping definition back side alignment done by Karl Suss aligner
	Back side alignment done by Karl Suss aligner
	Oxide etch back side
	Implant back side: phosphorus 100 KeV 6×10^{13} cm^{-2}
	Drive-in impurities into silicon: at 1000 °C: 35 min Ar, 10 min dry O_2, 30 min wet O_2, 10 min dry O_2, at 1150 °C: 16 h
Mask 2 (top and back)	Contact hole definition
	Oxide etch both sides
	Metal deposition (both sides), sputter aluminum 1.5 μm thick
Mask 3 (top and back)	Metal line definition
	Etch aluminum (wet etch)
Mask 4 (top)	Deep trench etch definition
	Bond backing support wafers
	Deep silicon etch thorough wafers (225 μm) by Surface Technology Systems deep reactive ion etcher
	Remove backing wafer by dipping in acetone (several days)

the diffusion lines contact each other through the contact hole. Aluminum is sputtered on the surfaces of the wafers. The thickness is set to be 1.5 μm. The metal line is formed through the wet etching process by mixed acid. Finally, a deep trench etched at the design diameter of the window cuts the wafer.

C. rf structures and window support

The rf structure to support the window is shown in Fig. 12. It consists of two aluminum circular waveguides with steps, a ceramic ring, and metal springs. The active window is located between the two waveguides. The ceramic ring fixes the active window at the design position.

The TE_{01} mode rf signal is launched by a compact wrap-around mode converter [16]. The diameter of the waveguides changes from 1.5 in. at the low impedance section to 1.3 in. at the high impedance section by the steps. The steps are designed so that the whole rf structure is matched by itself *without* the active window. Since silicon has a large dielectric constant, the impedance mismatch at the surface of the active window is large; the reflection from the window surface caused by this mismatch is not zero. However, this rf structure is designed and built without a matching section, which compensates for the mismatch at the surfaces of the active window. This is done because we are interested in the pure characteristics of the active window.

The two waveguides are dc separated. The ceramic ring works as the dc voltage gap. There are metal springs between the active window and the waveguides. The waveguides are connected to a biasing circuit. The biasing voltage is supplied to the active window through the waveguides and the springs. The waveguides are dc isolated from the TE_{01} mode converters by a Mylar insulators.

There is a gap between the two waveguides, but no choke structure. Since the surface currents of TE_{01} mode in circular waveguides are azimuthal, the gap does not cut any surface currents and there is no rf leakage through the gap. Indeed, this a big advantage of this structure over TE_{10} mode in rectangular window switches. We can avoid the complex choke structure, which is necessary in the rf structures of this later type.

Finally, since this structure needs to operate under vacuum, all gaskets for sealing the vacuum are Viton rubber gaskets for dc isolation.

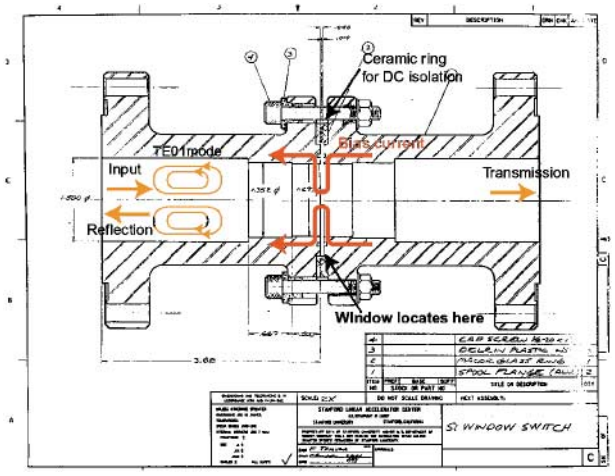

FIG. 12. (Color) Active window and rf structure.

IV. EXPERIMENTAL RESULTS

A. Low power measurements

Two types of low power measurements were performed: the network analyzer measurement and the active switching experiment with biasing. In the network analyzer measurement, the passive characteristics of the window supporting rf structure and the active window were examined. Also, in order to test the basic switching performance of the p-i-n/n-i-p diode array active window, the active switching experiment with a low power rf source was performed.

The schematic diagram of the passive measurement is shown in Fig. 13. The S parameters (S_{11} and S_{21}) of test devices, the window supporting rf structure, and the p-i-n/n-i-p diode array active window are measured by the network analyzer (HP8510) at the operating frequency 11.424 GHz.

Without the window, the S parameters of the rf structure were $S_{11} = -26.79$ dB and $S_{21} = -0.085$ dB, respectively. The total loss was 1.7%, including 1.4% loss of two TE_{01} mode converters. The supporting rf structure is almost perfectly matched. When the bulk silicon, with oxide but without diode and metal structure on the surface, was placed, the S parameters were $S_{11} = -2.500$ dB

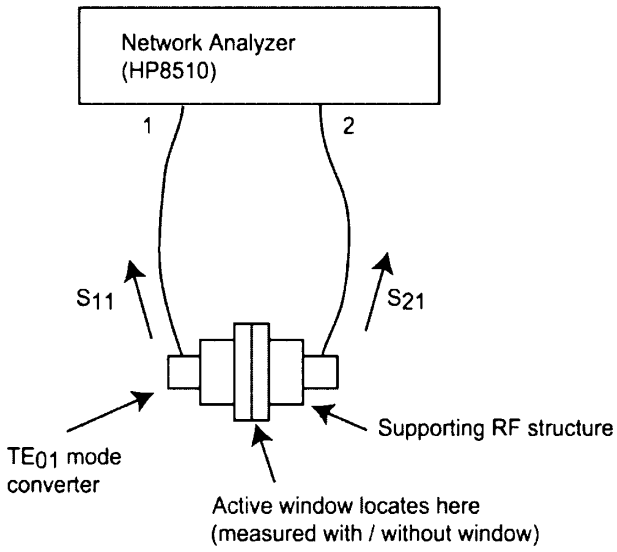

FIG. 13. Schematic diagram of the network analyzer measurement.

and $S_{21} = -3.9872$ dB. The total loss was 3.9% including the loss of mode converters. The loss at the window was 2.5%. This result is consistent with theoretical calculations. When the active window with full p-i-n/n-i-p diode array structure on both sides of the window was inserted, the S parameters were $S_{11} = -2.429$ dB and $S_{21} = -4.1726$ dB. The total loss was 4.5%, and the loss at the window was 3.1%. These S parameters are very close to those of the bulk silicon window. The difference between the losses of the window without and with the diode structure was 0.6%. This 0.6% of power was dissipated into the heavily doped diode structure. Hence, we confirmed that the reflection caused by the radial line structure with the coverage factor of 10% is reasonably small.

The schematic diagram of the active switching experiment is shown in Fig. 14. The rf signals generated by the signal generator are amplified to 1 W, and guided to the active window through an isolator and directional couplers. The reflection and the transmission of incident rf signals are picked up through 20 dB directional couplers and measured by the peak power meter (HP8990A). The voltage across the diode window is measured. Also, a current transformer measures the current through the diode window.

Prior to the active measurement, the characteristics of the rf components in the test setup were checked by the network analyzer. The measurement results are shown in Table II. The isolator had -34.08 dB reflection coefficient at the port facing the active window. Thus, it was confirmed that there is no parasitic resonance in the test setup caused by the reflection of the components.

The 10^{16} cm^{-3} doping density version was used for this experiment. The typical waveforms with the various forward bias and zero reverse bias are shown in Figs. 15–17.

TABLE II. Characteristics of the components.

Component	Characteristics
Isolator	Forward direction is port 1 → port 2 $S_{11} = -33.45$ dB, $S_{21} = -0.74$ dB, $S_{12} = -32.12$ dB, $S_{22} = -34.08$ dB
Terminator	-63 dB reflection
Directional coupler 1	Power pickup: -19.9 dB reflection: less than -40 dB
Directional coupler 2	Power pickup: -20.27 dB reflection: less than -50 dB

In these figures, the horizontal axis is time. The S parameters of the total test set, including the active window, the rf structure, and the TE_{01} mode converters, are plotted.

As shown in the figures, when the forward bias voltage was applied, the carriers were injected into the intrinsic region and the conductivity of the intrinsic region increased significantly. As a result, the reflection from the active window increased and the transmission decreased. The rise time of the reflection and the transmission modulation is dominated by the speed of the diffusion process. It showed weak dependency on the applied voltage.

When the forward bias was turned off, the transmission and the reflection recovered to the initial state slowly. The natural recovery time of the transmission was about 50 μs.

The maximum forward bias current of 115 A was achieved. With this maximum forward current, the total reflection was modulated to -0.6 dB and the total transmission was modulated to -22 dB. Comparing with the result of the network analyzer measurement described in the above, $S_{11} = -2.429$ dB, $S_{21} = -4.1726$ dB, the maximum transmission modulation was 18 dB.

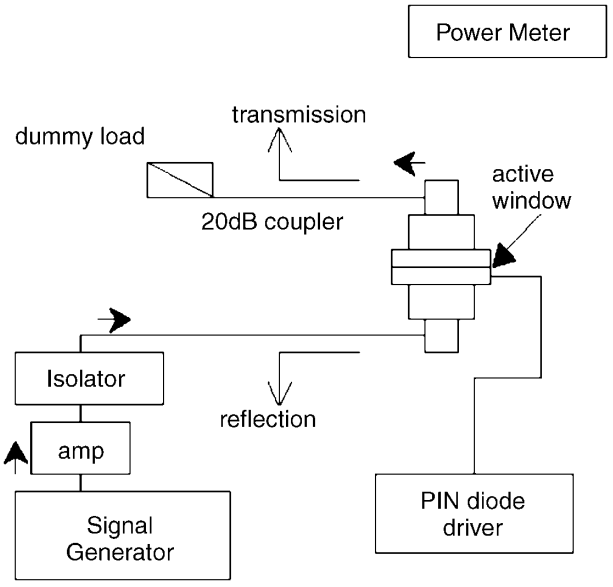

FIG. 14. Schematic diagram of the low power measurement.

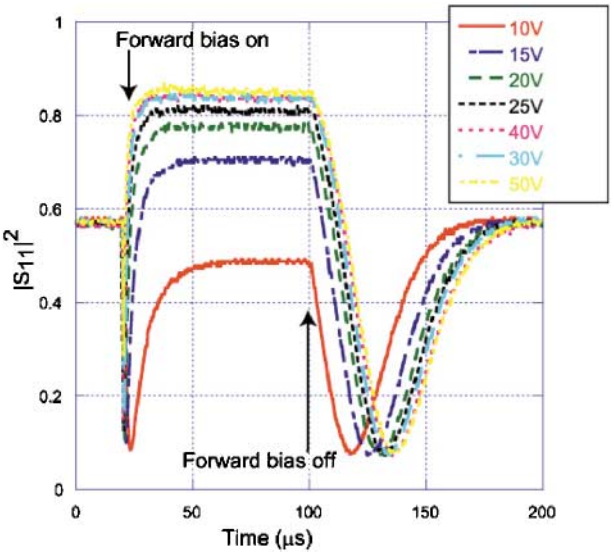

FIG. 15. (Color) Typical waveform of reflection with various forward biases.

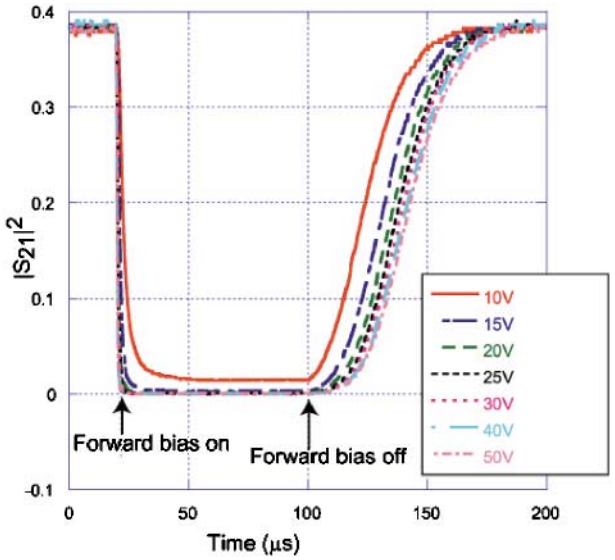

FIG. 16. (Color) Typical waveform of transmission with various forward biases.

The total loss with the 115 A forward bias current was 13.9% including the 1.4% loss of the TE_{01} mode converters. Hence, the loss dissipated into the active window was ~11.5%. From the measured loss of the active windows, the conductivity of the intrinsic region is calculated as 13.8 Ω/cm assuming a uniform distribution of the carriers in the intrinsic region. This conductivity corresponds to a carrier density of 7×10^{14} cm^{-3}.

In Fig. 18, the waveforms with a zero bias and a reverse bias at -120 V are plotted. As shown in the figure, the switching time was improved from 50 μs with no reverse bias to 20 μs with the -120 V reverse bias. When the transmission is close to zero, the curve of the transmission recovery without and with the reverse bias is almost the same. This means that the effect of the reverse bias voltage is not much when the intrinsic region is filled with the injected carriers. The reverse bias is effective after the relative transmitted power exceeds 0.05; the reverse bias voltage sweeps the carriers.

This result can be explained as follows. When the intrinsic region is filled with a lot of carriers, the *p-i-n* diode has very low resistance. Hence, most of the voltage drop occurs at the *external* resistance of the circuit, which includes (i) the resistance of the biasing circuit, (ii) the contact resistance between the metal springs and the surfaces of the active window and the rf structure, and (iii) the resistance of the thin metal lines on the surface of the window. The diode feels a low voltage and the electric field in the diode to sweep the carriers is small. In this situation, the carrier sweeping by the reverse bias voltage is not efficient. When the carrier density in the intrinsic region becomes relatively low, the voltage drop across the diode becomes higher. Thus, the carriers can be swept by the reverse bias faster than the case of zero bias. Therefore, reducing external resistance is necessary to sweep the carriers in the intrinsic region faster.

The 10^{17} cm^{-3} doping density version was also tested. However, the switching performance with the forward bias was not as good as the 10^{16} cm^{-3} version. At 60 V forward bias, the forward bias current was only 30 A and only

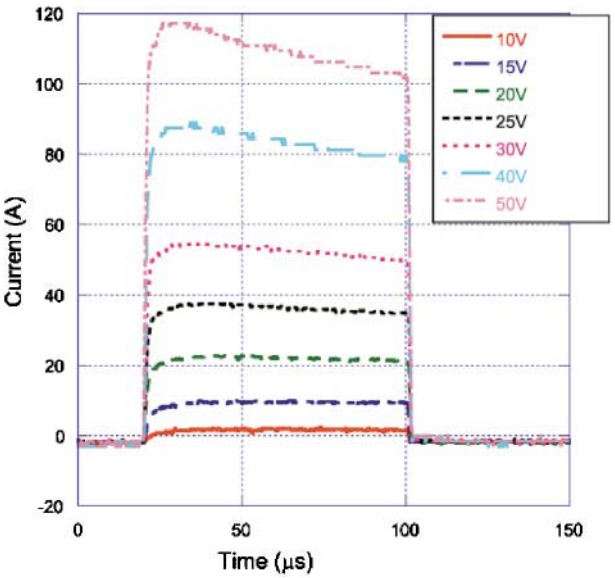

FIG. 17. (Color) Current with various forward bias voltages.

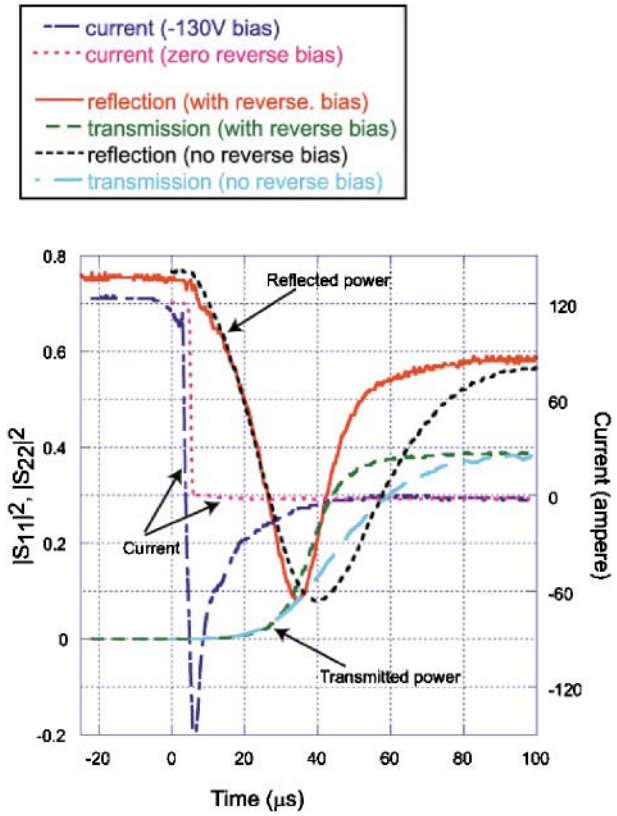

FIG. 18. (Color) The recovery from forward bias to reverse bias.

50% transmission modulation was achieved. It is quite possible that this was because of large contact resistance between the aluminum lines and the diode structure caused by processing problems. The highly likely scenario is that the natural oxide was not removed completely when aluminum was sputtered onto the silicon wafer.

As described above, the loss dissipated into the active window when the window is on was 11.5% and the achieved carrier density was 7×10^{14} cm^{-3}. The fastest switching speed from forward to reverse bias was 20 μs. To meet the requirements for the application of active pulse compression systems, the loss should be lower and the switching speed should be faster.

In this experimental version of active window, a low doping density was chosen to avoid the avalanche breakdowns with the dc reverse bias. The achieved carrier density in the intrinsic region, 7×10^{14} cm^{-3}, is a reasonable value for the 10^{16} cm^{-3} doping level. If the doping density is increased to 10^{19} cm^{-3}, many more carriers will be injected into the intrinsic region and the loss dissipated into the active window will be lower. In that case, the reverse bias should be applied to the window in a short pulse, because high reverse dc bias voltage will cause avalanche breakdown. Some possibilities to improve the switching speed of the active window will be discussed in conclusion section.

B. High power experiments

1. Results of passive high power experiment

As described in Sec. II, the power handling capabilities of one single active window directly determines the number of active elements required to handle a certain amount of power. The high power experiment is necessary to examine the feasibility of the application of the high power switches to rf pulse compression systems.

The high power experiment was performed by using the high power *X*-band klystron (XL-2) and SLED-II rf pulse compression system at SLAC. The schematic diagram of the high power experiment is shown in Fig. 19. The high power rf signal of 900 ns pulse duration was generated by the klystron (the operating frequency is 11.424 GHz). The rf pulse was compressed by SLED-II pulse compression system. The compressed rf pulse was fed to the active waveguide window. Typical waveform of the SLED-II output with a dummy load is shown in Fig. 20. In the figure, the klystron output signal of 50 MW is compressed to 200 MW. Since the window was not matched we used the pulse compression system to isolate the klystron from our window. Also it allowed us to operate the klystron at a relatively low power level so that it cannot be harmed by reflected rf power from the pulse compression system and the active window combination. The power level output from the pulse compression system to the active window was up to 15 MW. For our experiments, this power level was high enough. The pulse duration of compressed rf signal was 150 ns. Since the active window did not have cooling systems, the repetition rate was limited to 5 Hz.

The incident rf signal, the reflected signal, and the transmitted signal were measured by power meters and rf diode detector through directional couplers.

The TE_{01} mode converters have view ports to watch the surfaces of the window so that the video camera can detect flashing lights if arc occurs on the surface of the active window.

Two types of silicon windows were prepared for this high power experiment. The first silicon window is an active window, which has a full p-i-n/n-i-p diode array structure on both the topside and the back side. This active window is the 10^{17} cm^{-3} doping density version. The resistivity of the base material is 5000 Ω cm. The window thickness is 225 μm. The second silicon window had only the metal line structure on one side and no doping line structure; the other side had no structure (*metal-only version*). This version of the window was prepared for investigating the breakdown properties of the thin metal structure. The resistivity of the base material of this window is 1000 Ω cm and the thickness is 315 μm.

In Fig. 21, the reflected and transmitted powers from the active window with full diode structure are plotted. As shown in the figure, the reflected and transmitted powers were proportional to the input power. Hence, the reflection

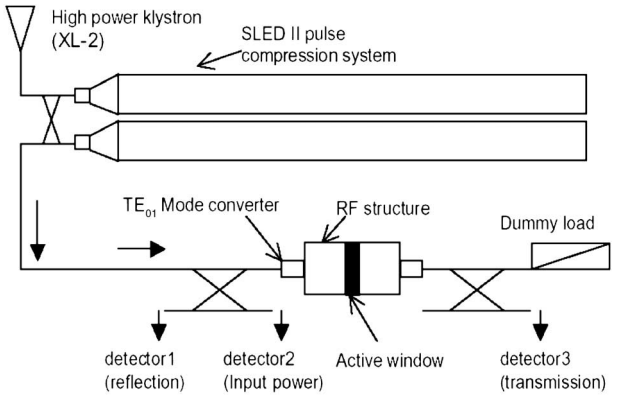

FIG. 19. Schematic diagram of the high power experiment.

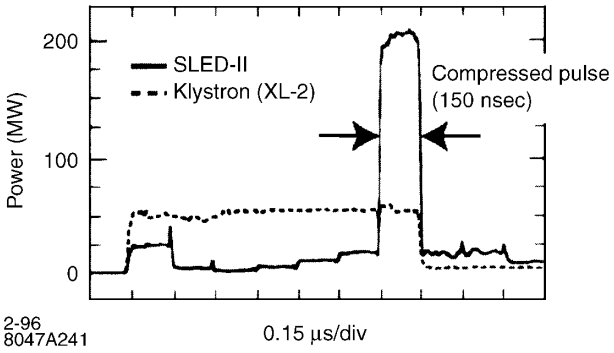

FIG. 20. SLED-II output signal.

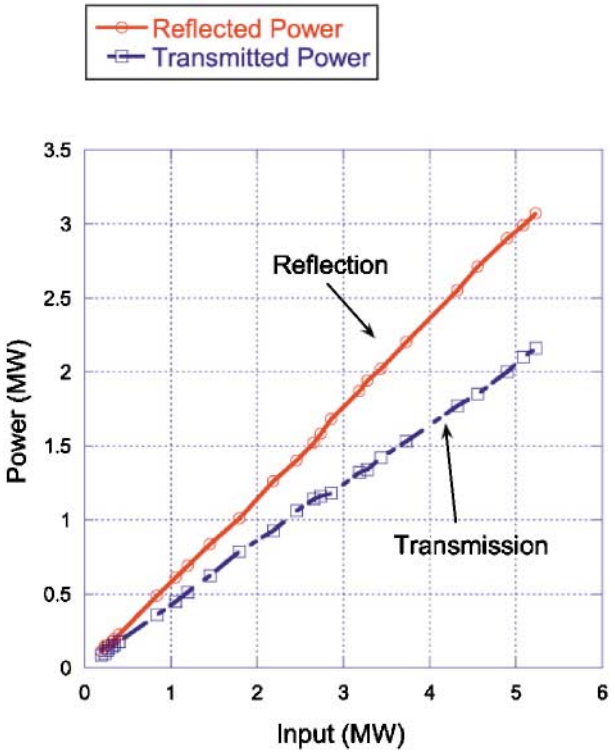

FIG. 21. (Color) Input versus transmission and reflection power.

coefficient did not change and the loss dissipated into the active window did not increase with increasing the input power up to 5.2 MW. This means that avalanche breakdowns did not occur at this power level. If the avalanche breakdown occurred, there would be a massive number of carriers in the intrinsic region, and reflection coefficient of the active window would have changed.

However, arcing started at the input power level of around 4 MW. When arcing occurred, the vacuum in the system became worse than about 10^{-5} Torr from 10^{-8} Torr at the normal high power operation, then the interlocks stopped the klystron. In Fig. 22, the waveforms of the transmitted and reflected rf signals when the arcing occurred are plotted. After the arcing started, the reflected power increased and the transmitted power decreased slowly.

This arcing was very vacuum dependent. We had to process slowly from the lower power levels after the trips. Flashing lights were observed by the video camera from both sides when the arcing occurred. These characteristics, vacuum dependency and flashing lights, are typical characteristics of the vacuum breakdowns, not the characteristics of avalanche breakdowns.

After achieving the maximum input power of 5.2 MW, the arcing occurred more and more frequently. Also, the arcing occurred at the lower power levels; i.e., we could not raise the input power any more. Thus, the high power operation was limited by this arcing. The maximum field at the surface of the window is calculated as 3.8 MV/m when the input power was 5.2 MW.

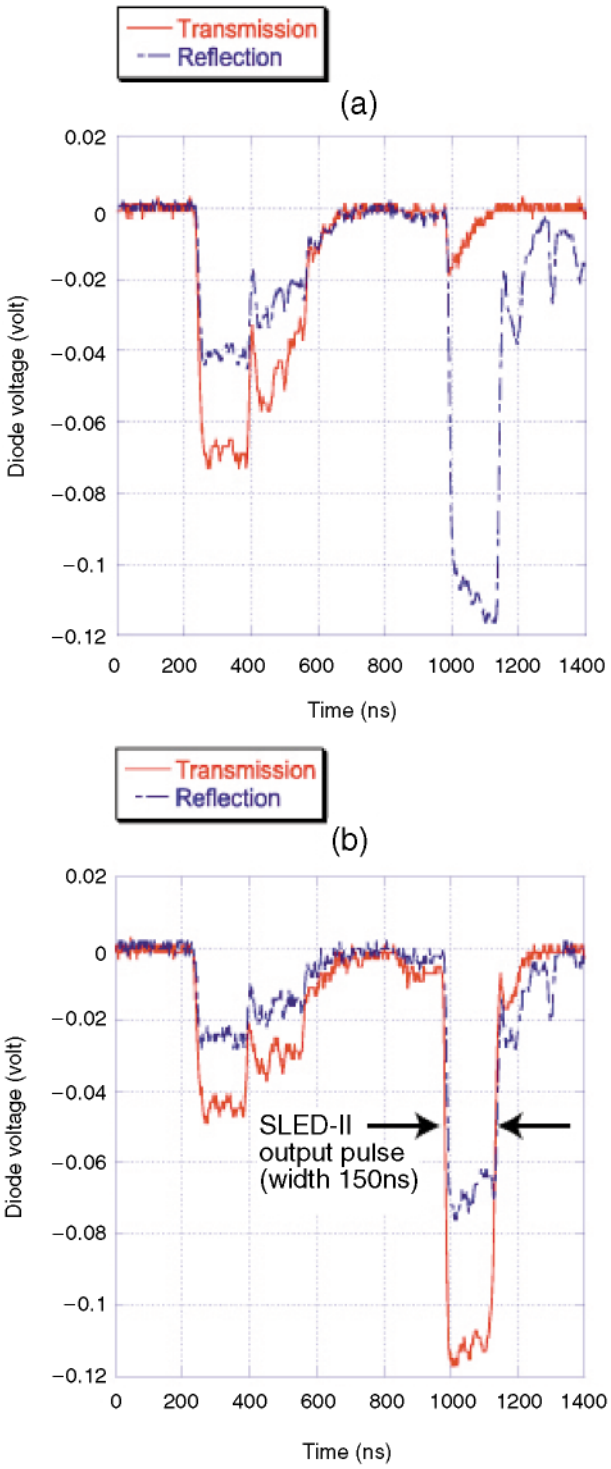

FIG. 22. (Color) Typical waveforms of reflected and transmitted rf signals when arc occurred. Bottom graph (b) shows waveform without arcing (metal-only version).

The pictures of the surface of the active window after this high power experiment are shown in Fig. 23. As shown in the figure, it is clear that the metal lines have many arcing traces but the silicon surface is not damaged at all. The arcing spots of the metal lines are similar to typical discharge traces. It is reasonable to assume that

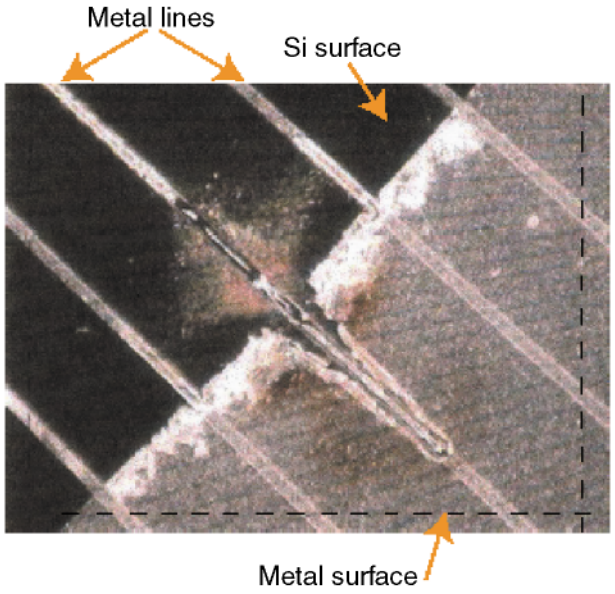

FIG. 23. Lines burned by biasing currents.

the arcing during the high power operation occurring between the metal lines and the vacuum became worse by aluminum vapor.

The metal-only version was also tested. The window was set in the system so that the downstream side had the metal structure. The metal-only version showed results similar to the active window with full p-i-n/n-i-p diode structure. The arcing between the metal lines on the surface limited the high power operation. The maximum input power of 12 MW was achieved. After the high power operation, similar arcing traces were observed on the metal lines. The silicon surface had no arc traces and no damage.

We tried the repetition rate of 30 Hz with the metal-only version. An interesting thing happened at the input power level of about 4 MW. The reflection increased significantly to almost full input power level, and it was kept high for long time (several minutes) even with much lower input power. We believe that, with 30 Hz of repetition rate, the window was heated to high temperature at several hundred degrees and the intrinsic carrier density in the silicon was increased by the thermal agitation. From this result, it is clear that, for the real application, some kind of cooling systems of the active window is necessary.

2. Results of high power switching experiment

As described above, the switching speed of the p-i-n/n-i-p diode array active window is not fast enough to switch the SLED-II output pulse within the pulse duration. Hence, the forward bias current was started before the klystron pulse started, and was kept for the entire klystron pulse duration.

The waveforms of the transmitted and reflected rf signal with and without the forward bias voltage are shown in Fig. 24. With the forward bias voltage at 130 V, the reflection increased and the transmission decreased. The reflected rf signal was modulated from 1.1 to 1.68 MW, and the transmitted rf signal was modulated from 0.63 MW to 60 kW. A 10 dB of transmission modulation was achieved. With the forward bias, no arcing on the surface of the active window was observed. It is reasonable because the active window is a conductor. When the window is biased in forward direction, the electric field of rf signal is minimum near the window surface.

However, after several hours of the active switching operation, the conductivity modulation became worse. Even with higher voltage, the forward current was not enough to modulate the reflection coefficient of the active window. Finally, no forward current would go through the active window.

The active window and the rf structure are connected to the dc biasing signal by metal springs. The contact is poor; the number of contact point touching the surface of the window and rf structure is the same as the number of curls in the spring, about a hundred. Also, each contact point has very small area. Hence, the total area of the contact is very small. The contacts became worse because the high forward current density destroyed them, then the forward bias could not go through.

Also, after the high power switching operation, several burned metal lines were found (see Fig. 23). The burned

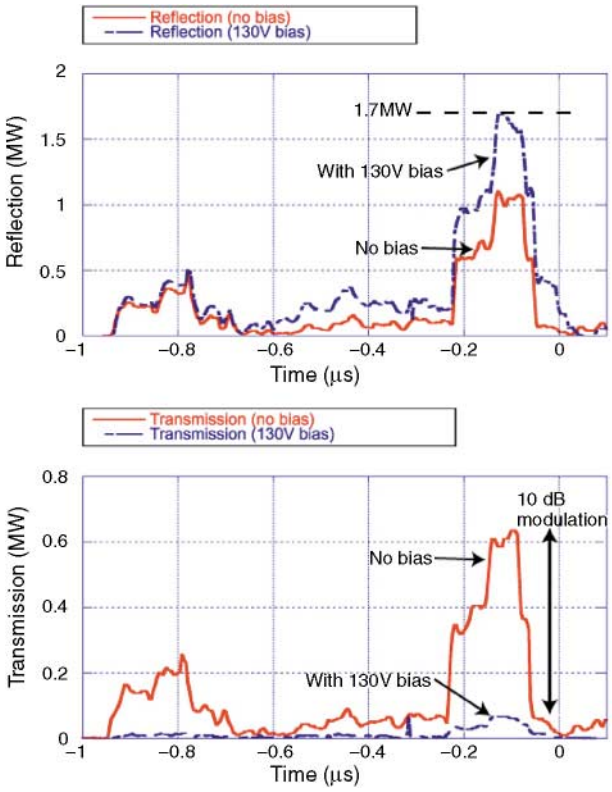

FIG. 24. (Color) Waveform with zero bias and 130 V forward bias.

position is very close to the wall of the waveguide, where the electric field of TE_{01} mode is minimum. The biasing current burned them.

The high power switching operation was limited by the poor contact between the active window and the metal springs. Also, the thin aluminum lines were a problem for the forward biasing operation.

V. CONCLUSIONS AND DISCUSSION

In this paper, we have discussed high power microwave switches for the applications to the rf pulse compression systems of the future linear colliders. We described theoretical and experimental studies of high power microwave switches.

The design methodology of the high power SPDT switch, which consists of active elements, was developed. The active element is composed of a symmetrical tee junction, a short plane, and an active window. Two configurations of the SPDT switch were described: the SPST array and the cascaded phase shifter. In both configurations, the load of the rf power is distributed to several active elements. The maximum electric field at the active window when the window is off and the loss dissipated into the active window when the active window is on are important properties. Rigorous expressions for the maximum electric field and the loss were derived.

The scaling law, which governs the relation between the number of elements and the power handling capability, was developed. The number of elements is proportional to the loss at each window and inversely proportional to the square of the maximum electric field limit of the window. Hence, the maximum electric field of the active window dominated the necessary number of elements.

A new p-i-n/n-i-p diode array active window were designed and built. The active window is built over a silicon substrate, which has the p-i-n/n-i-p diode array structure on both surfaces of the substrate. The array structure on each side consists of 400 heavily doped lines covered by metal lines. The lines do not disturb the TE_{01} mode rf signals because all lines are perpendicular to the electric field lines of that mode. The processing of the active window is based on the standard and common IC processing. The rf structure was designed and built. The structure supports the active window at a designated position and gives the electrical contact for biasing. The low power measurement of the active window demonstrated 18 dB of transmission modulation. The losses dissipated into the active window were 11.5%.

A high power experiment of the active window using a high power X-band klystron and a SLED-II pulse compression system was performed. Without bias, the active window was tested at up to 5.2 MW, to be compared with 100 kW of the power levels in past experiments. No avalanche breakdown in the silicon occurred. It has been confirmed that silicon active windows can handle rf signals at the levels of multimegawatts. However, the arcing between the metal lines on the surface of active window limited the high power operation.

The switching speed could be improved by reducing the resistance of the circuit, by paralleling the biasing circuits, and by reducing the window thickness. Also, employing thick metal lines and covering the window surface with a dielectric layer can help reduce the arcing problem.

To conclude this study, we address the question: Is it *possible* to use silicon windows for switching very high power rf signals? The experimental results give the answer *yes*. Although more work is needed for real applications, it should be emphasized that silicon active windows can handle high power X-band rf signals at the power levels of multimegawatts.

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