

Development and tests of fast 1-MA linear transformer driver stages

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In this article we present the design and test results of the most powerful, fast linear transformer driver (LTD) stage developed to date. This 1-MA LTD stage consists of 40 parallel RLC (resistor R, inductor L, and capacitor C) circuits called “bricks” that are triggered simultaneously; it is able to deliver ~ 1 MA current pulse with a rise time of ~ 100 ns into the ~ 0.1 -Ohm matched load. The electrical behavior of the stage can be predicted by using a simple RLC circuit, thus simplifying the designing of various LTD-based accelerators. Five 1-MA LTD stages assembled in series into a module have been successfully tested with both resistive and vacuum electron-beam diode loads.

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I. INTRODUCTION

The linear transformer driver (LTD) is a developing pulsed-power technology which shows promise for applications that require high-power, high-voltage, high-current, ~ 100 -ns output pulses. The LTD driver is an induction generator similar to the linear induction accelerator (LIA) [1,2], the inductive voltage adder (IVA) [3–6], and the linear pulsed transformer (LPT) [7]. All induction generators are based on Faraday’s law which states that the time-varying magnetic flux $B(t)$ penetrating a loop generates at the ends of this loop a voltage difference $U(t)$ equal to

$$U(t) = S \frac{dB}{dt}, \quad (1)$$

where S is the cross section of the loop. In an induction generator normally the loop is realized as a pillbox-shaped toroid, which in this article is called “induction cavity.” This toroid has a continuous azimuthal gap, and the voltage $U(t)$ appears across this gap. Since historically the first devices utilizing Faraday’s law were called “transformers,” all induction generators can also be considered as transformers. Hence, the induction cavity can be considered as the single-turn secondary winding of such a transformer. Its primary winding, which generates the azimuthal magnetic flux $B(t)$ that penetrates the cavity, may have different designs. A LIA is composed of a series of identical induction cavities. When assembled, it has a cylindrical region on axis, referred to as the bore, which has a series of annular gaps regularly spaced on its inner cylindrical surface. This bore is threaded by a beam of propagating particles which gets accelerated as they drift through each of the cavity gaps. The voltage across a given gap appears in coincidence with the passage of the particles

through the gap. Hence, the firing sequence of each LIA cavity is synchronized with the speed the particles propagate along the axis of the device.

IVA is also formed by a series of identical induction cavities, but unlike in LIA, its bore is threaded by a center conductor that together with the cylindrical surface of the bore form an output line that connects to the load. The outstanding advantage of the IVA is that this line serves as a transmission line; i.e., the electromagnetic (EM) energy propagates along this line from each cavity towards the load only, without reflections. In an ideal IVA two fundamental principles must be satisfied: first, the firing of the successive cavities must be synchronized with the speed in which the EM wave propagates along the output line, and second, the wave impedance of the output line must gradually increase to be matched with the drive impedance of the upstream cavities. In an ideal IVA [excluding IVAs driving magnetic insulated transmission lines (MITLs)], the output voltage pulse across a matched load is *independent of the number of cavities and is equal to the sum of all cavity pulses*.

LPT can be formed by one or a series of identical induction cavities. If it is one cavity only, it encloses several parallel primary windings that are triggered simultaneously. The gap of this cavity is located not on the inner surface of the toroid but on its side surface, and it must be insulated for the total output voltage. Since all primary windings are triggered simultaneously, the discharge circuit of the single-cavity LPT consists of the primary energy sources that are connected in series to the load through the inductance of the toroid. This inductance widens the output pulse, and therefore the output pulse of the single-cavity LPT is not the sum of the primary pulses applied to each primary winding. An IVA-type device consisting of several

induction cavities, where one or both of the above listed fundamental IVA principles are violated, is also an LPT in a sense that its output pulse is not a sum of the primary pulses. If any IVA principles are violated, the output line does not serve as a transmission line because the waves undergo multiple reflections; then the shape of the output pulse depends on the number of the cavities and on the width of the primary pulses. In particular, if the length of the primary pulses is much longer than the electrical length of the output line, this line serves as a series inductance, exactly in the same way as the inductance of the toroid in the single-cavity LPT.

Similar to IVA and LPT, the LTD driver consists of several induction cavities called “LTD stages” plus the center electrode threading through the axis of the cavities. The main difference from LIA, IVA, and LPT induction cavities is that the *LTD stage encloses the primary capacitive energy storage* [8]. The LTDs have several important advantages that make this technology attractive for the next generation of pulsed-power systems: (i) Since the LTD stages enclose the primary storage, the LTD driver is more *compact* compared to other generators having similar output parameters. For example, the footprint of a 1-TW, 10 LTD cavity driver is only $\sim 8 \text{ m}^2$. (ii) As any other primary energy storage, the LTD driver is *simple*. As described below, an LTD stage consists mainly of only three different parts: a capacitor, a gas spark switch, and a ferromagnetic core. (iii) Since the LTD primary energy storage is enclosed inside the cavity, it is practical and convenient to be built with relatively small size capacitors, which necessarily have less capacitance C . But this turns to be an important advantage for LTDs since the small (10–40 nF) capacitance becomes instrumental for directly generating short output pulses even if the inductance of each of the basic circuit (“brick”) may be relatively large ($\sim 250 \text{ nH}$). Each “brick,” described in detail in Sec. II, consists of two capacitors and one switch connected in series. A high-current LTD cavity encloses many such bricks connected in parallel to the load. (iv) Since the LTD driver consists of several individually triggerable stages, it can be operated in both LPT and IVA modes.

All the above advantages of the LTD technology offer the capability [9–15] to build fast, 100-ns time-scale compact and simple high-power drivers without any intermediate power amplification stages.

In Sec. II of this paper we describe the design of the most powerful, fast, 1-MA LTD stage developed to date. In addition, the LTD cavity electrical performance and experimental results are discussed and compared with numerical circuit code calculations. Some peculiarities related to the behavior of the ferromagnetic core, depending on the premagnetizing methods, are also presented and explained in detail. In Sec. III we present the design and test results of the five-stage 1-MA LTD module driving both resistive and electron-beam diode loads in the LPT mode.

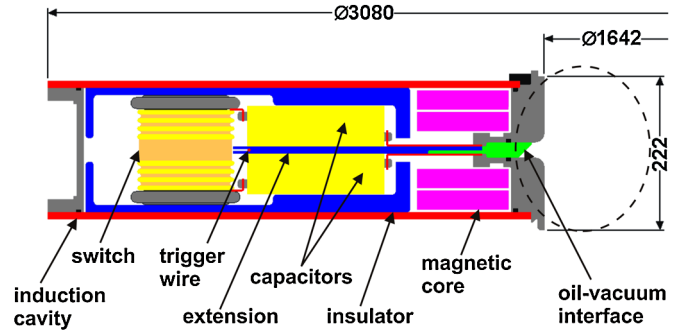


FIG. 1. (Color) Design of the 1-MA LTD stage showing two storage capacitors, the switch and the buses of the brick. Broken ellipse indicates the region of the load location and is presented in more detail in Fig. 2.

II. FAST 1-MA LTD STAGE

The design of the 1-MA fast LTD stage is shown in Fig. 1. The stage induction cavity is a pillbox-shaped toroid with an azimuthal gap at the center of the inside cylindrical surface. This gap is fitted with a vacuum tight oil-vacuum interface. Inside the cavity is located the capacitor bank with the switches, charge and trigger resistors, and the ferromagnetic core. The outside diameter of the stage is $\sim 3 \text{ m}$, the length along the main axis $\sim 22 \text{ cm}$, and the weight filled with oil $\sim 2.5 \text{ tons}$.

The capacitor bank is made of 80 storage capacitors type GA 35426 (40 nF, 100 kV) [16] that are arranged in 40 pairs. The capacitors in each pair are charged in opposite polarity up to $\pm 100 \text{ kV}$ and switched into the load by closing the multispark gap switch type fast LTD [17]. The set of two capacitors, the switch, and the buses connecting the capacitors from one side with the switch and from the opposite side with the azimuthal gap is called brick and represents the basic element of the stage. All the bricks in the stage are connected in parallel and located evenly in a circular array around the axis. For safety reasons, the neighboring bricks are separated by $\sim 1 \text{ k}\Omega$ charging resistors both in the positive and negative charging circuits.

The triggerable switches type fast LTD operate with dry air at a pressure of $\sim 4 \text{ ata}$ (or 0.405 MPa) for $\pm 100 \text{ kV}$ charging voltage. The DC voltage is distributed between several switch gaps with a corona discharge. Some features of these switches are described elsewhere [18–20]. They are triggered by $\sim -100 \text{ kV}$, $\sim 30 \text{ ns}$ rise time pulses which enter into the stage via four 65-Ohms high-voltage cables. Inside the stage, these cables are connected to a 4-mm diameter circular trigger wire located in a groove at the outer diameter of the insulator extension of the oil-vacuum interface. The trigger electrodes of the switches are connected to this wire through $\sim 500 \text{ Ohm}$ resistors.

In the tests of the single stage described below, the $\sim 2\text{-m}$ outer diameter ferromagnetic core had four separate rings, each ring being wound with a 80- μ -thick, 18-mm-

wide ET3524 anisotropic iron tape sandwiched in a 12- μ -thick, 22-mm-wide Mylar film insulation. The rings are molded into an epoxy compound to stabilize the turns and isolate the rings from each other. The magnetic induction at saturation of ET3425 iron is $B_S = 2$ T at $H = 30$ kA/m, the residual induction is $B_R = 1.2$ T, the coercive force is $H_C = 0.03$ kA/m, and the specific resistance of the ET3425 iron is $\rho = 5 \times 10^{-7}$ Ohm m. The total cross section of the iron in each ring is ~ 14 cm². The volt-second integral of the entire core is $VS_C^A \sim 22.4$ mVs with active premagnetizing ($\Delta B = 4$ T) and $VS_C^P \sim 18$ mVs with passive premagnetizing ($\Delta B = 3.2$ T), where ΔB is the total variation of the induced magnetic field in the cores. The performance of the core depending on the premagnetizing methods is discussed in Appendix A.

The high-voltage components inside the cavity are insulated from the walls of the cavity and from each other with dielectric polyethylene insulators (please see Fig. 1). The 1-cm-thick extension of the oil-vacuum interface isolates the capacitors and planar output lines (buses) of the bricks. The oil-vacuum interface is made from extruded acrylic. After assembly the induction cavity is filled with transformer oil for additional electrical isolation of the components.

For the experimental tests of each individual 1-MA LTD stage, the resistive load was placed inside the cylindrical opening of the stage as shown in Fig. 2. Two concentric plastic polyethylene cylinders were inserted separating the stage's inner cylindrical cavity into 2 sections. These sections were hermitically sealed up and down with two metallic conducting plates attached to the outer planar walls of the stage. 20 plastic rods were utilized to compress the "O" rings and establish electrical contact between the plates and the walls of the stage. The first of those two

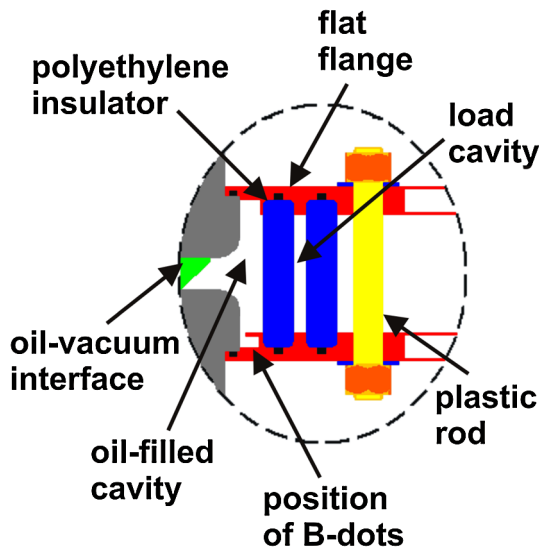


FIG. 2. (Color) Design of the load in tests of separate stage.

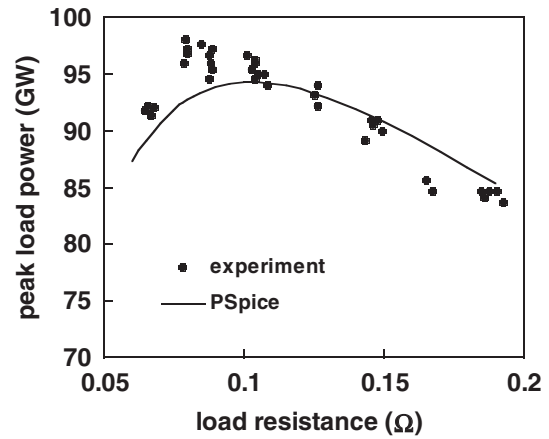


FIG. 3. Peak load power dependence on the load resistance. The dots are the experimental results and are compared with PSPICE simulation (solid curve).

sections, which is closest to the oil-vacuum interface, was filled with oil to avoid flashing along the interface surface. The second cavity between the two cylindrical insulators was filled with NaCl-water solution and served as the resistive load of the stage. The inductance of such load, estimated from its geometry, was 1.05 nH.

In these tests, the load current, I , was measured with two magnetic flux monitors (dB/dt) wound in opposite directions to produce opposite-polarity signals for electrical noise rejection and placed in the vicinity of the load. The load voltage U was measured with an external voltage divider, and the current around the core I_C was measured with another magnetic flux monitor (dB/dt). The resistance of the load defined as $R = U/I$ was varied from ~ 0.06 to ~ 0.19 Ohm by changing the concentration of the NaCl solution. The core was premagnetized before the shot (passive premagnetizing, see Appendix A) by using the premagnetizing pulse generator (PPG). The PPG is essentially an LC circuit with an inductance $L = 20$ μ H and capacitance $C = 40$ μ F. It was charged to 2 kV. A diode was connected in parallel to the capacitor in order to eliminate oscillations of the PPG voltage across the core.

Experiments were conducted with different resistive loads at ± 100 kV charging of the LTD capacitors. The obtained experimental results are summarized in Figs. 3–6 and are compared with PSPICE¹ [21] simulations. Figure 3 indicates that the optimum output stage impedance [15], which maximizes the output power to ~ 96 GW, is $R \sim 0.1$ Ohm. In this case, the load voltage (Fig. 4) is ~ 100 kV and the power rise time (Fig. 5) is ~ 90 ns. The simulation is in a reasonable agreement with experimental results; the only noticeable difference is the faster decrease of the energy delivered to the load for $R > 0.1$ Ohm as compared with the simulation prediction (Fig. 6). The energy is calculated according to equation

¹PSPICE is a registered trademark of MicroSim Corporation.

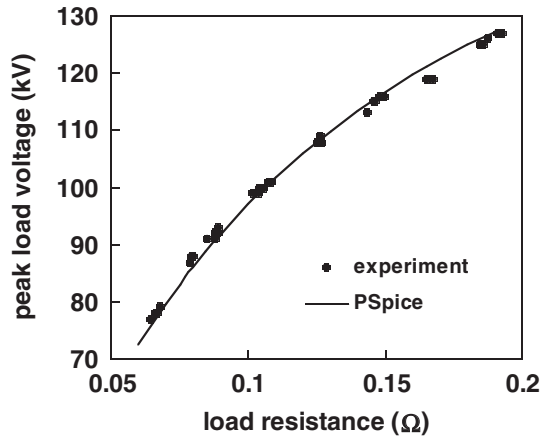


FIG. 4. Peak load voltage dependence on the load resistance. The dots are the experimental results while the solid curve is the PSPICE simulation.

$$E = \int_0^{t_0} UI dt, \quad (2)$$

where t_0 is the time when the load voltage crosses zero for the first time. The experimentally observed energy E has a maximum of ~ 11.3 kJ occurring for a load resistance $R \sim 0.1$ Ohm and is equal to $\sim 70\%$ of the total stored energy in the capacitors. In PSPICE, the energy E also peaks close to $R \sim 0.1$ Ohm, but for larger load resistances does not decrease as fast as in the experiments. The cause of this difference will be discussed below.

Figure 7 shows the recorded load voltage U and the current I_C leaking around the core to the cavity walls for $R = 0.107$ Ohm. At such load the volt-second integral VS_{LTD} , calculated as

$$VS_{LTD} \sim \int_0^t U dt, \quad (3)$$

does not reach the limit $VS_C^P = 18$ mVs (please see Fig. 13

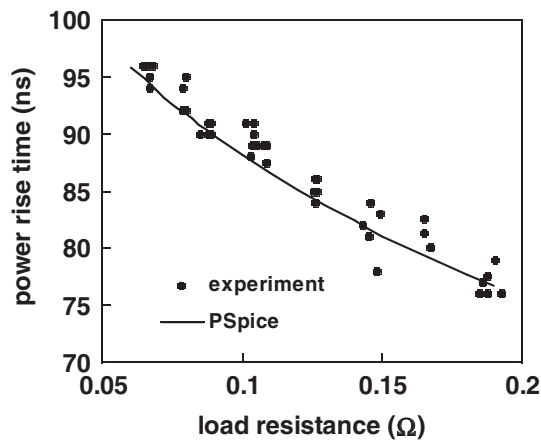


FIG. 5. Power rise time dependence on the load resistance. The experimental data points are compared with the PSPICE numerical simulation (solid curve).

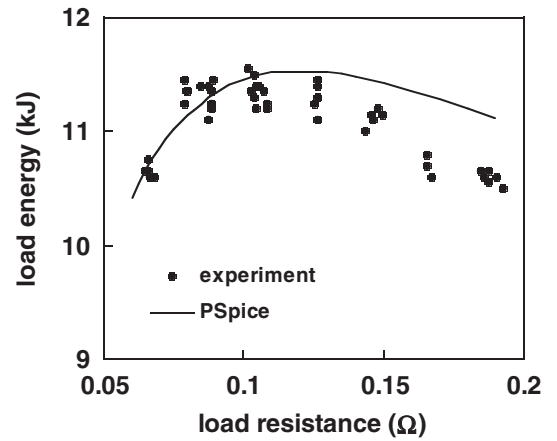


FIG. 6. Energy delivered to the load during the main pulse as a function of the load resistance. The experimental results (dots) are compared with the PSPICE simulation (solid curve).

of Appendix A). The shape of the current I_C is approximately the same as that of the voltage, indicating that the core in this shot behaved as a constant resistance $R_C = U/I_C$. For a measured load voltage $U \sim 100$ kV and $I_C \sim 180$ kA, the value of this resistance is estimated to be $R_C \sim 0.56$ Ohm.

Figure 8 presents similar traces as in Fig. 7, but now the results are obtained with an $R \sim 0.188$ Ohm. In this case the observed load voltage is higher and VS_{LTD} exceeds $VS_C^P = 18$ mVs after ~ 200 ns. At that time, the current I_C begins to rise again, confirming the saturation of the core. In spite of the higher load resistance, the voltage reversal here is larger than that of Fig. 7 because the inductance of the loop around the core, connected in parallel to the load, becomes very small and acts practically as a short.

The performance of the core depending on the premagnetizing methods was studied at $R = 0.166$ Ohm (Fig. 9). With this load and passive premagnetizing the core satu-

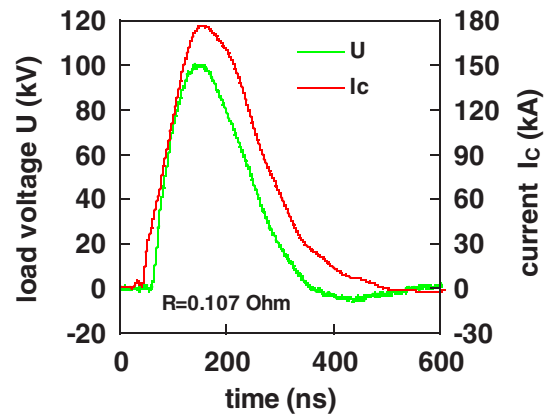


FIG. 7. (Color) Load voltage U and current around the core I_C at $R = 0.107$ Ohm. The volt-second integral VS_{LTD} does not reach the maximum of $VS_C^P = 18$ mVs. The current I_C is approximately proportional to the voltage U .

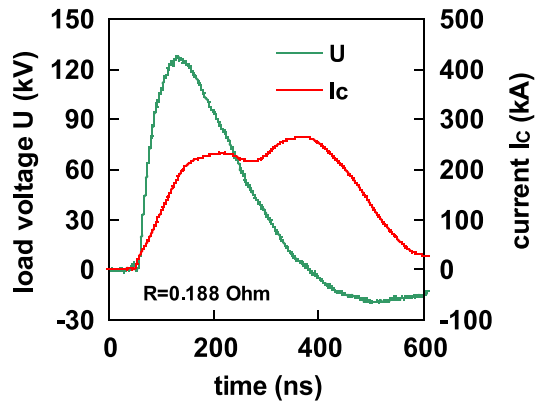


FIG. 8. (Color) Same traces as in Fig. 7 but with a different $R = 0.188$ Ohm. Because of higher voltage U the volt-second integral VS_U exceeds the limit $VS_C^P = 18$ mVs at ~ 200 ns in the pulse. At that time the current I_C begins to rise again, indicating saturation of the core.

rates at ~ 200 ns when VS_{LTD} reaches $VS_C^P = 18$ mVs. The energy loss in the core is ~ 3.6 kJ. At active premagnetizing the volt-second integral VS_{LTD} reaches again the value of 18 mVs at the same time, but now it does not reach the maximum available value of $VS_C^A = 22.4$ mVs. In this case, since the core does not saturate the energy losses are smaller and equal to 3.3 kJ, a decrease of 300 J. When the core is saturated from the very beginning, the current around the core is similar to the current through an inductor (e.g. it peaks at approximately the same time as the voltage crosses zero). The current exceeds 800 kA, the load voltage amplitude decreases by $\sim 10\%$, the total length of the pulse

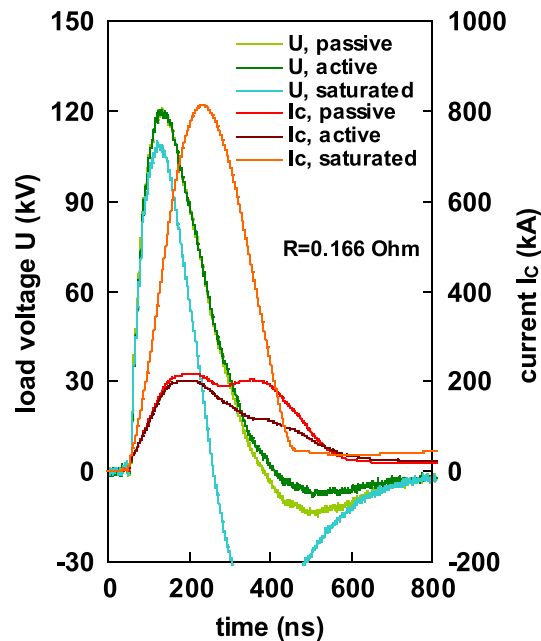


FIG. 9. (Color) Load voltage U and current around the core I_C at $R = 0.166$ Ohm depending on the premagnetizing method.

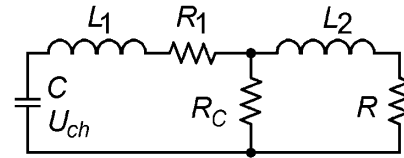


FIG. 10. Equivalent electrical circuit of a fast LTD stage.

decreases from ~ 350 ns to ~ 200 ns, and the energy loss by the time the voltage crosses zero increases to almost ~ 6 kJ.

Assuming that all switches close simultaneously and the cores do not saturate, the discharge of an LTD stage can be represented by a simple equivalent RLC (resistor R , inductor L , and capacitor C) circuit (Fig. 10). Here C is the total storage capacitance of all the bricks connected in parallel; R_1 is the resistance of the capacitors and the switches, L_1 is the total inductance of the bricks, and L_2 and R are the inductance and the resistance of the load.

The resistance R_C simulates the LTD core before it saturates. For slow pulses, the core behaves as a variable inductor L_μ , which is proportional to magnetic permeability of the core material $\mu = dB/dH$. In this case the circuit in Fig. 10 should include L_μ in parallel to the load instead of the R_C . The energy loss in the core would be defined by the surface area inside the static hysteresis loop $B = f(H)$. The volume of the 1-MA LTD core is $W \sim 0.036$ m³, then for the parameters of the ET3425 iron, the energy loss in L_μ at maximum possible $\Delta B = 2B_S$ is $E \sim W(2H_C) \times (2B_S) < 20$ J. (Please see Fig. 13)

If the voltage pulse applied to the conductive core is fast enough, it generates eddy current in the core material. The value of this current is defined by the driving voltage and the resistance of the layer which carries eddy current, R_C . However, to be precise even for the fast pulses, the circuit of Fig. 10 should include L_μ in parallel with the resistance R_C . Generally speaking, the resistance R_C is also variable since it reflects the dynamics of eddy current penetration into the core iron. Though the physics of this penetration is clearly the same as that of the skin depth, the exact expression of R_C for the given shape of the voltage pulse is rather complicated. For engineering purposes, the resistance R_C can be calculated assuming [as in Ref. [22]] that the static hysteresis curve and the voltage pulse are rectangular or [as in Ref. [23]] that dB/dt is approximately constant everywhere throughout the tape. Both approaches result in a constant value given by

$$R_C = k \frac{\rho S}{\delta^2 \ell}, \quad (4)$$

where ρ is the specific resistance of the core iron, S the total cross section of the iron in the core, ℓ the length of the core, and δ the thickness of the iron tape. The dimensionless coefficient k is found to be 8 in [22], and to be 12 in [23]. The dominant branch among L_μ and R_C can be

evaluated by comparing the total current $I_C(t)$ flowing around the core with the voltage across the load $U(t)$ (which is approximately the same as the voltage across L_μ and R_C). As discussed above, the traces in Fig. 9 indicate that if the core is not saturated the current $I_C(t)$ is almost proportional to the voltage $U(t)$, i.e., in the unsaturated core the resistance R_C (~ 0.56 Ohm) dominates. This value is rather close to $R_C \sim 0.7$ Ohm calculated from the Eq. (4) with $\delta = 80 \mu$, $S = 56 \text{ cm}^3$, $\rho = 5 \times 10^{-7}$ Ohm m, $\ell = 6$ m, and $k \sim 10$. For a sinusoidal voltage pulse with the peak amplitude of ~ 100 kV, the energy loss during the first quarter period $T/2$ (~ 350 ns) in a core resistance $R_C \sim 0.6\text{--}0.7$ Ohm is 2.5–3 kJ, which is much higher than the maximum possible energy loss in L_μ (< 20 J). Therefore the inductance L_μ in the circuit of Fig. 10 is neglected. (Note that when the core saturates, the value of μ drastically decreases and the circuit should include the greatly reduced L_μ rather than the R_C . (See the voltage and current traces for the saturated core case of Fig. 9). The best fits of the experimental data with the PSPICE code simulations are presented in Figs. 3–6. They were obtained using the circuit of Fig. 10 with $U_{\text{CH}} = 200$ kV, $C = 800$ nF, $R_1 = 0.0165$ Ohm, $R_C = 0.65$ Ohm, $L_1 = 6$ nH, and $L_2 = 1.05$ nH. These values are the total equivalent capacitance, inductance, and resistance of all of the 40 bricks of the 1-MA LTD stage. Here the inductance and resistance of the brick is assumed to be 240 nH and 0.66 Ohm, respectively. Since the simulated curves in Figs. 3–5 are quite close to the experimental data, we can conclude that the jitter of the 40 switches is at least much less than the rise time of the output pulse.

The difference between the simulated and observed energy delivered to the load for $R > 0.1$ Ohm (Fig. 6) seems to be the result of saturation of the core, which is not taken into account by the simple RLC circuit of Fig. 10. For example, at $R = 0.166$ Ohm (Fig. 9) the saturation of the core at passive premagnetizing increases the energy loss in the core by ~ 0.3 kJ. If this increase is subtracted from the simulated energy $E = 11.3$ kJ of Fig. 6, the energy delivered to the load becomes $E \sim 11$ kJ, which is much closer to what was measured in the experiment.

Note that, for the circuit in Fig. 10, the optimum load impedance providing the maximum output power can be calculated from the expression:

$$R_{\text{opt}} = R^* \left[1 - 0.73 \left(1 - 0.66 \frac{L_2}{L_1} \right) \frac{R^*}{R_C} \right], \quad (5)$$

where

$$R^* = 1.1 \sqrt{\frac{L_1 + L_2}{C}} + 0.8 R_1 \quad (6)$$

is the optimum load impedance for the case $R_C \rightarrow \infty$ [15]. Equation (5) is correct to within $\sim 1\%$ whenever

$\frac{R_1}{\sqrt{(L_1 + L_2)/C}} < 0.5$, $\frac{R_{\text{opt}}}{R_C} \leq 0.2$, and $\frac{L_2}{L_1} \leq 0.3$. A derivation of this expression is given in Appendix B.

The experimental results presented above were obtained with the first prototype 1-MA LTD stage. The loss current around the core when the stage operates at almost peak power is ~ 180 kA, which is $\sim 19\%$ of the load current $I = U/R \sim 935$ kA (see Fig. 8). In order to reduce these energy losses, the additional four 1-MA LTD stages utilized in the present work were built with finer lamination and larger cross section cores. Namely, the cores were fabricated with 50- μ -thick tape, and the iron cross section was increased from $\sim 56 \text{ cm}^2$ to $\sim 64 \text{ cm}^2$. According to expression (4), such changes would increase the resistance R_C from ~ 0.7 Ohm to ~ 2 Ohm [24]. The measured resistance R_C of such cores was ~ 1.5 Ohms. Other possible ways to improve the efficiency of the stage is to fabricate the core from Metglas, which is more expensive but has a resistivity ~ 2.5 times higher than ET3425 iron and/or use finer lamination core tape.

III. FIVE-STAGE 1-MA LTD MODULE

Five 1-MA LTD stages were assembled in series into a module and tested with resistive and electron-beam diode (e-beam diode) loads [25]. In both experiments all the stages were triggered simultaneously, so the LTD module was operated in a LPT mode.

The design of the module with the electron-beam diode load is shown in Fig. 11. The straight cathode stalk has a 757.5-mm radius and is cantilevered. The left side is mounted on the ground flange of the module, while the right freestanding end holds the ring-shaped planar cathode electrode of the diode.

The radial anode-cathode gap around the cathode stalk is 63.5 mm. The peak electric field on the cathode stalk at ~ 400 kV is ~ 65 kV/cm, which is well below the vacuum emission threshold of ~ 200 kV/cm. So the coaxial output vacuum line formed by the five-stage LTD module and the central cathode stalk was designed to operate in the vacuum insulated regime and not in a magnetic insulated transmission line (MITL) regime. The geometric inductance of the coaxial line is ~ 18 nH.

The planar vacuum e-beam diode has a cathode surface area of $\sim 2900 \text{ cm}^2$ and an anode-cathode (A-K) gap of 1–2 cm. The A-K is varied by changing the length of the small cylinders which support the annular anode plate. The front surface of the cathode electrode is covered with velvet cloth to facilitate electron emission since the electric field at the cathode was quite low. The diagnostics include two sets of magnetic flux monitors (dB/dt), B1 and B2. The two B1 probes (wound in opposite directions relative to each other) are located on the left grounded flange of the module vacuum chamber and when integrated give the total current I_{CS} flowing through the module from the left ground flange to the anode right flange. If there are

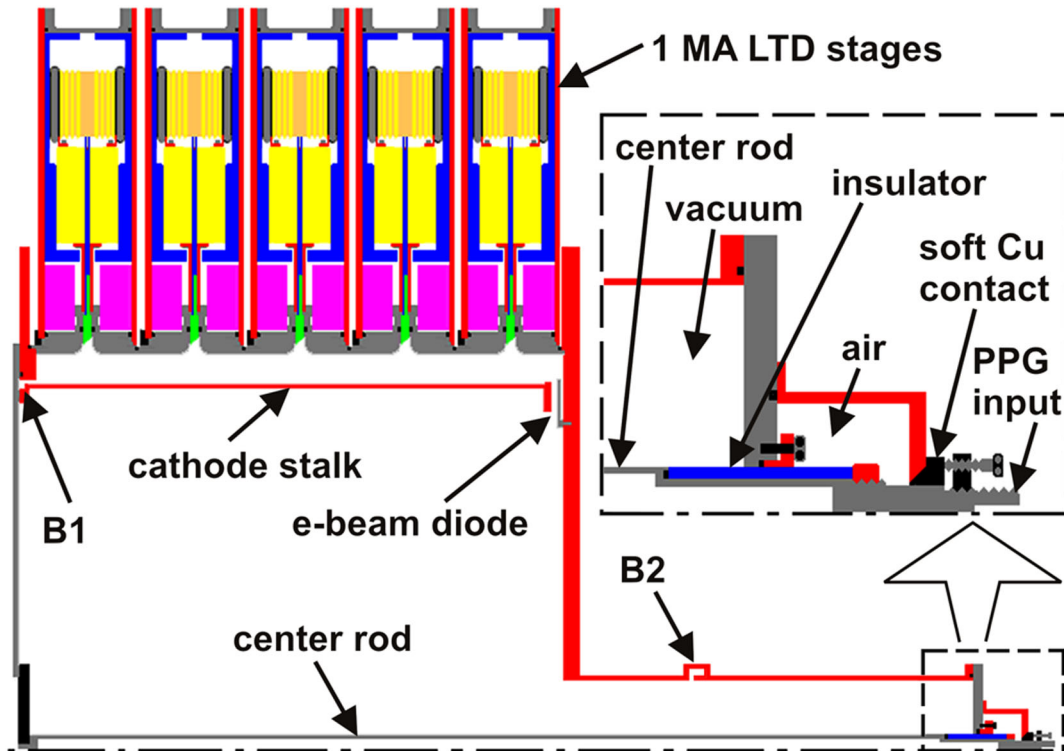


FIG. 11. (Color) Design of the five-stage LTD module with e-beam diode load. The cores of the stages were premagnetized before each shot without opening the module to the atmosphere; the PPG pulse was applied to the right end of the center rod that was disconnected from the grounded body of the module by removing the soft Cu contact.

no current leaks from the cathode stalk, this current is the sum of the diode current I_D and the current flowing through the center rod I_{CR} which shunts the diode with an inductance of ~ 1085 nH. The signals of the two B2 probes (also wound in opposite directions) when integrated provide the current I_{CR} and the diode current $I_D = I_{CS} - I_{CR}$ and, when multiplied with the rod inductance, give the diode voltage $U_D = L(dI_{CR}/dt)$.

The center rod serves two purposes: it allows measuring the diode voltage when connected to the right side anode flange, and it also allows premagnetizing the module cores when connected to the premagnetizing power supply (PPG). The design provides the capability to disconnect it between shots from the grounded body of the module for passive premagnetizing of the LTD cores without opening the module chamber to the atmosphere (please see blowup inset in Fig. 11).

The overall design of the five-stage LTD module with the resistive load was the same as in Fig. 11. However, the cathode stalk and the cathode and anode rings were replaced now by a resistive load assembly consisting of 30 separate resistors made from 4.4-cm diameter, 36-cm long polyethylene tubes filled with KBr water solution. The resistors were mounted at the ends of 3-cm diameter, 67-cm long aluminum rods arranged evenly in a cylindrical array surrounding the axis of the module at a radius of 76.5 cm. Current shunts in series with the resistors were

used to measure the current flowing in the KBr resistors and the voltage across the load. The entire inner volume of the module containing the KBr resistors assembly was filled with SF_6 at atmospheric pressure. Below we present experimental results and numerical simulations for the diode load experiments only.

Figure 12 shows the diode voltage U_D (in green) and current I_D (in blue) traces for five-stage LTD assembly charged to $U_{CH} = \pm 90$ kV and a diode A-K gap of 1.4 cm. In black and red are the diode voltage and current traces simulated with PSPICE for the same charging and diode parameters. The voltage reaches the maximum value of ~ 400 kV at ~ 100 ns. At the same time the current peaks at ~ 800 kA, while the electron-beam power becomes ~ 320 GW.

Since all the stages were triggered simultaneously, the module was simulated in PSPICE as a linear pulsed transformer (LPT). The utilized PSPICE equivalent circuit was composed of five RLC circuits connected in series to the diode load through the 18-nH inductance of the transformer output line. The center rod was connected in parallel to the diode, which according to the geometry of Fig. 11 was simulated as two transmission lines connected in series; the first had a 204 Ohm impedance and 3.86 ns transmission time length and the second had 100 Ohm impedance and 2.96 ns length, which give a total equivalent inductance of ~ 1085 nH. One of the five RLC circuits was

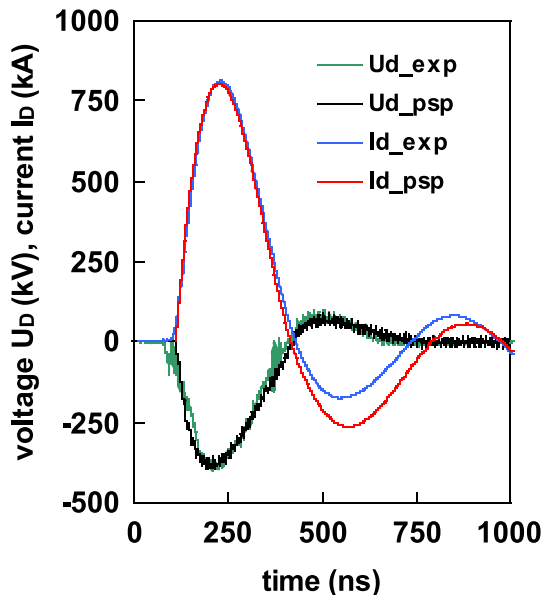


FIG. 12. (Color) Experimental results and PSPICE simulations. The diode voltage U_D for clarity of presentation is inverted (negative). The simulations were done for $U_{CH} = \pm 90$ kV and an emitting cathode area $A = 2100$ cm². The cathode emitting surface was assumed to be moving towards the anode at a constant velocity $V = 2 \times 10^6$ cm/s, simulating the expansion of the cathode plasma.

exactly the same as that presented in Fig. 10 with $R_C = 0.65$ Ohm. The other four circuits have a core resistance $R_C \sim 2.9$ times larger and equal to 1.9 Ohm because the remaining four stages have been built with finer lamination cores of 50- μ -thick iron tape and increased ~ 64 -cm² cross section.

The diode was simulated as a nonrelativistic planar diode with space charge limited electron emission, where the current is defined by

$$I_D = P(U_D)^{3/2} \quad \text{where } P = 2.335 \times 10^{-6} \frac{A}{d(t)^2}. \quad (7)$$

Here A is the cathode emitting area. The A-K gap $d(t)$ was assumed decreasing with time according to the expression

$$d(t) = d_0 - Vt \quad (8)$$

due to cathode plasma expansion at a constant velocity $V = 2 \times 10^6$ cm/s. The initial gap was assumed 1.4 cm. It was allowed to decrease to 0.02 cm and then was kept constant. To fit the experimental data during the main pulse, the cathode emitting area was assumed to be $A = 2100$ cm², which is $\sim 70\%$ of the geometrical surface area of the cathode.

In the tests with the e-beam diode, the five-stage module was operated at charge voltage between ± 80 to ± 90 kV and a number of AK gap settings varying from 1.0 to 1.7 cm. During the resistive load experiments we fired a total of 500 shots; 300 of them were at ± 100 kV charging.

IV. CONCLUSION

In the present work we have shown that fast LTD stages can be built with as many as 40 separate bricks. The optimum load resistance of this stage is ~ 0.1 Ohm. The power pulse delivered to such a load has a ~ 100 GW peak value and a rise time of ~ 100 ns. The electrical behavior of the stage can be predicted by using a simple RLC circuit, which confirms that the jitter of the switches is small compared to the rise time of the output pulse. This greatly simplifies the design of various LTD-based accelerators. The stages can be assembled in series into a module and used as a high-voltage, high-power driver for various applications. The most powerful LTD module consisting of five 1-MA LTD stages was tested with resistive and e-beam diode loads in LPT mode. The experimental results are in excellent agreement with numerical simulations. Experiments with a 1 TW module, which includes 10, 1-MA LTD stages connected in series, are in preparation at Sandia National Laboratory, Albuquerque, USA. This LTD module will be the first ever IVA built with a transmission line insulated with deionized water. All ten LTD stages were designed and manufactured at the High Current Electronic Institute (HCEI) in Tomsk, Russia, and transferred to Sandia. Results of this work will be presented in future publications.

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APPENDIX A: PREMAGNETIZING OF THE CORE

When the LTD and/or PPG pulse are applied to the single-turn winding of the core, which is made up by the PPG input and the cavity walls, the magnetic induction B in the core iron varies according to Faraday's law,

$$B = \frac{1}{S} \int_0^t U_{\text{LTD}} dt + B_0, \quad \text{or} \quad B = \frac{1}{S} \int_0^t U_{\text{PPG}} dt + B_0, \quad (A1)$$

where B_0 is the initial induction at $t = 0$, S is the cross section of iron in the core, U_{LTD} and U_{PPG} are the LTD and PPG voltage pulses, respectively. The units of the parameters are in the SI system. If, for example, we assume that the LTD pulse is positive so that it moves the induction along the hysteresis curve in the $+B_S$ direction (please see Fig. 13), the PPG pulse (at either passive or active premagnetizing) must be negative to move the induction back

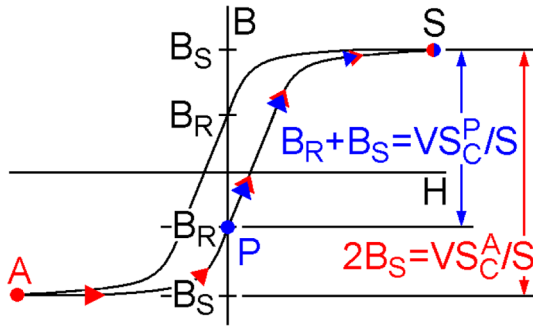


FIG. 13. (Color) Variation of the core induction depending on the LTD firing time relative to the premagnetizing pulse. Blue arrows describe the core behavior if the LTD stage is fired later than the end of the PPG pulse (passive premagnetizing), while the red arrows present the case where the LTD is fired at peak PPG current (active premagnetizing).

down to negative saturation $-B_S$. The core saturates when the value of B in Eq. (A1) reaches B_S with the LTD pulse and $-B_S$ with the PPG pulse, where $B_S = 2.0$ T is the induction at saturation of ET3425 iron. The difference between the passive and active premagnetizing is the value of the initial induction B_0 at the time the LTD is fired.

At *passive* premagnetizing the LTD pulse is applied after the end of the PPG pulse. In this case the induction reaches $-B_S$ during the PPG pulse and relaxes to $-B_R$ after the end of the pulse. Then for the LTD pulse the initial induction is $B_0 = -B_R$, and the core will not saturate before the volt-second integral VS_{LTD} reaches the limit

$$VS_{LTD} = \int_0^t U_{LTD} dt = S(B_S + B_R) \equiv VS_C^P. \quad (\text{A2})$$

The tested 1-MA LTD stage had a core with $S \sim 56 \times 10^{-4}$ m², $B_S = 2$ T, and $B_R = 1.2$ T. Equation (A2) then gives $VS_C^P \sim 18$ mVs. Passive premagnetizing is the standard method used in modern IVAs.

The induction at saturation B_S ($= 2.0$ T) of the ET3425 iron is sufficiently higher than the residual induction B_R ($= 1.2$ T). This allows an increase of the volt-second integral VS_{LTD} to a higher than $VS_C^P \sim 18$ mVs value if active premagnetizing is used. At *active* premagnetizing, the LTD is triggered at the time when the PPG voltage pulse saturates the core in opposite polarity. At that time the PPG *current* reaches maximum. For the LTD pulse the initial induction then is $B_0 \sim -B_S$, and the core does not saturate before the volt-second integral VS_{LTD} reaches the maximum value of

$$VS_{LTD} = \int_0^t U_{LTD} dt = S(B_S + B_S) \equiv VS_C^A, \quad (\text{A3})$$

which is ~ 22.4 mVs for the core of the tested 1-MA LTD stage. Active premagnetizing is used in IVAs utilizing Blumlein as a source driving individual cavities [3].

The variation of the induction in the core iron during the LTD pulse, depending on the premagnetizing method, is

schematically illustrated in Fig. 13. The blue arrows indicate the path from point P to point S followed by the magnetic induction of the core during the LTD pulse when the LTD is triggered after the PPG pulse (passive premagnetizing). The red arrows indicate the path from point A to point S taken by the core during the LTD pulse when the LTD is triggered at peak PPG current. At that time the induction of the core is at $B_0 \sim -B_S$ (active premagnetizing).

APPENDIX B: OPTIMUM LOAD IMPEDANCE OF AN LTD STAGE

Derivation of Eq. (5)

We estimate here the optimum load impedance R_{opt} of the LTD circuit presented in Fig. 10. Reference [15] finds that when $R_C \rightarrow \infty$ and $L_2/L_1 = 0$, the optimum load impedance is given by the following expression:

$$R^* = 1.1 \sqrt{\frac{L_1 + L_2}{C}} + 0.8R_1. \quad (\text{B1})$$

Reference [26] finds that when R_C is finite and $L_2/L_1 = 0$, the optimum load impedance is given by the following:

$$R'_{opt} = R^* \left[1 - 0.73 \frac{R^*}{R_C} \right]. \quad (\text{B2})$$

We estimate here the optimum load impedance R_{opt} when R_C is finite and $L_2/L_1 \neq 0$. We use dimensional analysis to observe that it may be possible to express the ratio R_{opt}/R'_{opt} as a function only of the ratios R'_{opt}/R_C and L_2/L_1 :

$$\frac{R_{opt}}{R'_{opt}} = f\left(\frac{R'_{opt}}{R_C}, \frac{L_2}{L_1}\right). \quad (\text{B3})$$

We calculated R_{opt}/R'_{opt} numerically at several values of R'_{opt}/R_C and L_2/L_1 . We find that to a reasonable approximation

$$R_{opt} = R^* \left[1 - 0.73 \left(1 - 0.66 \frac{L_2}{L_1} \right) \frac{R^*}{R_C} \right]. \quad (\text{B4})$$

When $L_2/L_1 = 0$, Eq. (B4) becomes identical to Eq. (B2), which is developed in Ref. [26]. When $L_2/L_1 = 0$ and $R'_{opt}/R_C = 0$, Eq. (B4) becomes identical to Eq. (B1), which is developed in Ref. [15]. Equation (B4) is correct to $\sim 1\%$ whenever

$$\frac{R_1}{\sqrt{(L_1 + L_2)/C}} < 0.5, \quad (\text{B5})$$

$$\frac{R^*}{R_C} \leq 0.2, \quad (\text{B6})$$

$$\frac{L_2}{L_1} \leq 0.3. \quad (\text{B7})$$

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