High current, 0.5-MA, fast, 100-ns, linear transformer driver experiments

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The linear transformer driver (LTD) is a new method for constructing high current, high-voltage pulsed accelerators. The salient feature of the approach is switching and inductively adding the pulses at low voltage straight out of the capacitors through low inductance transfer and soft iron core isolation. Sandia National Laboratories are actively pursuing the development of a new class of accelerator based on the LTD technology. Presently, the high current LTD experimental research is concentrated on two aspects: first, to study the repetition rate capabilities, reliability, reproducibility of the output pulses, switch prefires, jitter, electrical power and energy efficiency, and lifetime measurements of the cavity active components; second, to study how a multicavity linear array performs in a voltage adder configuration relative to current transmission, energy and power addition, and wall plug to output pulse electrical efficiency. Here we report the repetition rate and lifetime studies performed in the Sandia High Current LTD Laboratory. We first utilized the prototype ~0.4-MA, LTD I cavity which could be reliably operated up to ±90-kV capacitor charging. Later we obtained an improved 0.5-MA, LTD II version that can be operated at ±100 kV maximum charging voltage. The experimental results presented here were obtained with both cavities and pertain to evaluating the maximum achievable repetition rate and LTD cavity performance. The voltage adder experiments with a series of double sized cavities (1 MA, ±100 kV) will be reported in future publications.

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I. INTRODUCTION

Sandia National Laboratories are actively pursuing the development of a new class of accelerators based on the linear transformer driver (LTD) technology [1–3]. LTD based drivers are considered for many applications including future very high current Z-pinch inertial confinement fusion (ICF) drivers like ZX and Z-pinch inertial fusion energy (IFE) drivers.

High currents can be achieved by feeding each core with many capacitors connected in parallel in a circular array. High voltage is obtained by inductively adding many stages in series. Utilizing the capacitors and switches presently available, we can envision building the next generation of fast Z-pinch drivers without the usage of large deionized-water and oil tanks as is the case with the conventional pulsed-power technology drivers. For example, an LTD based replacement of a Saturn accelerator could fit in the space now occupied only by its water tank [4]. The overall Saturn footprint is ~707 m^2 and that of the water tank is only 113 m^3 (~ 16%). The Saturn LTD design is a bit taller (7.5 m in height) than the existing device (5 m in height), and hence the by volume percentage is ~24%. Most importantly, the new design eliminates the need for a tank containing 950 m^3 of oil to house the 36 Marx generators and for another separate tank containing ~190 m^3 of deionized water to house the pulse forming and transmission lines network. In addition to the relative compactness, LTD has a number of very significant advantages compared to the Marx-and-water-line technologies. These drivers do not require insulating dielectric stacks for high-voltage hold-off; the coaxial voltage adders, made of LTDs, and the power transmission lines could be directly connected without interface to the reaction vacuum chamber. The latter assumes that vacuum self-magnetic insulated transmission lines (MITL) transfer the electric power to the load [3–5]. (If the voltage adder and transmission lines utilize deionized water as insulator [6], water to vacuum interface near the load would be necessary). All the switches operate with pressurized air and not with SF6, so there are no asphyxiation hazards. The device is contained within the steel walls of the LTD cavities and is grounded at all times. Hence, the electrical hazard is dramatically reduced. The gas switches are very quiet; therefore there is no mechanical shock to significantly shorten the life of the assembly. Because the entire device is enclosed in stainless steel walls there is also no electromagnetic power (EMP) radiated at the surrounding the device area. However, the most important advantage of all is that the LTD drivers offer the possibility of a reprated operation. They can be multipulsed with a repetition rate, in principle, up to the capacitor specifications, which is of the order of 10 Hz. Of course other system components like switch pressurization and fast purging following

each shot may limit the operating repetition rate to lower frequencies. The relatively high repetition rate capability makes LTD the driver of choice for inertial fusion energy (IFE) where the required repetition rate is estimated to be 0.1 Hz [7–9]. In the following sections we briefly describe the basic circuit theory underlying the LTD operation, describe our fast high current LTD cavities, and give performance results.

In Sec. II we describe the fast high current (~ 0.5 MA) LTD cavity and its operation. In Sec. III we briefly outline the basics of the LTD technology. Section IV contains the results obtained with the first prototype (LTD I) cavity, while in Sec. V the performance of the second LTD II cavity is presented and compared with circuit code simulations.

II. THE 0.5-MA LTD CAVITY

An LTD cavity is basically an induction accelerator cavity that encloses the entire pulse-forming network that generates the output pulse. This pulse is applied across the insulator that separates the anode and cathode output electrodes (A-K gap) of the cavity. The LTD cavities studied here are doughnut shaped. At all times the walls of the cavities are at ground potential. In Fig. 1, one cavity is presented with the top metal cover and plastic insulator that insulates the charged parts from the cavity walls removed. The cavity contains two circular arrays of 40-nF, 25-nH single-ended capacitors. In Fig. 1 only the top array is seen. The bottom array is separated from the top by a ~ 1 cm plastic insulator plate. The top capacitors can be charged up to $+100$-kV maximum charge and the bottom ones up to -100 kV. Each pair of negatively and positively charged capacitors are connected in series with a separate switch positioned vertically and capable of holding 200-kV potential difference ($= 100 - (-100)$). This basic unit, "brick," composed of two capacitors and one switch connected in series, defines the period of the cavity output pulse. The capacitors and switches are the only two active elements, which are repeated many times in a cavity interior depending on the required output current pulse amplitude. Figure 2 shows the actual design side section of a brick with a liquid resistor as a load at its center [10,11], and Fig. 3 is a pictorial representation again of a side section of the cavity where the load is now the coaxial line formed by the inner cylindrical surface of the cavity and the central (cathode) cylindrical electrode (at this representation a pair of double-ended capacitors is assumed).

FIG. 1. (Color) Top view of the prototype LTD I cavity. The top metal cover and plastic insulator which insulates the charged parts from the cavity walls are removed.

When the trigger pulse ($+100$ kV) arrives into the middle plane of the switches, the switches close and the capacitors start to discharge towards the walls of the cavity, which are grounded at all times. However, the ferromagnetic core has the appropriate cross-sectional area to block the pulse from going to ground and forcing it to be applied across the plastic insulator of the A-K gap for a duration of ~ 150 ns. This induces an opposite sign pulse on the cathode electrode, which propagates upstream through the coaxial transmission line. When the core saturates, any remaining energy goes to the ground.

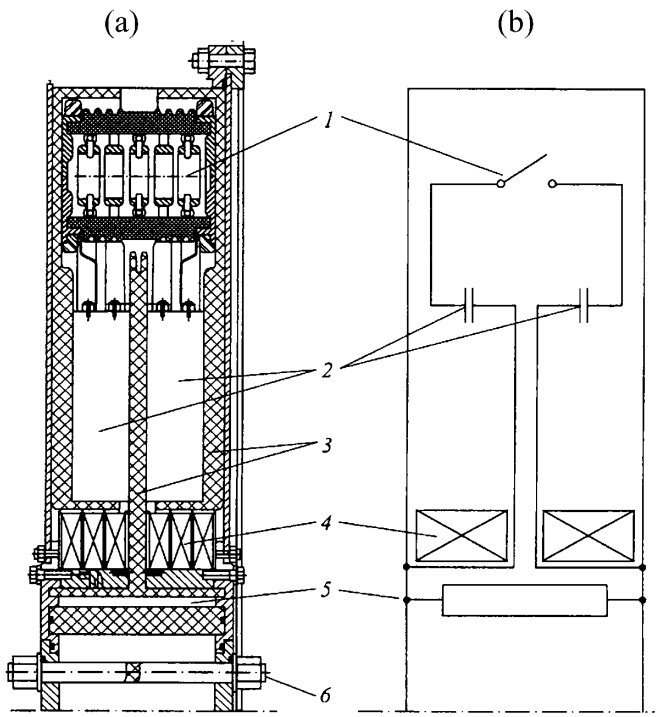

FIG. 2. (a) Side section of a brick with a liquid resistor as a load. This is an actual reduction of the cavity assembly blueprint. (b) Schematic electrical diagram of the brick. The cavity components are: 1—switch; 2—capacitors; 3—plastic insulator plates; 4—ferromagnetic cores; 5—annular KBr liquid resistor load; 6—supporting nylon rod.

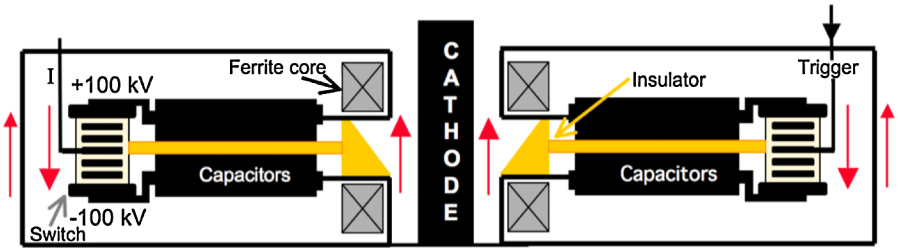

FIG. 3. (Color) Pictorial representation of a side section of the LTD cavity where the load now is the coaxial line formed by the inner cylindrical surface of the cavity and the central (cathode) cylindrical electrode (at this representation double-ended capacitors are assumed). The red arrows show the current direction in each conductor.

In order to achieve a fast, ~70-ns, rise time output pulse with a ~100-ns FWHM, the inductance of the brick must be kept as low as possible. The brick inductance (~ 230 nH) is the sum of the two capacitor inductances (~ 50 nH), the switch inductance (~ 120 nF) and the inductance of the circuit bushes (~ 60). The bushes are thin aluminum plates that connect one capacitor terminal to the switches and the other to the anode or cathode electrode of the A-K gap, completing the circuit loop and bringing the pulse of the brick to the load resistor (in our laboratory cavity case) or to the accelerating A-K gap (voltage adder configuration of Fig. 3). The single-ended capacitors of our LTD I and LTD II cavities make, by necessity, the basic brick circuit a bit longer. For our new 1-MA LTD cavities we have developed in collaboration with General Atomics Electronic Systems double-ended capacitors model # 35426 [12] (Fig. 4). A single-ended capacitor has both terminals at the top of the housing, and since the maximum voltage difference between the two terminals is 100 kV, it requires more plastic insulation and longer housing. A double-ended capacitor has the high-voltage terminal at the top and the ground terminal at the bottom of the plastic housing (similar to the 1.5 V common household batteries). This helped to decrease the length of the basic circuit loop; however, the inductance of the brick remains practically the same since now the capacitors are part of the current loop. In both cases the total measured inductance of the brick up to the ferromagnetic cores is the same and approximately equal to 230 nH. The switches are pressurized with dry refrigerated air. The pressurized refrigerated air, in addition to helping the switches hold the voltage until trigger time, also cools the switch interior during high frequency rep-rated operation. Depending on the capacitor charging voltage, the switch operating pressure can vary between a few atmospheres and up to six atmospheres. The air following each shot is removed fast by connecting the switch chambers with a large vacuum chamber that is continuously pumped down to a 10-torr pressure. This prevents the products of air breaking down from leaving deposits on the plastic inside surface of the cylindrical

FIG. 4. (Color) Double-ended (left) and single-ended capacitors. The arrow indicates the high-voltage terminal. The other is the ground terminal. The single-ended capacitors are 7.5 cm longer in order to insulate the two electrodes that are side by side. In the figure above only the high-voltage terminal of the single-ended capacitor is shown; the other one is hidden by the plastic insulator plate.

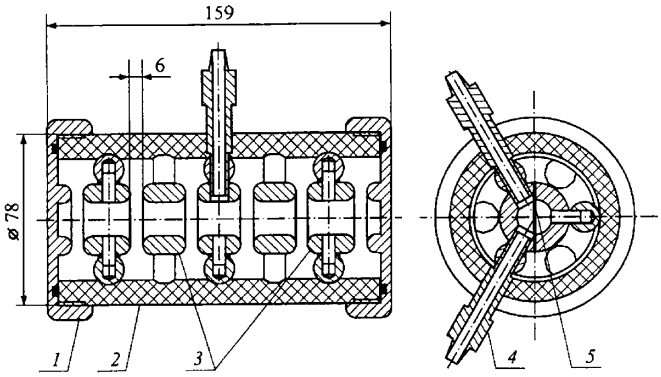

FIG. 5. Schematic diagram of the LTD cavity switch. The operating maximum voltage is ±100 kV and the maximum current 25 kA. The switch components are: 1—cover flange; 2—cylindrical nylon housing; 3—spark gap electrodes; 4—tube for inlet and outlet; 5—rod holder of corona voltage grading needles. The dimensions are in mm. The cross section of the switch is taken through the middle electrode [11].

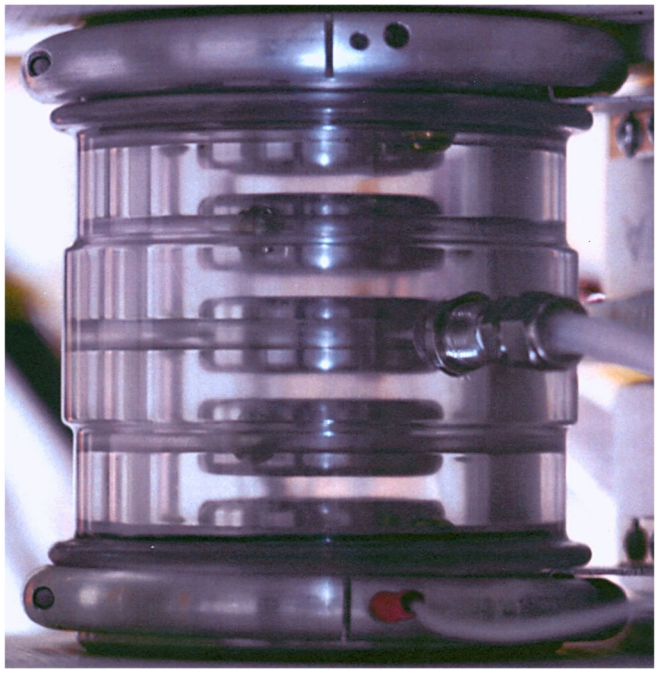

FIG. 6. (Color) Photograph of the LTD cavity switch. The voltage grating electrodes of the switch can be seen as well as one of the gas switch input connected to the center electrode.

switch wall during the arcing and conducting stage of the switch (Figs. 5 and 6) [11,13].

We developed a repetition system that can recycle the switches very fast [14]. Actually the limiting factor in our experiments was not the switches but the capacitor charging power supply software. With a faster communicating power supply with our LAB-VIEW program we could have exceeded the 0.1 Hz repetition rate required for the IFE driver. The switches are relatively small with a diameter of ~8 cm and height of ~16 cm, which together with the plastic insulator plates (of a total thickness of ~5 cm) and the outside flat walls, practically defines the depth of the cavity (~ 22 cm). The overall dimensions of the LTD I cavity are: outer diameter 199 cm, inner diameter 78 cm, and height ~22 cm. The outer diameter of the LTD II cavity is 5 cm larger (~ 204 cm). We can visualize them as large oversized doughnuts with flat top and bottom surfaces.

III. THE LTD PRINCIPLE AND ITS EQUIVALENT CIRCUIT

Figure 7 represents the equivalent simplified circuit of an LTD cavity neglecting the core losses, which in a very finely laminated Metglas core are practically equal to zero. The circuit contains a switch, a capacitor C, an inductance L, and a resistance R. We assume that the switch represents all the parallel-connected switches of the cavity; the capacitor is equal to the sum of the capacitance of all the capacitors; the inductance is equal to the total inductance

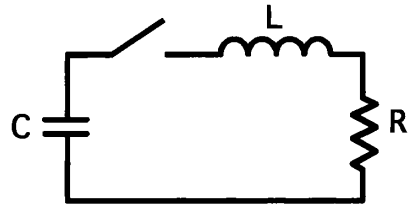

FIG. 7. LTD cavity simplified equivalent circuit. The resistance R is the sum of the load and internal circuit impedance. This circuit neglects the core losses.

including that of the switches, capacitors, and load; and finally the resistance R includes the load plus the internal resistance of the cavity. A more realistic equivalent circuit usually considered in numerical simulations is presented in Fig. 8, where the resistance (R_1) and inductance (L_1) of the LTD cavity are separately included from the respective parameters L_2 and R of the load. In addition, and this is the main and important difference from the circuit of Fig. 7, the core losses are included in the form of a parallel resistor to the load R_c.

The second order differential equation that governs the circuit behavior of Fig. 6 is that of the typical damped oscillation that is given by the familiar expression of Eq. (1):

$$L\frac{d^2i}{d^2t} + R\frac{di}{dt} + i/C = 0. \tag{1}$$

This equation can be solved analytically, and in its general form the solution has a rather cumbersome trigonometric expression for the load voltage, current, power, and energy as a function of time [1]. Numerical solutions are necessary to simplify these expressions. Specifically the load resistance that maximizes the circuit power output has been estimated numerically for both the circuit of Figs. 7 and 8 by the Refs. [6,15], respectively. However, there are two special cases where the solution has simple forms: when $R = \sqrt{\frac{L}{C}}$ and when $R = 2\sqrt{\frac{L}{C}}$. The first is the "matched" case where the load resistance is equal to the characteristic impedance of the circuit, and the second is the critically matched case where the solution does not exhibit any oscillation. In the matched case, the time to peak current and voltage and the values at that particular

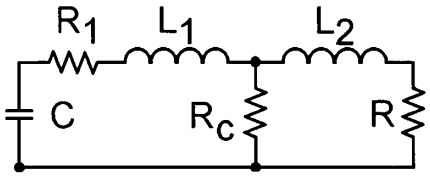

FIG. 8. LTD cavity equivalent circuit including core losses represented with the resistance R_c. Here R_1 and L_1 are the cavity total resistance and inductance and L_2 is the inductance of the load.

time of the voltage, current, and energy transferred to the load are given by the following expressions:

$$t_{\text{peak}} = \frac{2\pi}{\sqrt{3^3}}\sqrt{LC} = 1.21\sqrt{LC}\ \text{(s)} \tag{2}$$

$$i_{\text{peak}} = \frac{2V_0}{\sqrt{3}R}e^{-\pi/(3\sqrt{3})}\sin(\pi/3) = 0.55\frac{V_0}{R}\ \text{(A)} \tag{3}$$

$$V_{\text{peak}} = Ri_{\text{peak}} = 0.55V_0\ \text{(V)} \tag{4}$$

$$E(t_{\text{peak}}) = 0.40E_0\ \text{(J)}, \tag{5}$$

where here V_o and E_0 are, respectively, the initial charge voltage and the total energy stored in the capacitor at $t = 0$. The units utilized are those of the SI system.

In the critically matched case the peak current is smaller by 33% and the energy transferred to the load at peak time by 20%. However, the rise time is shorter and the peak voltage higher:

$$t_{\text{peak}} = \sqrt{LC}\ \text{(s)} \tag{6}$$

$$V_{\text{peak}} = 0.74V_0\ \text{(V)}. \tag{7}$$

From the above arguments and expressions, it is obvious that for certain applications like radiographic machines where the x-ray output is proportional to a higher than quadratic exponent of the electron beam voltage, and where the output current requirements are relatively modest, the critically ($R = 2\sqrt{\frac{L}{C}}$) or higher overmatched load conditions are the choice. Indeed the first radiographic LTD machine currently in operation in Sandia is critically matched to the radiographic diode load [16].

On the other hand, for Z-pinch drivers where large current and efficient energy transfer to the load at peak current are of paramount importance, simply matched loads of $\sqrt{\frac{L}{C}}$ should be the configuration of choice. However, recent current scaling experiments with the Z accelerator [17] demonstrated that faster current rise time driven pinches and shorter implosion times (although with lower peak load current) yielded higher x-ray radiated power. Therefore, it is conceivable that a critically matched design would be appropriate for large Z-pinch drivers in order to provide faster load current rise times despite the lower peak current.

IV. EXPERIMENTS WITH THE PROTOTYPE LTD I CAVITY

The prototype cavity was the first high current LTD cavity device ever built, and it had a specific problem. The peripheral cylindrical walls (Fig. 1) were too close to the switch high-voltage terminals. This prevented us from charging the capacitors to ±100 kV. Therefore the first set of experiments reported here was performed at maximum charging voltage of ±90 kV. In fact, these tests uncovered this minor defect, which was corrected in the newer cavity model LTD II. For the second experimental campaign we obtained the new improved version, LTD II cavity, where the diameter of the cylindrical wall was 5 cm larger. Hence, the data reported in Sec. V refer to this cavity, and all were obtained at the maximum charging voltage of ±100 kV.

The prototype LTD I cavity was constructed at the High Current Electronic Institute in Tomsk, Russia as a single shot device. It was delivered to Sandia and installed at the High Current LTD laboratory pictured in Fig. 9. Following single shot testing, all the support systems such as capacitor charging, switch pressurization, switch vacuum purging, premagnetization of the ferromagnetic cores and triggering systems were modified to facilitate repetitive pulse operation [14,18]. Figure 9 shows a view of the LTD cavity where some of the charging and trigger cables and air hoses connecting to the cavity are visible. A LABVIEW [19] based software program was written to automatically control the above operations including the data acquisition system. We can preset the number of pulses required for every experimental campaign and the interpulse separation, press the computer key, and let the system go on firing and collecting data. In the presently reported experiments the cavity output load was a liquid resistor installed at the center of the cavity (Figs. 1 and 2).

The research with the prototype LTD I cavity had the following goals: (1) Fire a large number of shots and evaluate the longevity of the cavity's active components such as capacitors and switches. (2) Determine the output current and voltage jitter, which measures the pulse-to-pulse variation of starting point as compared to the trigger pulse arrival in the switches. (3) Improve, adjust, and modify the various elements of the automation systems and computer program software so the cavity firing repetition rate could approach as close as possible to the

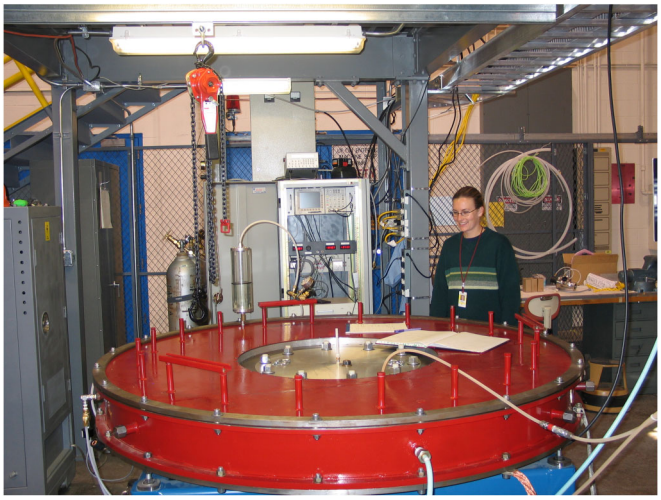

FIG. 9. (Color) The High Current LTD Laboratory.

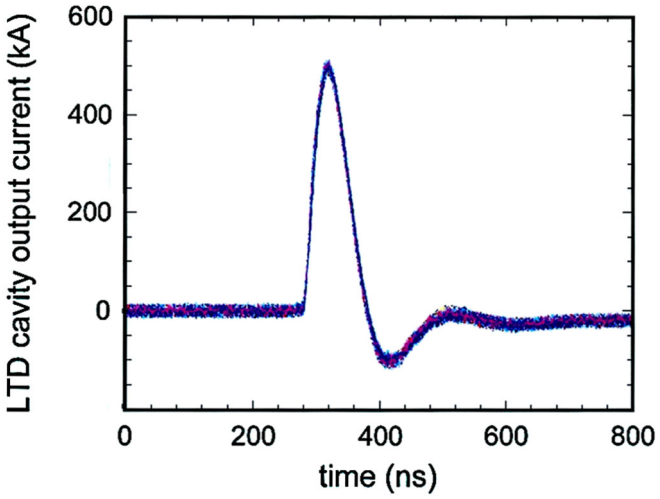

FIG. 10. (Color) 200 shots output pulse current overlay of the prototype LTD I cavity.

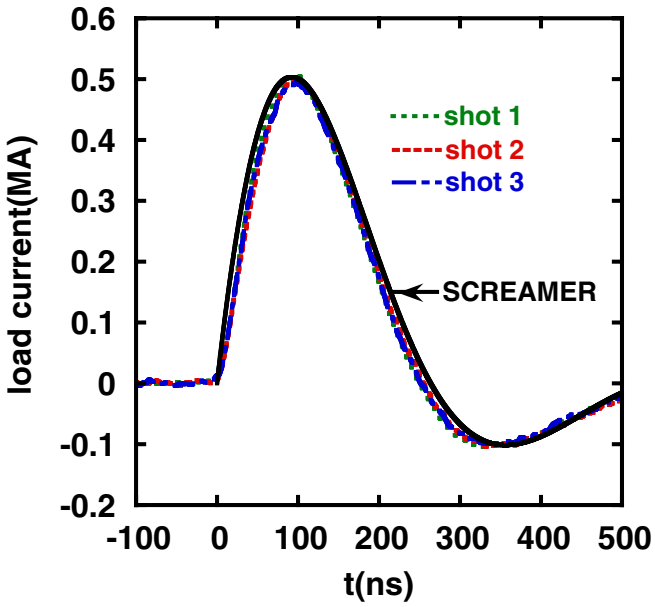

FIG. 11. (Color) Comparison of three output current traces obtained of the prototype LTD I cavity with the SCREAMER circuit code calculations.

required 0.1 Hz frequency of an inertial fusion energy (IFE) power plant. (4) Measure the reproducibility of the voltage and current pulses. (5) Evaluate the number of switch prefires.

Most of the above set goals were successfully completed: (1) We fired 13 000 shots at rep-rate higher than five shots per minute without experiencing any component overheating or problems with the switches, the capacitors, and supporting automated systems. It is interesting to note that the output voltage and current pulses are extremely reproducible as witnessed by a 200-shot overlay (Fig. 10). Parallel with this study, a small circuit setup composed of one switch and two capacitors connected in series (= brick) (similar to one of the 20 parallel circuits enclosed in the LTD cavity) was fired for 37 000 times with a repetition rate of three shots per minute with no switch or capacitor failure. This later study was done in Tomsk HCEI under Sandia contract. It is obvious that the LTD technology is very reliable and is a good candidate for the next generation of large Z-pinch drivers where hundreds of thousands of LTD switches will be utilized and for the IFE driver [20,21] where a very large number of shots will be required. (2) The measured cavity output jitter was quite small. During the 13 000 shots we observed a jitter less than 2 ns (1 sigma), which is much better than the one of the conventional pulsed-power devices. (3) We came very close to the IFE required repetition rate. Towards the end of this campaign we were able to fire every 10.3 seconds, which is equivalent to 0.097 Hz. Installation of a higher current charging power supply could increase the firing frequency up to 0.12 Hz. (4) The pulse-to-pulse reproducibility as witnessed from Fig. 9 is excellent with variation better than 1% (1 sigma). (5) Finally we are happy to report that during the 13 000 shots following the evaluation of the switch optimum operating pressure not one switch prefire was recorded.

Figure 11 compares a sample of the cavity output current traces with the results of the SCREAMER [22] circuit code calculations. The input circuit parameters were $C = 400$ nF, $L = 14$ nH, and $R = 0.170$ Ohm and the capacitor initial charge voltage $V = 166$ kV $= +83 - (-83)$ kV. The value of R was slightly adjusted to reproduce the data. The experimental results are in good agreement with the simulations.

V. EXPERIMENTS WITH THE LTD II CAVITY AT 100-KV CHARGING

The experimental campaign with the LTD II cavity had somewhat different goals. In addition to firing a large number of shots for component longevity verification, the cavity performance for different switch pressures was studied. Namely, the switch pressure was varied from 53 psia (= 366 kPa) to 67 psia (= 463 kPa) in steps of 2 psia ($\sim$ 14 kPa). For each pressure setting 1000 shots were fired at ± 100-kV charging. In order to avoid large temperature variations of the liquid load resistor, the shots were performed at the moderate repetition rate of three shots per minute. Figure 12 compares a typical output voltage trace, at ± 100 kV charging, with PSPICE [23] circuit code calculations. The input circuit parameters were the following: $C = 400$ nF, $L_1 = 12$ nH, $R_1 = 0.033$ Ohm, $R_C = 1.3$ Ohm, $L_2 = 0.7$ nH, and $R = 0.2$ Ohm and the capacitor charge voltage 200 kV $= +100 - (-100)$ kV. Both traces are close to overlapping. Figure 13 shows a self-brake curve obtained by charging all 20 bricks of the cavity.

For the LTD II experimental campaign the LAB-VIEW software was substantially upgraded. For every shot the

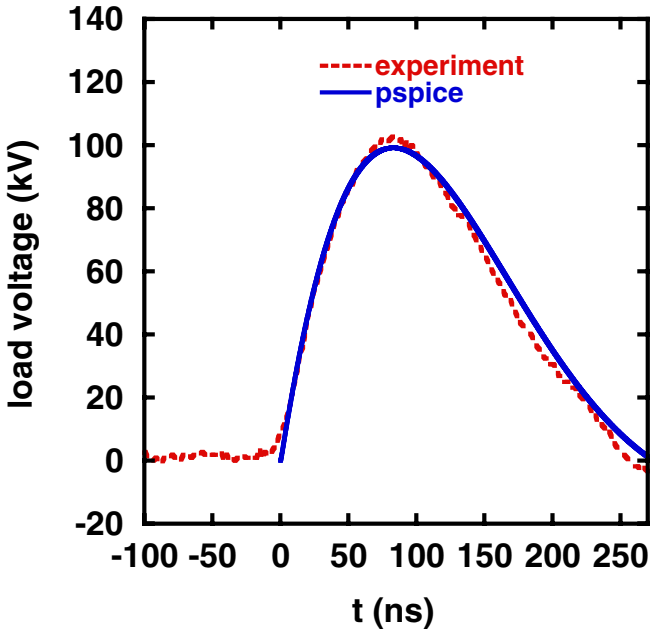

FIG. 12. (Color) Typical load voltage trace compared with a PSPICE [23] circuit code calculated voltage trace.

following voltage pulse output parameters were recorded and statistically analyzed: switch closure time (the time interval between the arrival of the trigger pulse on the switches and the start of the output pulse) (Fig. 14), switch closure jitter (Fig. 15), voltage pulse rise time (Fig. 16), output voltage shape (Fig. 12), fall time (Fig. 17), FWHM (Fig. 18), and amplitude (Fig. 19): similar parameters were recorded for the output current pulses. As the switch pressure increased above 65 psia (= 450 kPa), the trigger jitter, pulse rise time, FWHM, and standard deviations

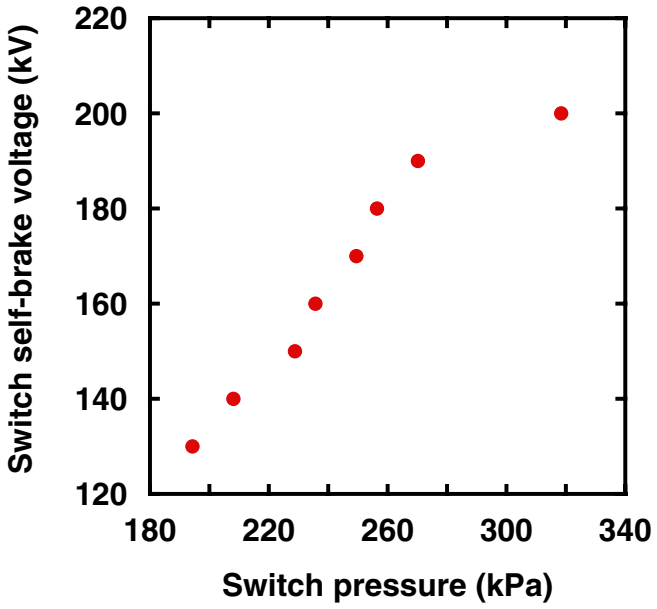

FIG. 13. (Color) Self-break curve of the LTD switches.

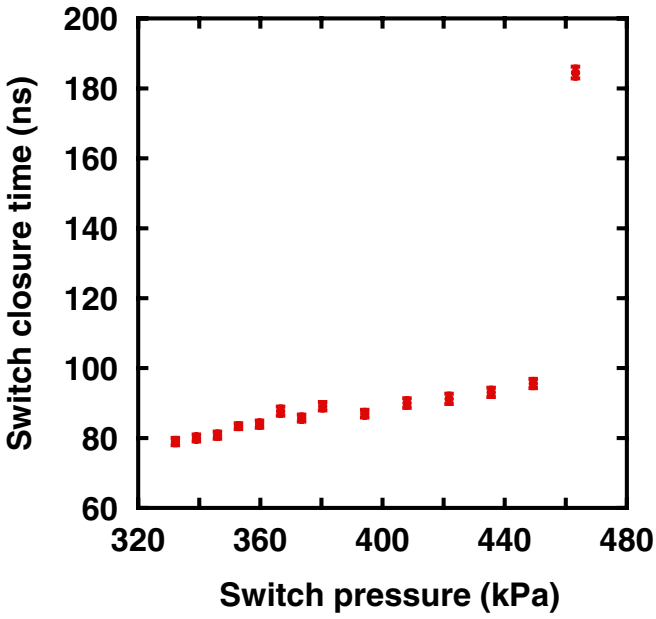

FIG. 14. (Color) Pictorial representation of the switch closure time (the time interval between the arrival of the trigger pulse on the switches and the start of the output pulse) as a function of the switch pressure.

increased. Our data suggest that the switches perform equally well in the 360–450-kPa pressure range for a ±100-kV charging operation. At this pressure range the pulse rise and fall times, FWHM, trigger jitter, and amplitude standard deviations were approximately the same with a very slight increase going from lower to higher pressures. However, as the pressure increased from about 330–

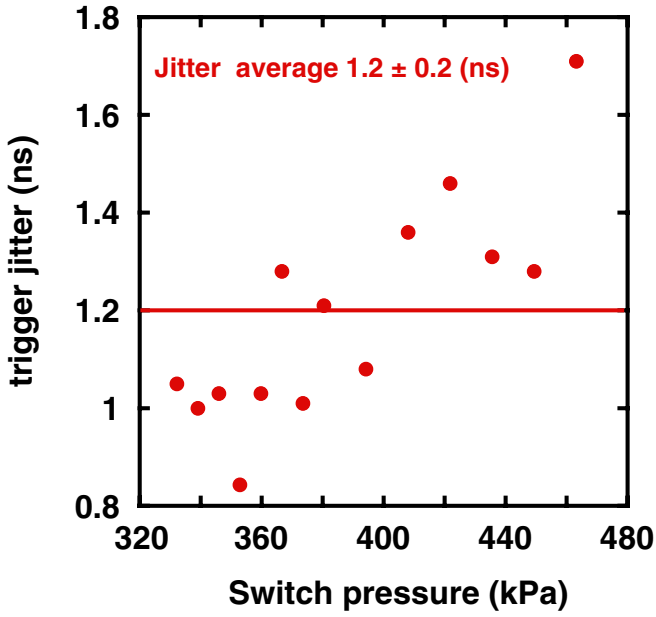

FIG. 15. (Color) Switch closure variation (jitter) for the switch pressure range studied.

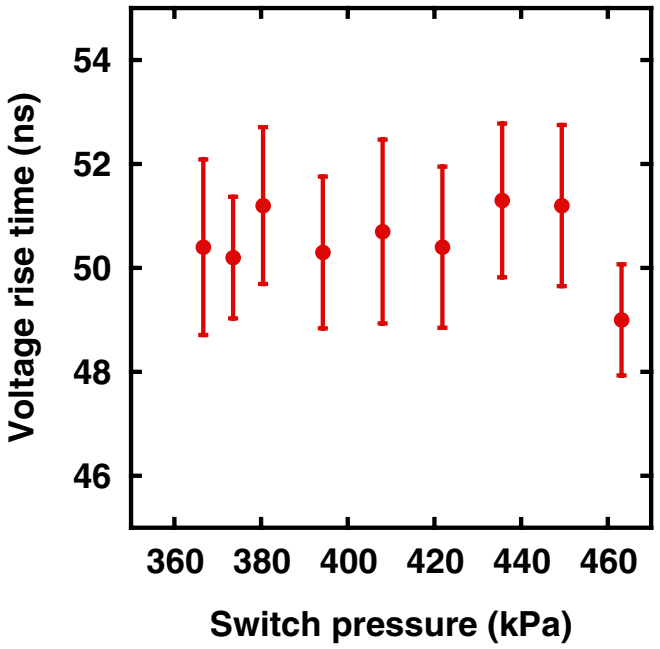

FIG. 16. (Color) Average pulse rise time as a function of switch pressure. The error bars represent the shot to shot statistical variation (1σ).

450 kPa the switch closure time increased by ~10 ns (Fig. 14). Following conditioning of the switches at the beginning of the experimentation with approximately 500 shots, no prefires were observed in the entire pressure range studied.

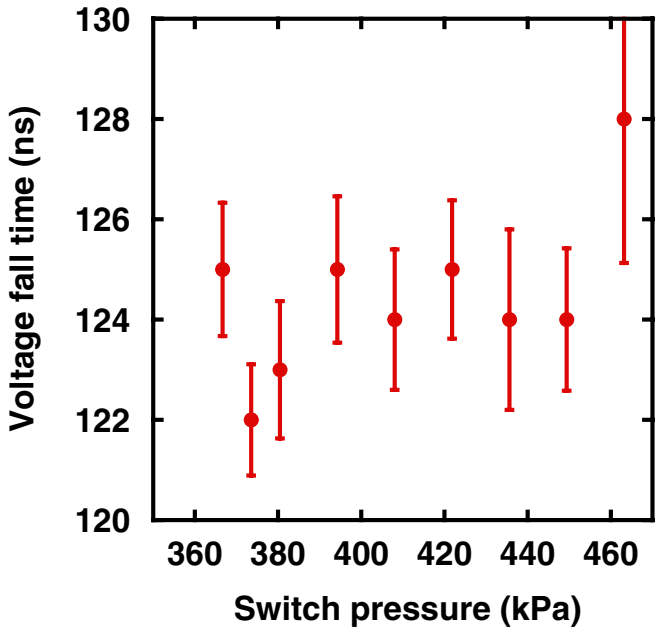

FIG. 17. (Color) Average pulse fall time as a function of switch pressure. The error bars represent the shot to shot statistical variation (1σ).

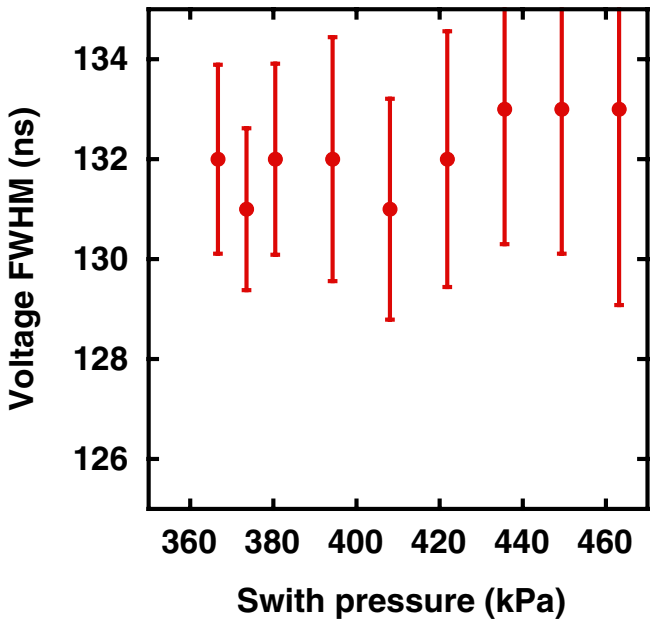

FIG. 18. (Color) Average output pulse full width at half maximum (FWHM) for a number of switch pressures. The charge voltage was always ±100 kV.

During the shot series the temperature of the liquid resistive load was monitored. The observed current and voltage amplitudes were obtained at approximately 20°C temperature. The liquid of the load had a closed-circuit recirculating cooling system.

The LTD II cavity performed equally well to the prototype cavity. At ±100 kV charging, following switch con-

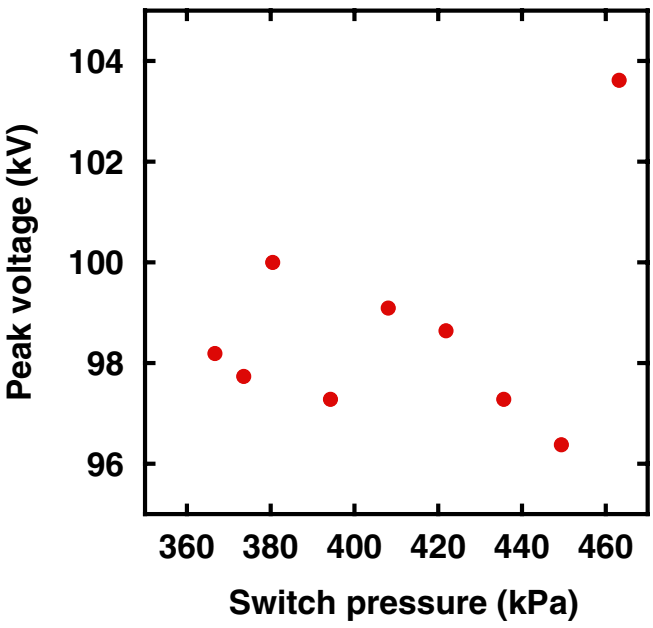

FIG. 19. (Color) Average output pulse amplitude as a function of switch pressure. The error bars are the standard deviation of 100 shots for each pressure and are smaller than the size of the dots.

ditioning, no prefires were observed in the experimentation range of 367 to 463 kPa. It is interesting to note that, although the studied pressure range varied from 5% to 32% above the self-brake pressure for a 200 kV voltage across the switches (Fig. 13), the output pulse characteristics remained practically unchanged. A switch research program is currently underway in Sandia National Laboratories to develop and evaluate alternative fast LTD switches.

VI. SUMMARY

An extensive test of the LTD technology is being performed at Sandia National Laboratories utilizing two, high current LTD cavities. Both the prototype LTD I cavity and the improved version LTD II performed remarkably well. The prototype cavity was operated only up to 90-kV charging and delivered to a matched load up to 0.45-MA current. 13 000 shots were logged in with neither prefires nor any active component failure. The pulse output shape and amplitude reproducibility were excellent (Fig. 9) with amplitude variation less than 1% (1σ). The jitter was as small as 2 ns. The achieved repetition frequency was 0.097 Hz, which is quite close to the 0.1 Hz required for IFE applications. The LTD II cavity is performing equally well. The output current and voltage to a matched load were, respectively, 0.5 MA and 100 kV. The gas switch pressure was varied, and the optimum operating pressure range where the output pulse has the fastest rise time and narrower FWHM was established. The impressive performance of the 0.5-MA LTD cavities encouraged us to proceed with the construction of the larger 1-MA LTD [2] cavities. These larger cavities will constitute the building blocks of the next generation of fast, high current pulsed-power accelerators and possibly be utilized as Z-pinch and IFE drivers and as high intensity x-ray radiographic sources. First tests of these larger cavities individually as well as in a five-cavity voltage adder configuration were performed at the High Current Electronic Institute at Tomsk, Russia, jointly with Sandia National Laboratories. This work will be reported in a separate publication [24]. Experiments with the LTD II cavity will continue in order to establish the lifetime of the active cavity components. In addition, it will serve as a test bed for evaluating a number of different types of switches developed in the USA, charging and trigger resistors, alternative capacitor configurations, and other cavity components.

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