Scalable flux controllers using adiabatic superconductor logic for quantum processors

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Quantum processors have the potential to accelerate specific computing tasks but are difficult to scale up due to engineering limitations, such as the number of available cables and cooling power for dilution refrigerators for quantum bits (qubits). Hence, it is very important to develop scalable, energy-efficient interface circuits that can control many qubits via a few control lines inside a dilution refrigerator. One of the most important interface circuits is the flux controller (FC), which generates arbitrary dc flux bias to adjust the characteristics of component devices such as qubits. In this paper, we propose and demonstrate FCs using an energy-efficient superconductor logic family, adiabatic quantum-flux-parametron (AQFP) logic. We develop two types of FCs: the AQFP FC and the AQFP/single-flux-quantum (AQFP/SFQ) FC. Both FCs require only a few control lines and have extremely small power dissipation, thus exhibiting high scalability. Furthermore, the AQFP/SFQ FC can control flux bias using ballistic SFQ transmission, which is crucial for integration with qubits. As a proof of concept, we demonstrate AQFP and AQFP/SFQ FCs at 4.2 K, fabricated by the AIST high-speed standard process. Our results indicate that AQFP logic is highly suitable for use as qubit interface circuits for very large-scale quantum processors, especially from the viewpoint of the control line count, power dissipation, and amount of supply currents.

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I. INTRODUCTION

Quantum processors (including circuit-based and annealing types) [1–5] hold the promise for outperforming classical computers in some specific applications [6–10]. However, scaling up quantum processors is a great engineering challenge due to various limitations. For superconducting quantum processors, increasing the quantum bit (qubit) count in a brute-force way has associated limitations regarding the number of cables and cooling power for a dilution refrigerator [11], in which qubits are cooled to ∼10 mK to suppress thermal noise. An alternative is to employ scalable, energy-efficient interface circuits that can control many qubits via a few control lines inside a dilution refrigerator. Such interface circuits are being extensively developed by several research groups using cryogenic complementary metal-oxide-semiconductor circuits [12] and superconductor Josephson circuits [13–17].

One of the most important interface circuits is the flux-bias circuit [13,18–21], which we refer to as a flux controller (FC) in this paper. An FC generates arbitrary dc flux bias to adjust the characteristics of component devices, such as the junction-pair balance and inductances of qubits and the coupling coefficients of couplers [13]. FCs are currently used in annealing quantum processors but should be similarly applicable to circuit-based quantum processors for qubit adjustment. An FC comprises an array of flux digital-to-analog converters (Φ-DACs) [13] integrated with a dedicated addressing scheme. The Φ-DACs apply dc flux to the target devices, and the polarity and/or magnitude of the flux bias generated by each Φ-DAC is externally programmed via the addressing scheme. The third-generation annealing quantum processor of D-Wave Systems Inc. [19] uses an FC comprising superconducting quantum interference device (SQUID)-based Φ-DACs integrated with the XYZ addressing scheme. This FC can apply dc flux bias to $n\,(\in \mathbb{N})$ devices using only $O(n^{1/3})$ control lines, thus reducing the cable count for qubit control. An even more scalable FC using the quantum flux parametron (QFP) [22,23] has been proposed [20,21]. This FC combines SQUID-based Φ-DACs with a QFP shift register (SR) as an addressing

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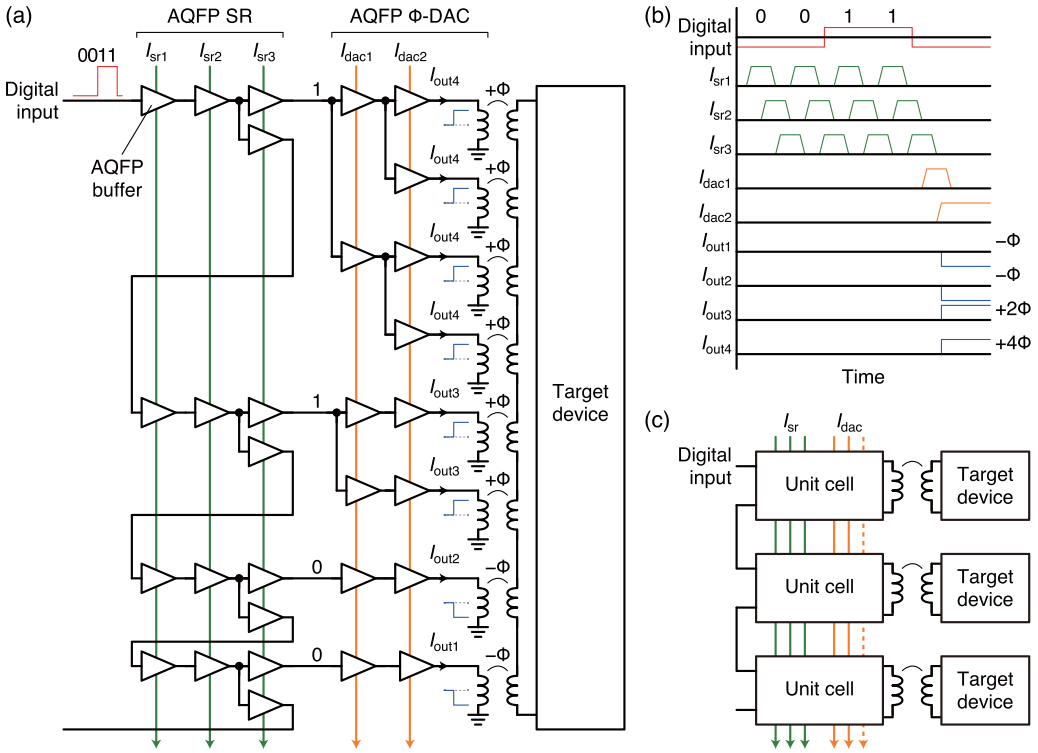


FIG. 1. Adiabatic quantum-flux-parametron (AQFP) flux controller (FC). (a) Unit cell, comprising an AQFP shift register (SR) and AQFP flux digital-to-analog converter (Φ-DAC). The AQFP Φ-DAC applies dc flux bias to the target device in accordance with the digital input sequence. (b) Typical waveforms. (c) Block diagram of an entire AQFP FC, comprising serially connected unit cells. The number of control lines does not increase with the target device count due to the serial connection.

circuit and can apply dc flux bias to n devices using just a few control lines, independent of the value of n. However, this QFP-based FC has not yet been demonstrated and has potential difficulties regarding integration with qubits, as will be explained later.

In this paper, we propose and demonstrate QFP-based FCs using adiabatic QFP (AQFP) logic [24,25], an energy-efficient superconductor logic family based on the QFP. We develop two types of FCs, the AQFP FC and the AQFP/single-flux-quantum (AQFP/SFQ) FC. Both FCs operate with high scalability (i.e., a few control lines, low power dissipation, and low supply currents) due to the nature of AQFP circuits, such as adiabatic switching [26,27] and serial excitation [28]. Furthermore, the AQFP/SFQ FC enables remote flux programming by combining AQFP and SFQ circuit technologies, which is crucial for integration with qubits. Interface circuits such as FCs should be placed apart from qubits since the insulating SiO_2 layers in the circuits can deteriorate the coherence time of qubits [16,29]. The AQFP/SFQ FC can solve this problem by programming the flux bias via long transmission lines, away from qubits. This is a clear advantage over the original QFP-based FC [20,21], which needs to be placed near qubits due to the use of galvanic and magnetic coupling.

In the following sections, we detail the AQFP and AQFP/SFQ FCs. We first explain the operating principle of both FCs and discuss the performance of each FC in terms of scalability, programming speed, and junction count. We show that both FCs can operate with a few control lines, independent of the target device count, and high flux programming speed. We also validate the basic idea of remote flux programming by a numerical simulation of the AQFP/SFQ FC. Furthermore, we demonstrate AQFP and AQFP/SFQ FCs, fabricated by the AIST 10 kA/cm^2 Nb high-speed standard process (HSTP) [28], at 4.2 K as a proof of concept of AQFP-based FCs. Finally, we summarize the features of the AQFP and AQFP/SFQ FCs in comparison with the previously proposed FCs. Our results indicate that AQFP-based FCs can be used to control the characteristics of many qubits in a very large-scale quantum processor.

II. AQFP FC

The AQFP FC is a simple FC comprising basic AQFP gates and can operate with a few control lines by taking advantage of the serial excitation scheme [28].

A. Operating principle

Figure 1(a) illustrates an example of the unit cell of the AQFP FC. The unit cell comprises an AQFP SR (i.e., buffer chain) and AQFP Φ-DAC. Here, I_{sr1} through I_{sr3} are the excitation currents for the AQFP SR, and I_{dac1} and I_{dac2} are those for the AQFP Φ-DAC. The AQFP Φ-DAC applies flux bias to the target device (e.g., a qubit and a coupler) by combining the magnetic flux generated by each buffer coupled to the target device, with the polarity and magnitude of the flux bias determined by the digital input sequence through the AQFP SR. In Fig. 1(a), a 4-bit input sequence 1100 [the least significant bit (LSB) appears first in the time waveforms in this paper, as in conventional serial data transmission] is transmitted through

the AQFP SR and is then converted into eight output currents in the AQFP Φ-DAC in a binary way, i.e., the ith bit in the sequence is converted into 2^{i-2} output currents, labeled $I_{\mathrm{out},i}(i \in \{2,\ 3,\ 4\})$, whereas the first bit is converted into a single output current, labeled I_{out1} (otherwise, the number of the output currents will be odd, and a zero flux bias cannot be generated). For example, the second bit 0 is converted into a single negative output current labeled I_{out2}, and the third bit 1 is converted into two positive output currents labeled I_{out3}. As a result, the AQFP Φ-DAC applies a total flux bias of $+4\Phi$ to the target device, if each positive (negative) output current generates a flux bias of $+\Phi$ $(-\Phi)$. The polarity and magnitude of the flux bias depends on the input sequence, and thus, the AQFP Φ-DAC shown in Fig. 1(a) can apply flux bias to the target device with a nine-level flux resolution $(-8\Phi,\ -6\Phi,\ ...,\ +6\Phi,\ +8\Phi)$, in accordance with nine input patterns (for example, 0000, 0001, ..., 1101, 1111). Note that a zero-flux bias (0Φ) is generated by, for example, 1000, where the flux generated by the most significant bit (MSB) cancels out those generated by the other three bits.

Figure 1(b) shows typical waveforms for the unit cell. The digital input sequence transmits through the AQFP SR in the manner of three-phase excitation [23] with I_{sr1} through I_{sr3}. After the entire sequence is loaded into the AQFP SR, I_{dac1} and I_{dac2} are activated in turn to distribute the sequence to the AQFP Φ-DAC. Finally, the output currents are generated, and a total flux bias of $+4\Phi$ is applied to the target device.

Figure 1(c) shows a block diagram of an entire AQFP FC with three target devices. This AQFP FC comprises 3 unit cells connected in series, through which the common excitation currents and digital input sequence are transmitted. Importantly, the number of control signals (I_{sr1}, I_{sr2}, I_{sr3}, I_{dac1}, I_{dac2}, and the digital input) and the amount of supply currents do not increase with the target device count n because of the serial connection, thus reducing the cable count for qubit control. Note that the number of excitation stages in an AQFP Φ-DAC increases with the flux resolution m because more output currents are generated via a longer splitter tree as m increases. However, an AQFP Φ-DAC with any number of stages can be operated by at most three excitation currents (I_{dac1}, I_{dac2}, and I_{dac3}) due to serial excitation [28]. Therefore, the number of control signals does not increase with m.

B. Discussion

Here, we discuss the advantages of the AQFP FC. First, the AQFP FC comprises only basic AQFP gates and is thus easy to design. Furthermore, the AQFP FC exhibits high scalability because an AQFP FC can operate with only seven control lines at most and a fixed amount of supply currents (independent of the values of n and m) and exhibits extremely small power dissipation due to adiabatic switching [26,27].

We also explore the flux programming speed of the AQFP FC. For an m-level flux resolution and an input sequence with a length of l $(\in \mathbb{N})$ bits per unit cell, m is given by

$$m = 1 + 2^{l-1}, \tag{1}$$

from Fig. 1(a). Therefore, the number of steps (i.e., clock cycles) required to load the input sequence into the entire AQFP SR for n target devices is $N_{\mathrm{sr}} = nl = n[\log_2(m-1) + 1] = O(n \log m)$. The logic depth, i.e., the number of excitation stages, $d(\in \mathbb{N})$ of an AQFP Φ-DAC is given by

$$d = l - 2, \tag{2}$$

from Fig. 1(a). Consequently, the number of steps required to distribute the data sequence in the entire AQFP SR to the AQFP Φ-DACs is $N_{\mathrm{dac}} = O(d) = O(\log m)$. Therefore, the total number of programming steps is given by

$$N = N_{\mathrm{sr}} + N_{\mathrm{dac}} = O(n \log m). \tag{3}$$

For large n and m, this step number is less than that for the conventional programming scheme [18] in the worst case, i.e., m flux quanta are loaded into each SQUID-based Φ-DAC one by one, which requires $N = O(nm)$ steps. The flux programming by the AQFP FC is relatively quick because all the AQFP Φ-DACs are programmed in parallel.

One drawback of the AQFP FC is that the excitation currents for the AQFP Φ-DACs need to be kept activated to continuously excite the AQFP buffers applying flux bias to the target devices. This can be solved by using the AQFP with π Josephson junctions (π-AQFP) [30] since π-AQFP gates are excited when the excitation current is off. Another drawback is that the gate count (i.e., junction count) in each AQFP Φ-DAC increases with m. It is difficult to precisely estimate the gate count for any m, and hence, we estimate the gate count roughly as follows: The gate count a of an AQFP Φ-DAC is assumed to be proportional to the bit length l and the logic depth d, i.e., $a = O(ld) = O(l^2) = O[(\log m)^2]$. Each gate (buffer) includes two Josephson junctions, so that the junction count of an AQFP Φ-DAC is given by $M_{\mathrm{dac}} = 2a = O[(\log m)^2]$. On the other hand, from Fig. 1(a), the junction count of an AQFP SR in a unit cell is given by $M_{\mathrm{sr}} = O(l) = O(\log m)$. Therefore, the junction count of an entire AQFP FC is given by

$$M = n(M_{\mathrm{dac}} + M_{\mathrm{sr}}) = O[n(\log m)^2]. \tag{4}$$

This is greater than the junction count for the conventional structure [18], for which $M = O(n)$. Therefore, the AQFP FC is suitable for systems with a small value of m (i.e., low flux-bias resolution).

All component circuits (i.e., buffers) in the AQFP FC operate adiabatically, so its power dissipation is extremely small. From the previous study [25], the energy dissipation of an AQFP buffer is $E \sim 10^{-23}$ J for an iteration frequency of $f =$ 100 MHz. Therefore, assuming $f = 100$ MHz, $n = 10^4$, and $m = 8$ ($\sim nm$ is the maximum number of AQFP buffers operating at the same time) as an example, the maximum power dissipation is roughly estimated to be $E \times nmf = 80$ pW, which should be negligibly small for various cryocoolers.

III. AQFP/SFQ FC

The AQFP FC operates with high scalability and high programming speed but requires a relatively large junction count for a high flux-bias resolution, which may occupy a relatively large circuit area. The AQFP/SFQ FC solves this problem by combining AQFP and SFQ circuit technologies, while sharing the advantages of the AQFP FC. The AQFP/SFQ FC also possesses an additional feature of remote flux programming.

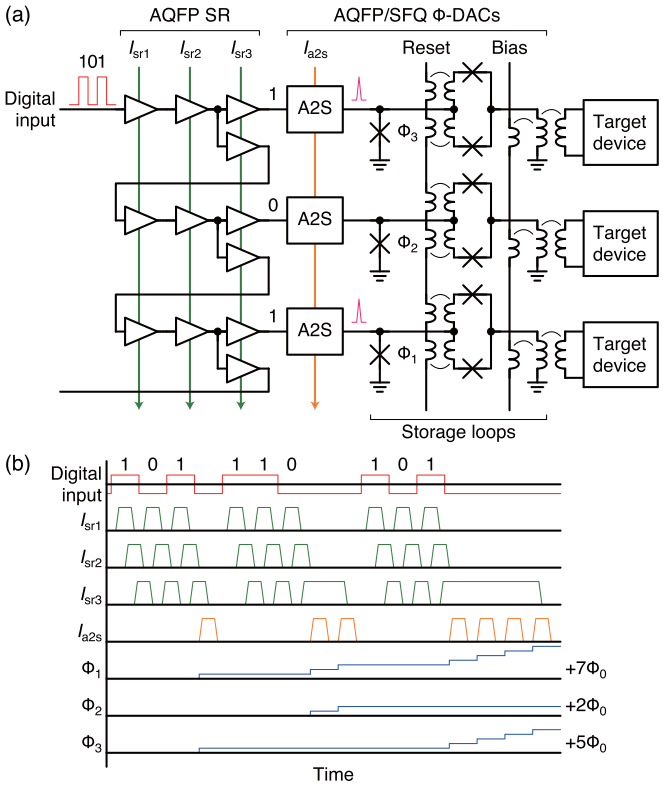


FIG. 2. Adiabatic quantum-flux-parametron (AQFP)/single-flux-quantum (SFQ) flux controller (FC). (a) Circuit diagram, comprising an AQFP shift register (SR) and AQFP/SFQ flux digital-to-analog converters (Φ-DACs). The AQFP-to-SFQ interfaces (A2Ss) load flux quanta into the storage loops in accordance with the digital input sequence, thereby controlling the flux bias to the target devices. (b) Typical waveforms, showing that the flux states (Φ_1 through Φ_3) of the three storage loops are controlled with an eight-level resolution by a nine-bit sequence.

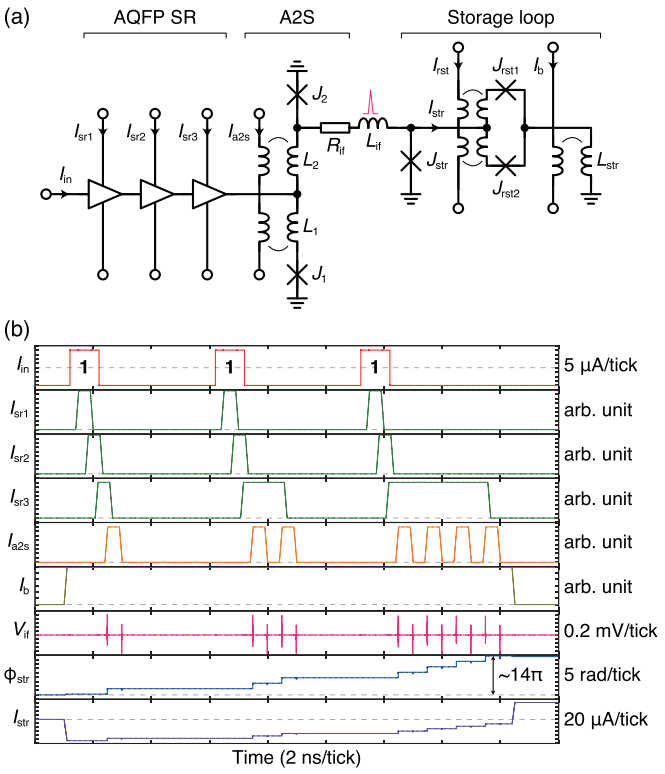


FIG. 3. Numerical simulation of a unit cell of the adiabatic quantum-flux-parametron (AQFP)/single-flux-quantum (SFQ) flux controller (FC). (a) Circuit diagram for numerical simulation. The critical currents are 200 μA, 200 μA, and 139 μA, for J_1, J_2, and J_{str}, respectively. β_c is 0.61, 1.9×10^2, and 4.0 for J_1, J_2, and J_{str}, respectively. $L_1 = L_2 = 1.48$ pH, $L_{if} = 1.68$ pH, $L_{str} = 171$ pH, and $R_{if} = 0.80$ Ω. (b) Simulated waveforms, showing that seven flux quanta are loaded into the storage loop by the digital input 111.

A. Operating principle

Figure 2(a) illustrates the circuit diagram of an AQFP/SFQ FC with three target devices. The AQFP/SFQ FC comprises an AQFP SR and AQFP/SFQ Φ-DACs, each including an AQFP-to-SFQ interface (A2S) [31] and a SQUID-based storage loop [13]. Here, I_{sr1} through I_{sr3} are the excitation currents for the AQFP SR, and I_{a2s} is that for the A2Ss. An AQFP/SFQ Φ-DAC applies flux bias to a target device by coupling the flux quanta in the storage loop to the target device, with the polarity and magnitude of the flux bias (i.e., the polarity and number of stored flux quanta) determined by the digital input sequence through the AQFP SR. Importantly, the number of control lines (I_{sr1}, I_{sr2}, I_{sr3}, I_{a2s}, the digital input, reset signal, and bias current) and the amount of supply current do not increase with n or m due to the serial excitation scheme [28], demonstrating the high scalability of the AQFP/SFQ FC.

Figure 2(b) shows typical waveforms for the AQFP/SFQ FC shown in Fig. 2(a), where Φ_1 through Φ_3 denote the flux quanta stored in the first through third storage loops. The operation of this AQFP/SFQ FC is as follows: The first three bits 101 are transmitted through the AQFP SR in synchronization with I_{sr1} through I_{sr3}. Then I_{a2s} is activated once, so that the first and third A2Ss load a flux quantum into the first and third storage loops, respectively, i.e., $\Phi_1 = \Phi_3 = \Phi_0$ (Φ_0 is a flux quantum), while Φ_2 remains at zero flux. For the second three bits 011 [the LSB appears first in Fig. 2(b)], I_{a2s} is activated twice, and then the first and second A2Ss load two flux quanta into the first and second storage loops, respectively, giving $\Phi_1 = 3\Phi_0$, $\Phi_2 = 2\Phi_0$, and $\Phi_3 = \Phi_0$. For the third three bits 101, I_{a2s} is activated four times, which results in $\Phi_1 = 7\Phi_0$, $\Phi_2 = 2\Phi_0$, and $\Phi_3 = 5\Phi_0$. In this binary way, flux quanta are loaded into the storage loops in parallel, which results in quick flux programming, as will be shown later.

To give a clearer image of the operation of the AQFP/SFQ FC, we conduct a numerical simulation of a unit cell of the AQFP/SFQ FC, shown in Fig. 3(a). The A2S is a QFP with a large LI_c product [31], which enables the A2S to operate nonadiabatically and produce SFQ pulses. The storage loop is based on an rf SQUID comprising a Josephson junction J_{str} and an inductor L_{str}, flux-biased by a bias current I_b. A dc SQUID with J_{rst1} and J_{rst2} is inserted into the storage loop to reset the flux state [13]. Consequently, the A2S can load flux quanta into the storage loop via J_{str} in accordance with the input current I_{in} applied to the AQFP SR.

Figure 3(b) shows simulation waveforms of the unit cell by a Josephson circuit simulator (JSIM) [32], where V_{if} is the voltage across J_2, ϕ_{str} is the phase difference across J_{str}, I_{str} is

the current through $L_{\rm str}$, and the gray dashed lines represent zero for each waveform. The circuit parameters, including the McCumber parameter $\beta_{\rm c}$ [33], used in the simulation are shown in the caption of Fig. 3, and the device parameters are for the HSTP. The unit cell operates as follows: $I_{\rm b}$ is activated first, and $I_{\rm sr1}$ through $I_{\rm sr3}$ are activated in turn to transmit the first input 1 through the AQFP SR. Then by activating $I_{\rm a2s}$, the A2S receives the input 1 and produces a positive SFQ pulse at $V_{\rm if}$, which is loaded into the storage loop via $J_{\rm str}$ (i.e., $\phi_{\rm str}$ increases by $\sim 2\pi$). When turning off $I_{\rm a2s}$, the A2S also produces a negative pulse at $V_{\rm if}$, which escapes via the isolation resistor $R_{\rm if}$ (a more detailed description of the A2S can be found in the literature [31]). For the second input 1, $I_{\rm a2s}$ is activated twice, so that two flux quanta are added to the storage loop. Then for the third input 1, four flux quanta are added to the storage loop by activating $I_{\rm a2s}$ four times, which results in $\phi_{\rm str} \approx 14\pi$ (i.e., seven flux quanta are kept in the storage loop). Finally, $I_{\rm b}$ is turned off, and a current corresponding to seven flux quanta remains at $I_{\rm str}$, which applies flux bias to a target device via magnetic coupling. In this binary way, the unit cell can control the magnitude of the flux bias (i.e., the number of flux quanta in the storage loop) with an m-level resolution by a $\log_2 m$-bit sequence at $I_{\rm in}$. Moreover, the polarity of the flux bias can also be controlled by changing the polarity of the flux quanta in the storage loop. This can be done by loading negative flux quanta into the storage loop using a negative pair of $I_{\rm a2s}$ and $I_{\rm b}$, which will be confirmed in later experiments.

B. Discussion

Here, we discuss the performance of the AQFP/SFQ FC. As with the AQFP FC, the AQFP/SFQ FC exhibits high scalability because an AQFP/SFQ FC can operate with only seven control lines and a fixed amount of supply current (independent of the values of n and m), in addition to exhibiting extremely small power dissipation. Note that the SFQ part in the AQFP/SFQ FC (i.e., storage loop) is flux-biased and hence does not generate static power dissipation, unlike the conventional SFQ logic family, rapid SFQ (RSFQ) logic [34].

Furthermore, we explore the flux programming speed of the AQFP/SFQ FC. For n target devices and an m-level flux resolution, an n-bit sequence is loaded into the AQFP SR $\log_2 m$ times, according to Fig. 2. Here, $N_{\rm sr} = n$ steps are required to load each n-bit sequence into the AQFP SR. Moreover, for the ith n-bit sequence ($i \in \mathbb{N}$), $N_{\rm dac} = 2^{i-1}$ steps are required to add flux quanta into the storage loops. Hence, the total programming step count is given by

$$\begin{aligned} N &= \sum_{i=1}^{\log_2 m} (N_{\rm sr} + N_{\rm dac}) \\ &= \sum_{i=1}^{\log_2 m} (n + 2^{i-1}) = n\log_2 m + m - 1 = O(n\log m), \end{aligned} \quad (5)$$

assuming that n is much larger than m. As with the AQFP FC, this programming step count is less than that for the conventional programming scheme in the worst case [$N = O(nm)$], due to the parallel flux programming of the AQFP/SFQ Φ-DACs.

Moreover, unlike the AQFP FC, the junction count of the AQFP/SFQ FC does not increase with m because more flux quanta can be stored in each storage loop by increasing the critical current of $J_{\rm str}$ and/or the value of $L_{\rm str}$. Therefore, the total junction count of an AQFP/SFQ FC is $M = O(n)$, indicating that the AQFP/SFQ FC will occupy a smaller circuit area than the AQFP FC for systems with a large value of m (i.e., high flux-bias resolution). The maximum value of m depends on the layout design and fabrication process but should be as large as the flux resolution of the annealing quantum processors of D-Wave Systems Inc. (for instance, 8 bits in the second-generation machine [18]) since the basic design of the flux storage loop in the AQFP/SFQ Φ-DAC is similar to that in the Φ-DAC of D-Wave Systems Inc. processors.

The AQFP/SFQ FC does not generate static power dissipation, so its power dissipation is determined by the nonadiabatic switching of the Josephson junctions in the A2S and storage loop. Here, J_1 and J_2 in the A2S dissipate an energy of $\sim 2I_{\rm c,a2s}\Phi_0$ per cycle, where $I_{\rm c,a2s} = 200$ μA is the critical current of J_1 and J_2. Also, $J_{\rm str}$ dissipates an energy of $\sim I_{\rm c,str}\Phi_0$ per flux storage operation, where $I_{\rm c,str} = 139$ μA is the critical current of $J_{\rm str}$. The other parts in the AQFP/SFQ FC operate adiabatically and dissipate much less energy. Therefore, assuming $f = 100$ MHz and $n = 10^4$, the maximum power dissipation is roughly estimated to be $(2I_{\rm c,a2s} + I_{\rm c,str})\Phi_0 \times nf = 1.1$ μW, which is still less than the typical cooling power of dilution refrigerators (~ 10 μW) and indicates the high energy efficiency of the AQFP/SFQ FC. The power dissipation can be further reduced by lowering the critical currents of the Josephson junctions.

Another notable feature of the AQFP/SFQ FC is remote flux programming. As mentioned in the introduction, interface circuits such as FCs typically include insulating SiO_2 layers because of the use of multilayer Nb processes [35,36] and should thus be placed apart from qubits. This is difficult for the AQFP FC and the original QFP-based FC [20,21] since the superconducting building blocks are combined via galvanic and magnetic coupling. In the AQFP/SFQ FC, the A2Ss are decoupled from the storage loops by $R_{\rm if}$ [see Fig. 3(a)], which enables ballistic SFQ transmission [37,38] between an A2S and a storage loop. For this reason, the AQFP/SFQ FC can perform remote flux programming, as shown in Fig. 4(a), assuming the use of three-dimensional multichip integration [39]. Only the storage loop is integrated on the qubit chip, whereas the other parts (AQFP SR and A2S) are integrated on a different chip, with the storage loop and the other parts connected to each other via a transmission line through an interposer. Figure 4(a) illustrates a unit cell, but the illustration could be easily expanded into an entire AQFP/SFQ FC; thus, most of the parts in the AQFP/SFQ FC can be placed apart from qubits. Furthermore, a storage loop is a simple structure and should be able to be integrated on the qubit chip without using SiO_2 layers. Hence, remote flux programming using the AQFP/SFQ FC can solve the problem of integration with qubits. Note that it is also possible to integrate the storage loop on the interposer chip, depending on the multichip configuration. To validate the above idea, we conduct a numerical simulation of the circuit shown in Fig. 4(a). In the simulation, the circuit and device parameters are the same as those used in Fig. 3. A transmission line with a characteristic impedance

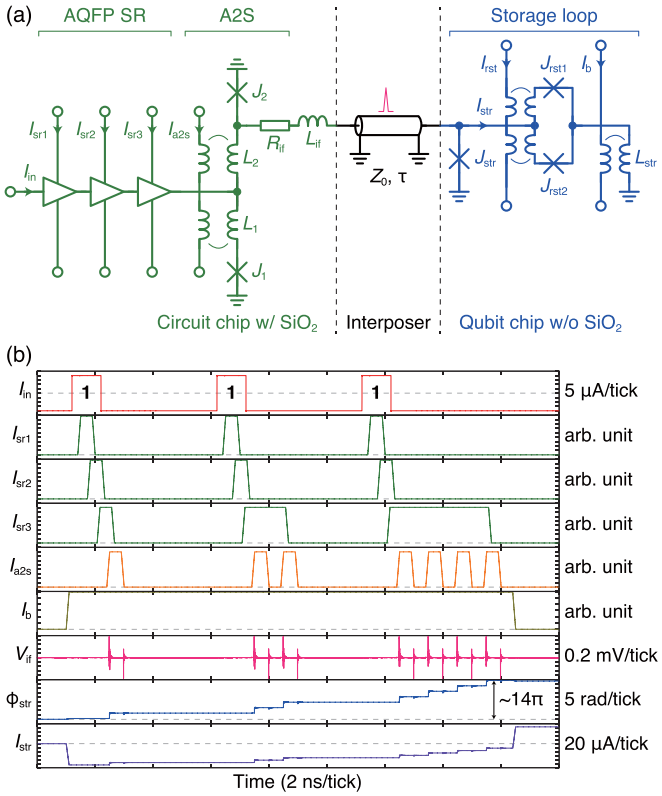


FIG. 4. Remote flux programming using the adiabatic quantum-flux-parametron (AQFP)/single-flux-quantum (SFQ) flux controller (FC). (a) Conceptual circuit diagram. (b) Simulated waveforms, showing that seven flux quanta are loaded into the storage loop via a long transmission line ($Z_0 = 3.7\ \Omega$ and $\tau = 10$ ps).

(Z_0) of 3.7 Ω and a propagation delay (τ) of 10 ps, which corresponds to a length of 3.0 mm for the speed of light, is inserted between the A2S and storage loop. Figure 4(b) shows simulated waveforms by JSIM. Although small reflections can be seen at $V_{\rm if}$, the A2S loads seven flux quanta into the storage loop via a long transmission line in the same manner as the waveforms shown in Fig. 3(b), thereby validating the basic idea of remote flux programming.

IV. EXPERIMENTS

As a proof of concept, we demonstrate unit cells of the AQFP FC and the AQFP/SFQ FC at 4.2 K in liquid He. Specifically, we measure the flux bias generated by each FC and show that both AQFP and AQFP/SFQ FCs can control flux bias in accordance with the digital inputs. We fabricated the FC chips using the HSTP.

A. Demonstration of an AQFP FC

Figure 5(a) shows a micrograph of the fabricated AQFP FC, which comprises an AQFP SR, an AQFP Φ-DAC, and a dc SQUID as a target device, based on the circuit schematic shown in Fig. 1(a). The AQFP Φ-DAC applies flux bias to the dc SQUID in accordance with the input current $I_{\rm in}$, and the polarity and magnitude of the flux bias are measured by the modulation of the dc SQUID (i.e., V-Φ characteristics) [40,41], with bias and modulation currents ($I_{\rm sq}$ and $I_{\rm mod}$) applied to the dc SQUID. During experiments, all the control signals except for $I_{\rm sq}$ were supplied by arbitrary waveform generators, and the output voltage $V_{\rm out}$ of the dc SQUID was amplified by a 40-dB low-noise amplifier and observed by an oscilloscope. Note that the AQFP SR and AQFP Φ-DAC were designed using directly coupled AQFP cells [42] for miniaturization and that the upper right circuit in Fig. 5(a) is a buffer chain for the preliminary test of data transmission through the AQFP SR.

Figure 5(b) shows measurement waveforms for two different input patterns, 1111 and 0011. Due to the design difference in the AQFP Φ-DAC, the MSB appears first at $I_{\rm in}$ in this figure, whereas the LSB appears first in Fig. 1(b). The input sequence through $I_{\rm in}$ is loaded into the AQFP SR in synchronization with $I_{\rm sr1}$ through $I_{\rm sr3}$. Then the AQFP Φ-DAC receives the sequence from the AQFP SR and applies flux bias to the dc SQUID by turning on $I_{\rm dac1}$ and $I_{\rm dac2}$. Finally, $I_{\rm mod}$ ramps up and the modulation of $V_{\rm out}$ is observed. Between the two input sequences, the dc SQUID generates voltage pulses at different timings during the increase of $I_{\rm mod}$, which indicates that the dc SQUID modulation is shifted by the flux bias generated by the AQFP Φ-DAC. During the first ∼50 μs, some signals appear at $V_{\rm out}$ because $I_{\rm sq}$ was always on and the dc SQUID responded to the AQFP Φ-DAC during flux programming. These signals do not affect the flux bias measurements.

Figure 5(c) shows the measurement results of the dc SQUID modulation for all nine input patterns (0000, 0001, ..., 1101, 1111), where $\Phi_{\rm mod}$ is the modulation flux applied to the dc SQUID by $I_{\rm mod}$. The dc SQUID modulation clearly shifts depending on the input sequence, thus demonstrating that the flux bias $\Phi_{\rm dac}$ generated by the AQFP Φ-DAC is controlled by $I_{\rm in}$. Assuming that $\Phi_{\rm dac}$ is zero flux for a sequence of 1000 (since the flux generated by the MSB should cancel out those generated by the other three bits), we calculate $\Phi_{\rm dac}$ for all the input patterns from the shift amount of the dc SQUID modulation. Figure 5(d) shows $\Phi_{\rm dac}$ as a function of the input sequence, where the markers are the data calculated from Fig. 5(c) and the line denotes the linear regression. This figure clearly demonstrates that the AQFP FC can control flux bias by a nine-level flux resolution. From the linear regression, the resolution of $\Phi_{\rm dac}$ is found to be $5.8 \times 10^{-2} \times \Phi_0$ per level, which depends on the coupling coefficient between each AQFP buffer in the AQFP Φ-DAC and the target device.

B. Demonstration of an AQFP/SFQ FC

Figure 6(a) shows a micrograph of a fabricated AQFP/SFQ FCs, where the left-hand FC is evaluated in this paper. The AQFP/SFQ FC comprises an AQFP SR, an AQFP/SFQ Φ-DAC (i.e., an A2S and a storage loop), and a dc SQUID as a target device, based on the circuit schematic shown in Fig. 3(a). In a similar way to the experiments for the AQFP FC, we measure the flux bias generated by the AQFP/SFQ FC from dc SQUID modulation.

Figure 6(b) shows measurement waveforms under two bias conditions for the AQFP/SFQ Φ-DAC: positive and negative pairs of $I_{\rm a2s}$ and $I_{\rm b}$. The left-hand waveforms show that six flux quanta are loaded into the storage loop by the input sequence 110 [the LSB appears first in Fig. 6(b)] and a positive pair

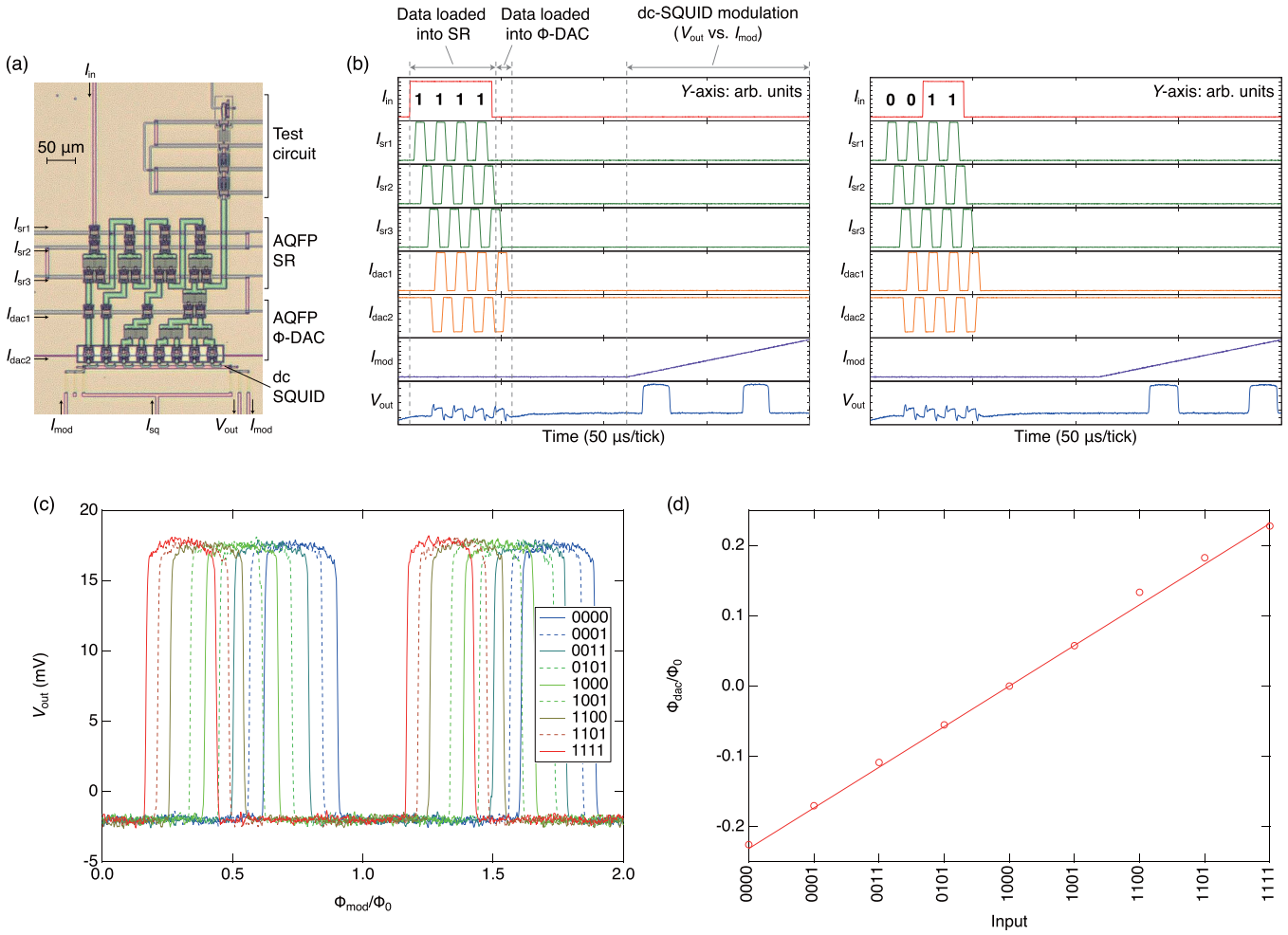


FIG. 5. Experiments on an adiabatic quantum-flux-parametron (AQFP) flux controller (FC) at 4.2 K. (a) Micrograph, where a dc SQUID is coupled to the AQFP flux digital-to-analog converter (Φ-DAC) as a target device. (b) Measurement waveforms for two different input patterns of 1111 and 0011. (c) Measurement results of the dc SQUID modulation for all input patterns. (d) Flux bias as a function of the input sequence, calculated from the dc SQUID modulation. This figure demonstrates that the AQFP FC can control flux bias with a nine-level resolution in accordance with the input sequence.

of I_{a2s} and I_b. Compared with Fig. 3(b), the profile of I_b is complex due to the characteristics of the A2S. We used an A2S optimized for gigahertz-range frequencies [31], and thus, in this experiment, we controlled the amplitude of I_b such that a flux quantum is correctly loaded into the storage loop at the rise edge of I_{a2s}. This I_b control will be unnecessary if the A2S is optimized for lower operating frequencies. The right-hand waveforms in Fig. 6(b) show that three negative flux quanta are loaded into the storage loop by the input sequence 100 and a negative pair of I_{a2s} and I_b. As mentioned above, the AQFP/SFQ Φ-DAC can store negative flux quanta by inverting the polarity of I_{a2s} and I_b. In this operating mode, the polarity of I_{in} is also inverted, and thus, negative flux quanta are loaded into the storage loop when the input is a 0. During the first ∼150 μs, some signals appear at V_{out} because I_{sq} was always on, and the dc SQUID responded to the AQFP/SFQ Φ-DAC during flux programming. These signals do not affect the flux bias measurements.

Figure 6(c) shows the measurement results of the dc SQUID modulation for all eight input patterns (000, 001, ..., 111) in the case of positive I_{a2s} and I_b. The dc SQUID modulation clearly shifts depending on the input sequence, thus demonstrating that Φ_{dac} generated by the AQFP/SFQ Φ-DAC is controlled by I_{in}. We also observe a similar dc SQUID modulation for negative I_{a2s} and I_b. Moreover, we calculate Φ_{dac} for all the input patterns from the shift amount of the dc SQUID modulation, assuming that Φ_{dac} is zero flux when the input sequence is 000 and 111 for positive and negative pairs of I_{a2s} and I_b, respectively (since no flux is loaded into the storage loop). Figure 6(d) shows Φ_{dac} as a function of the input sequence for both positive and negative pairs of I_{a2s} and I_b, where the markers are the data calculated from the dc SQUID modulation, and the lines denote linear regression. This figure clearly demonstrates that the AQFP/SFQ FC can generate both positive and negative flux bias and that the flux bias is controlled with an eight-level flux resolution under each bias condition. From the linear regression, the resolution of Φ_{dac} is $3.7 \times 10^{-2} \times \Phi_0$ per level, which depends on the coupling coefficient between the storage loop and the target device.

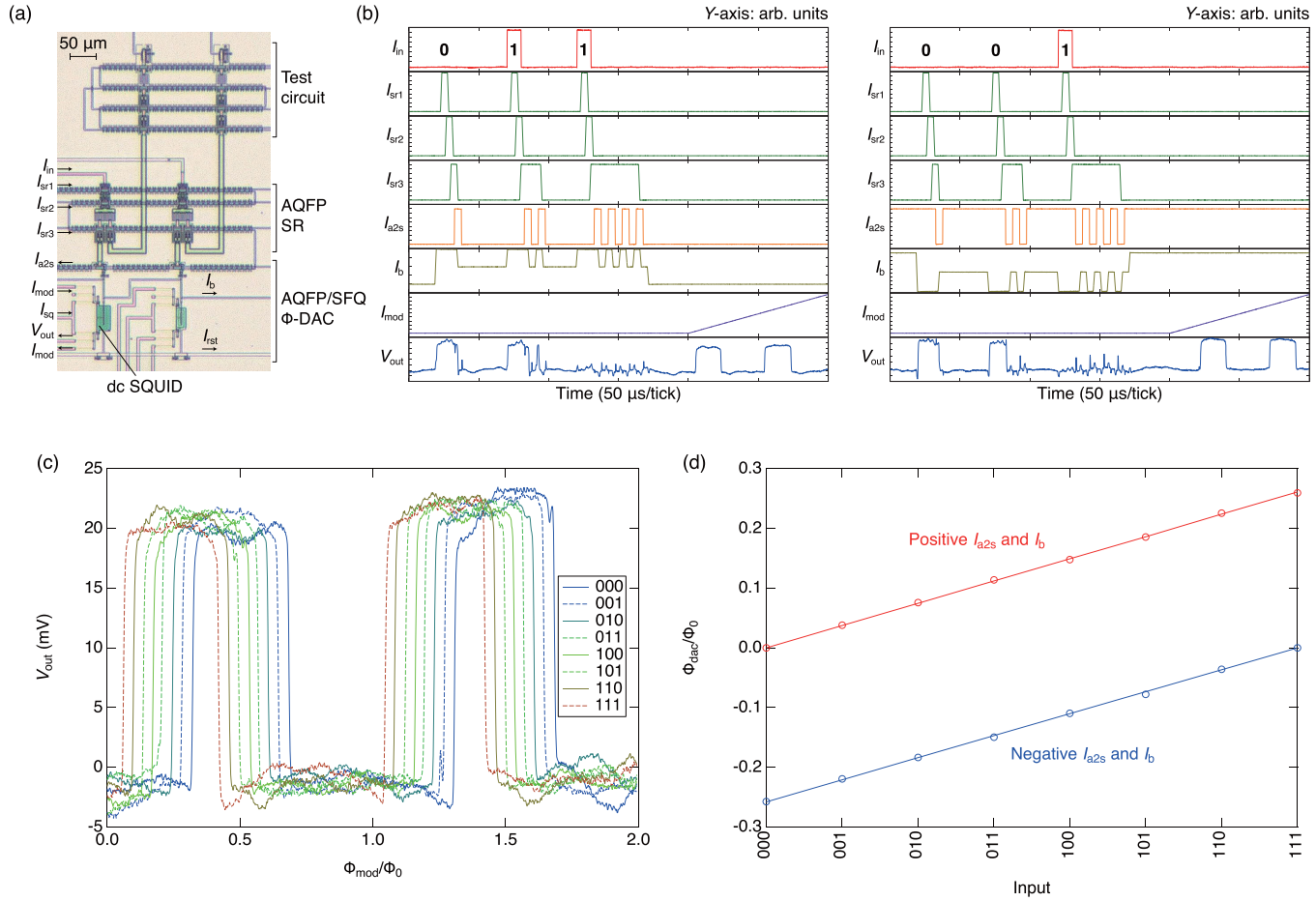


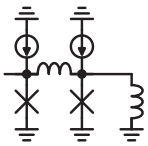
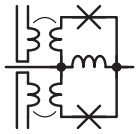
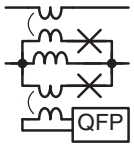
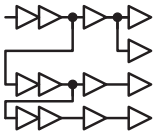
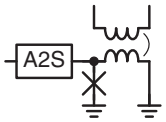
FIG. 6. Experiments on an adiabatic quantum-flux-parametron (AQFP)/single-flux-quantum (SFQ) flux controller (FC) at 4.2 K. (a) Micrograph, where the left-hand AQFP/SFQ FC was evaluated. (b) Measurement waveforms under two different bias conditions: positive and negative pairs of I_{a2s} and I_b. (c) Measurement results of the dc SQUID modulation for positive I_{a2s} and I_b. (d) Flux bias as a function of the input sequence. This figure demonstrates that the AQFP/SFQ FC can control flux bias with an eight-level resolution under each bias condition, in accordance with the input sequence.

V. CONCLUSIONS

Inspired by the early proposal of the QFP-based FC [20,21], we developed two types of scalable FCs using AQFP logic for quantum processors: the AQFP FC and the AQFP/SFQ FC. Both FCs exhibit high scalability in terms of the number of control lines and the amount of supply current, which results from the use of serial data transmission through an AQFP SR. Additionally, both FCs can program flux bias to multiple devices using less programming steps than the conventional scheme in the worst case because of the parallel operation of the AQFP and AQFP/SFQ Φ-DACs. Furthermore, the AQFP/SFQ FC can perform remote flux programming, where the storage loops and the other parts of the system can be separated by long transmission lines. This feature will be crucial for integration with qubits. Our proof-of-concept experiments at 4.2 K demonstrated that both AQFP and AQFP/SFQ FCs can control the flux bias by digital inputs. The above results indicate that AQFP logic is highly suitable for use in qubit interface circuits for very large-scale quantum processors.

Finally, we summarize the features of various FCs in Table I. The features of the RSFQ, XYZ-SQUID, and QFP FCs (where the names for these FCs are assigned for convenience) were estimated from the literature [13,18–21]. Some of the items were difficult to estimate and were thus inferred as explained in the footnotes of Table I. The item *low-power operation* denotes whether the FC can operate without static power dissipation. The RSFQ FC generates static power dissipation due to bias resistors. The item *isolation from SiO_2* denotes whether qubits can be decoupled from the SiO_2 layers in the FC chip. Remote flux programming may be applicable to the RSFQ and XYZ-SQUID FCs, as with the AQFP/SFQ FC. The item *demonstration* denotes whether a demonstration of the FC has been reported in the literature. To the best of our knowledge, a demonstration of the QFP FC has not been reported yet. Overall, the use of superconductor digital circuits contributes to a significant reduction in the control line count. Especially addressing using a QFP-based SR enables flux programming via a few control lines. The comparison in Table I clarifies the advantages of the AQFP/SFQ FC for every performance aspect. One of the most important challenges for using the AQFP/SFQ FC in actual quantum processors is to achieve storage loops with a large inductance for high flux resolution (i.e., large m values). Therefore, we plan to adopt space-efficient inductor technologies, such as three-dimensional, stacked inductors

TABLE I. Comparison of various FCs.

Technology	RSFQ	XYZ-SQUID	QFP	AQFP	AQFP/SFQ
Unit cell					
Φ-DAC	SQUID	SQUID	SQUID	AQFP buffers	A2S and SQUID
Addressing	RSFQ demux tree	XYZ addressing	QFP SR	AQFP SR	AQFP SR
Number of control lines	$O(\log n)$	$O(n^{1/3})$	$O(1)$	$O(1)$	$O(1)$
Amount of supply current	$O(n)$	$O(1)$	$O(1)$	$O(1)$	$O(1)$
Junction count	$O(n)$	$O(n)$	$O(n)$	$O[n(\log m)^2]$	O(n)
Number of programming steps in the worst case	$O(nm)$	$O(nm)$	$O(n \log m)$[a]	$O(n \log m)$	$O(n \log m)$
Low-power operation		√	√	√	√
Isolation from SiO_2	√[b]	√[b]			√
Demonstration	√	√		√	√
Reference	[13]	[18,19]	[20,21]	This paper	This paper

[a]The number of programming steps is not clear from the literature but should be the same as those for the AQFP and AQFP/SFQ FCs.
[b]Remote flux programming may be applicable.

[43], Josephson inductances [44], and high kinetic-inductance materials [45].

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