Spatial dependence of dopant incorporation and electrical transport in Si-doped GaAs(Sb) nanowires

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Silicon (Si) impurities are among the most widely used dopants in GaAs-based electronic and optoelectronic materials, including low-dimensional systems such as nanowires (NWs). Undesired *p*-type conduction is often observed in Si-doped GaAs NWs due to the amphoteric nature of Si, but can be mitigated by proper catalyst-free, vapor-solid growth processes. Yet, the intriguing dynamics of Si dopant incorporation and spatial distribution within the NW structure are largely unknown, which are key to understanding the resulting electrical activity on a local scale. Here, we correlate the spatial distribution of Si dopants with the electrical transport characteristics of catalyst-free, selective-area grown GaAs(Sb) NWs. Through a combination of atom probe tomography, resonant Raman scattering, and single-NW field effect transistor measurements, spatial nonuniformities in Si concentration are revealed in both the axial and the radial directions. Si dopant gradients induced by the highly nonlinear growth rate along the NW axis result in varying rectifying current-voltage (*I*-*V*) characteristics with decreased conductivity (lower Si concentration) towards the NW tip. Surface segregation further leads to increased Si concentrations (up to $\sim 10^{20}$ cm^{-3}) on the surface of the GaAs(Sb) sidewalls, generating a thin parasitic region of high *p*-type conductivity. Finally, removal of the Si-enriched *p*-type surface region is demonstrated by controlled wet chemical etching in citric acid, revealing the intended *n*-type conduction of the bulk region of the NW.

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I. INTRODUCTION

Over the years, freestanding III-V semiconductor nanowires have emerged as a promising material platform for a variety of nanoscale device applications due to their unique one-dimensional (1D) geometry and associated freedom in heterostructure engineering [1]. They form an integral part of electronic and optoelectronic devices including advanced NW field-effect transistors (NW-FET) [2–4], NW-based light-emitting diodes and lasers [5–8], and next-generation solar cells [9,10] and photodetectors [11,12], in which accurate doping control is mandatory to enable the envisioned performance.

Indeed, doping control has been an intense subject of research in the recent decade [13,14], especially in GaAs-based NWs, where the realization of reliable *n*-type conductivity has remained challenging [14,15]. The most common *n*-type dopant source in GaAs is silicon (Si), which, however, is amphoteric by nature [16], and may lead to undesired *p*-type behavior under certain conditions [14,17–19]. In typical catalyst-assisted GaAs NWs grown by vapor-liquid-solid processes, Si dopants incorporated via the metal-rich droplet reservoir preferentially occupy anion (As) sites [14,17–19], resulting in *p*-type doping. *n*-type doping on cation (Ga) sites is only achieved through extreme As-rich conditions as in hydride vapor phase epitaxy [14] or by means of vapor-solid (VS), selective area epitaxial (SAE) approaches [5,20–22]. In these processes both axial and radial growth are present that are expected to lead to differences in doping rates; however, studies of dynamically varying incorporation and spatial distribution of Si dopants within VS-grown GaAs NWs, and their corresponding local electrical activity, are still missing. Such insights are instrumental for the development of intentionally doped NW devices [23–25], as in NW solar cells, electroluminescent NW devices, or Esaki tunnel diodes, where spatial doping inhomogeneities may affect *p*-*n* junction design, carrier recombination dynamics, and current-voltage characteristics [25,26].

Here, we report on the spatial dependencies of Si dopant incorporation and associated electrical transport characteristics of entirely droplet-free, VS-type GaAs(Sb) NWs grown by SAE on silicon. We combine a variety of methods, including atom probe tomography (APT), resonant Raman scattering, and single-NW transport characterization to derive spatial variations in the Si dopant distribution both in the axial and the radial directions. Different dopant distributions are shown to lead to distinct gradients of the current-voltage (*I*-*V*) characteristics and carrier conductivity along the NW, as well as the formation of a Si-dopant-enriched *p*-type surface region. Wet-chemical postprocessing of the Si-enriched surface layer is further developed to recover the desired *n*-type conductive nature of the as-doped NWs.

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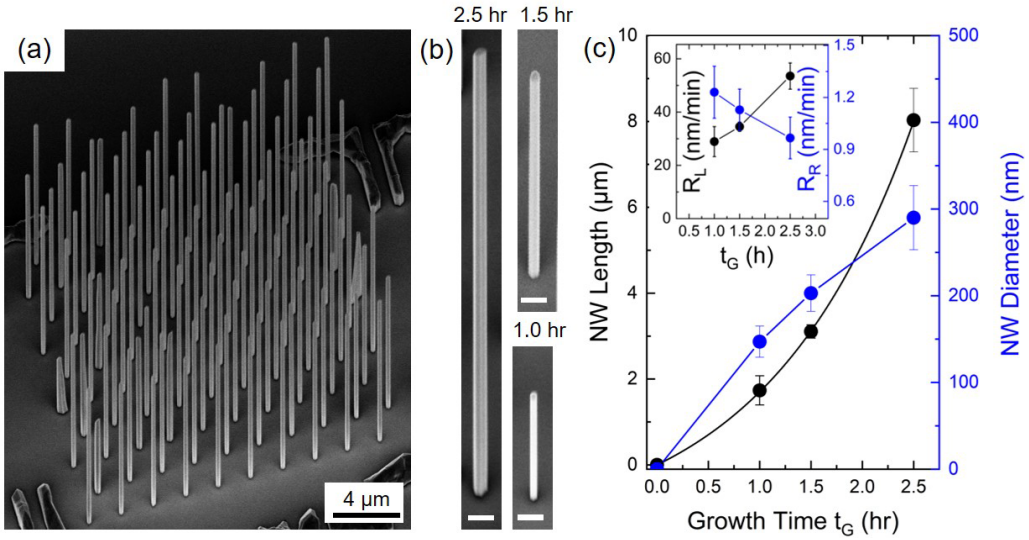

FIG. 1. (a) SEM image of a Si-doped GaAs(Sb) NW array grown for 2.5 h, resulting in ∼8-μm-long and ∼300-nm-thick NWs. (b) Enlarged SEM images of single NWs grown at different growth times of 1, 1.5, and 2.5 h under otherwise identical conditions. (c) Evolution of NW length/diameter and corresponding axial (R_L) and radial (R_R) growth rates with growth time t_G (see inset). The scale bar in (b) is the same for all images (0.5 μm).

II. EXPERIMENTAL DETAILS AND RESULTS

A. Nanowire growth

The Si-doped GaAs(Sb) NWs were grown by solid-source molecular beam epitaxy (MBE) on lithographically prepatterned Si(111) substrates, as described in detail in our previous work (Refs. [24,27]). The mask pattern was defined in a 20-nm thin SiO_2 dielectric layer on top of the Si substrate, consisting of various fields with different mask opening sizes ($d_0 = 50$–140 nm) and pitch ($p = 0.25$–$2\,\mu$m). To obtain NWs with extended lengths (several micrometers long), which are necessary for electrical transport characterization with multiple contacts placed on single NWs, an antimony (Sb) flux was provided during the growth [24,27,28]. The surfactant action of Sb, which occurs in the limit of low Sb flux, substantially increases the axial growth rate, but keeps the Sb incorporation very low (∼1%–2%), in order to mimic the electronic properties of Sb-free GaAs NWs [27,28]. In contrast, GaAs NWs grown by MBE without a supply of Sb surfactant tend to suffer from early growth termination and limited lengths [29]. Growth was performed at a temperature of 685 °C under highly As-rich conditions (V/III ratio of 63), using a Ga flux of 0.6 Å s^{-1}, and As/Sb beam equivalent pressure of 5.5×10^{-5} and 3×10^{-7} mbar, respectively [24].

Si doping was enabled by a thermal sublimation source, where the doping level is controlled by adjusting the source filament current. In our system, a filament current of 13 A (used throughout this study) creates a Si flux of $\sim 1.6 \times 10^{12}$ cm^{-2} s^{-1} that yields a corresponding Si dopant concentration of 1.4×10^{19} cm^{-3} in planar Si-doped GaAs reference films (growth rate of $\sim 1\,\mu m\,h^{-1}$) [30]. Similar Si dopant concentrations are also measured in the present Si-doped GaAs(Sb) NWs, as discussed below. The high Si doping level was chosen to probe *variations* in Si distribution via APT with high accuracy above the APT sensitivity limit of $\sim 2 \times 10^{18}$ cm^{-3}. NW samples grown for APT analysis contain an additional thin undoped AlGaAs/GaAs shell passivation layer (5 nm $Al_{0.3}Ga_{0.7}As$/3 nm GaAs) that serves as a marker of the terminal growth surface. All other NWs explored in this study are free of any surface passivation.

Figure 1(a) presents a typical scanning electron microscopy (SEM) image of an as-grown Si-doped GaAs(Sb) NW array on Si, obtained for a growth time of 2.5 h and pattern pitch of 2 μm. The array shows high uniformity with good growth yield (>90%), and only slight size fluctuations that are attributed to the stochastic nature of the underlying twin-induced growth mechanism [29,31]. The NWs exhibit a nontapered morphology with a length of 8±0.74 μm, a diameter of 295±37 nm, and a crystal structure that is exclusively of a zinc-blende phase with rotational twin domains, as previously identified from transmission electron microscopy studies [27,28]. To better understand the growth dynamics of such extended NWs, growth was performed at two additional growth times (1 and 1.5 h) to capture the evolution in NW length and diameter. The SEM images in Fig. 1(b) and corresponding NW length and diameter evolution in Fig. 1(c) reveal that the axial growth rate increases rapidly and superlinearly with time, while the radial rate is much smaller and decreases slightly as growth proceeds. These characteristics mimic recent observations of undoped GaAs [28,32] and GaAsSb NWs [28], as well as of InAs-based [33,34] and III-N NWs [35], pointing to a universal behavior that governs the catalyst-free VS growth process. Specifically, the superlinear increase in NW length with time can be understood by the continually increasing sidewall surface area that increases the collection of impinging atoms which diffuse to the axial growth front [28,32–36]. Once the length of the NW exceeds the sidewall diffusion length, superlinear growth ceases and growth transitions towards sublinear dynamics [36]. Here, the Sb flux maintains the superlinear growth throughout the investigated range of growth times.

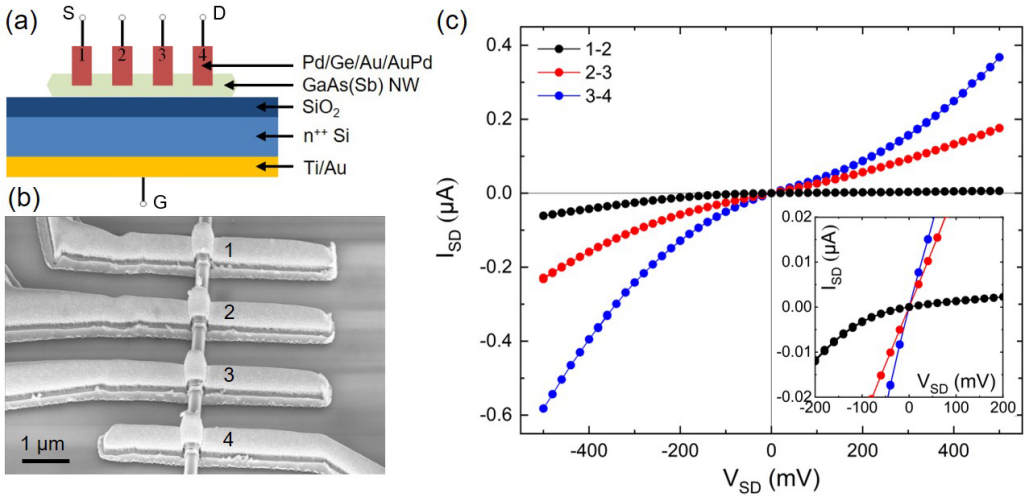

FIG. 2. (a) Schematic illustration and (b) SEM image of as-fabricated back-gate NW-FET containing a total of four equidistant (Pd/Ge/Au/AuPd) metal contacts as source and drain contacts; the n^{++} Si substrate serves as global back gate. (c) *I-V* characteristics measured between different contact pairs along the NW after annealing at 300 °C for 90 s (e.g., 1-2: black/near NW tip; 2-3: red/NW center; 3-4: blue/near NW bottom). The inset shows the respective characteristics at lower voltage range (±200 mV).

B. Electrical transport properties

Using the longest NWs from this series, the electrical transport characteristics were assessed by probing the *I-V* and NW-FET characteristics (in back-gate configuration) on single NW devices at room temperature. Hereby, individual GaAs(Sb):Si NWs were drop-casted onto 200-nm SiO_2/n^{++}-Si substrates (i.e., global back gate) and contacted by multiple, evenly spaced electrodes along the NW axis (four contacts separated by 1.3 µm), using electron beam lithography (EBL) and metal evaporation. As metallization a multilayer stack of Pd/Ge/Au/PdAu (50/170/10/800 nm) was employed; a common choice for *n*-type contacts to GaAs NWs [37,38]. Prior to metallization, the NWs were exposed to a solution of $HCl : H_2O$ (1:1) for 30 s to remove the native oxide on the GaAs(Sb) sidewall surfaces. A schematic illustration as well as a corresponding SEM image of a typical contacted NW-FET device is shown in Figs. 2(a) and 2(b). Thermal annealing was used to further improve the contact conductivity (see Supplemental Material, Fig. S1 [39]). While nonannealed contacts exhibited high resistance (∼10 GΩ), thermal annealing above 300 °C reduced the resistance by up to four orders of magnitude to the ∼800 kΩ–100 MΩ range. The observed improvement in conductivity agrees well with previous work using Pd/Ge/Au metal contacts on Si-doped GaAs NWs, and was mediated by the in-diffusion of Ge metal [38]. In this process, the palladium (Pd) serves as a catalyst that promotes the diffusion of Ge to subsurface sites in the GaAs.

Interestingly, the *I-V* characteristics and associated resistance values depend strongly on the location of the probe contacts on the NW. This is directly illustrated by measurements in two-terminal (2T) configuration between adjacent contact pairs (one acting as source, the other as drain) at different sections along the NW. As shown in Fig. 2(c), contact pairs 1-2, 2-3, and 3-4 arranged from the NW tip towards the NW bottom yield nonlinear *I-V* curves with quite different levels of nonlinearity. Concurrently, lower currents are measured for contacts closer to the NW tip compared to those towards the bottom of the NW. This behavior is consistent in all investigated NWs from this sample (total of 17 NWs measured, with additional examples shown in the Supplemental Material, Fig. S2 [39]). Concomitant with the decrease in conductivity (increase in resistivity) towards the NW tip, the *I-V* curves show increasing nonlinearity. These rectifying characteristics resemble those of back-to-back Schottky contacts and are not surprising given the typical Schottky barrier heights of the employed metals interfacing the GaAs NW sidewalls (barrier heights of ∼0.7–0.9 eV on GaAs(110) for Pd/Au) [40]. A similar spatially varying nonlinearity in the *I-V* characteristics was recently observed in intrinsically doped Si NWs [41] and Te-doped GaAs NWs [42] and was attributed to doping gradients along the NW.

The high device resistance and strong rectifying behavior near the NW tip observed in our NW devices is consistent with current transport in the limit of reduced doping concentration. In such regime, one expects thermionic emission (TE) to govern the current transport across the barrier at the metal/NW interface, resulting inevitably in highly asymmetric Schottky diode behavior [inset, Fig. 2(c)] [42,43]. Moving towards the bottom of the NW, the Schottky barrier is obviously reduced, as the *I-V*'s asymmetry is weakened and a lower device resistance is observed (cf. Supplemental Material, Fig. S2 [39]). The *I-V* characteristics become more linear as field emission begins to dominate TE once the doping concentration is sufficiently high [42,43]. We further note that over the applied bias range (±500 mV), no space charge limited transport was observed in any of the device sections along the NW (see double-logarithmic *I-V* plots in the Supplemental Material, Fig. S3 [39], and references therein [44,45]). This suggests that relatively high doping concentrations (that are much higher than the density of carriers injected via the contacts) prevail in all parts of the NW [44,45].

Further insights into the spatially variant transport characteristics are revealed from 2T-NW-FET measurements

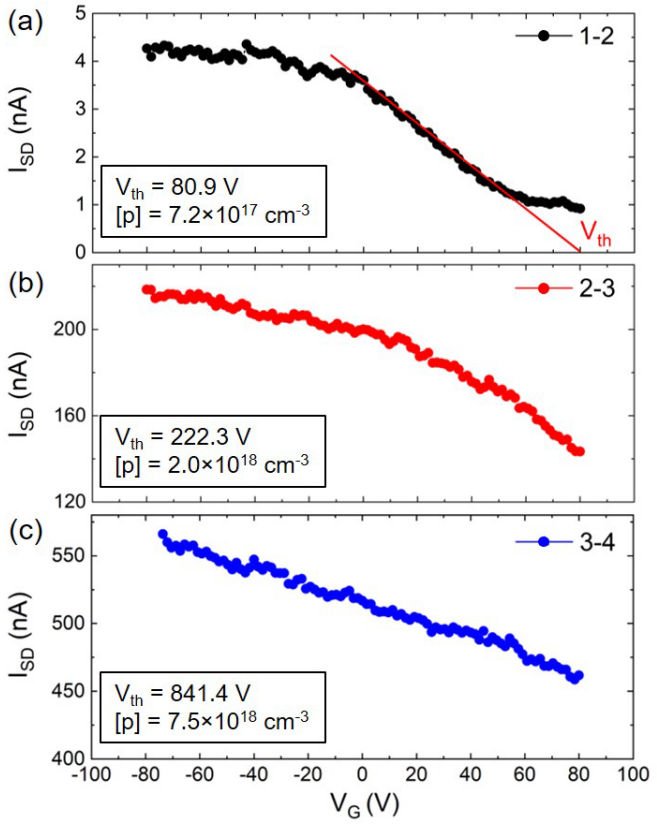

FIG. 3. I_{SD}-V_G transfer characteristics of a back-gated NW-FET under fixed $V_{SD} = 0.5$ V, for three different source-drain contact pairs along the NW: (a) region near the NW tip (1-2), (b) center region (2-3), and (c) bottom region (3-4). The turn-on threshold voltage V_{th} is determined from linear regression of the transconductance [linear drop of the I-V curve; see red line in (a)] and its intersect with the V_G axis. The resulting threshold voltages and estimated p-type carrier concentrations are given in the panel of each respective figure.

performed under a global back gate at room temperature. During these measurements, a constant source-drain voltage ($V_{SD} = 0.5$ V) and variable gate voltage (V_G) was applied to the top Pd/Ge/Au/AuPd contacts and the heavily doped Si substrate, respectively. Given the fact that NW-FET characteristics are very sensitive to the near-surface properties and typically exhibit large hysteresis due to surface states [46,47], the I_{SD}-V_G characteristics presented in the following refer to sweeps in the reverse voltage direction for V_G, for the sake of consistency. Full sweeps and associated hysteresis data are also shown in the Supplemental Material (Fig. S4 [39]). Figure 3 shows the resulting transfer characteristics for the different contact pairs from a typical NW-FET over a gate voltage range from +80 to −80 V. All I_{SD}-V_G curves show a consistent trend that the NW-FET is in an on state (high current) at negative gate bias, while positive gate bias depletes the carrier density. These features are typical characteristics of a p-type NW-FET, implying an inversion of the supposedly n-type behavior of the Si-doped GaAs(Sb) NW. The observation of p-type conduction further means that specific regions with high excess hole densities are present, presumably in the surface region, which fully compensate the electrons in the NW. We anticipate that either surface doping via surface states may cause such hole accumulation at the NW surface [46], or as we point out below, Si dopant induced changes in the surface conductivity due to the strong amphoteric behavior of Si dopants in GaAs.

Before further discussing the origins of these intriguing features, we emphasize that the NW-FET characteristics reveal the same trends in conductivity along the NW axis, as found in Fig. 2. Close to the NW tip, the current through the device is relatively small (few nanoamperes), while the device exhibits clear pinch-off for positive gate bias. In contrast, regions towards the bottom of the NW show increasingly higher current (several hundred nanoamperes), but the carrier density is much harder to deplete by the gate and pinch-off is approached only under exceedingly large gate bias. Such behavior is typical in NWs with very high doping density, which makes gating efficiency from the n^{++}-Si back gate quite inferior compared to NWs with lower doping density, as recently also found for p-type (Be-doped) GaAs NWs [48].

To account for these differences, one can examine estimates of the carrier density in the different sections of the NW-FET by fitting the transconductance, i.e., linear part of the I_{SD}-V_G curves. From the extrapolation of the fits to the intersect with the V_G axis, the turn-on threshold voltage V_{th} can be derived [see Fig. 3(a)]. V_{th} is a useful metric that is linked to the carrier density (n) in the NW transport channel, via the relationship $n = C_G \times V_{th}/(e \times l \times A)$ [46–49]. Here, C_G is the gate capacitance, that is estimated from the widely used metal plate capacitor model [50], while l and A are the length and cross-sectional area of the NW channel (as measured by SEM). For example, an extracted V_{th} of 80.9 V for contact pair 1-2 [Fig. 3(a)] yields a p-type carrier concentration of 7.2×10^{17} cm^{-3}. Performing a similar analysis for the other contact pairs 2-3 and 3-4 gives an estimated p-type carrier concentration of 2.0×10^{18} cm^{-3} and 7.5×10^{18} cm^{-3}, respectively. We emphasize that this variation in estimated carrier concentration gives a meaningful overall trend along the NW, but the absolute values in carrier density have to be treated with care. This is because the gate capacitance is a parameter that relies on a simplified analytical expression [50], and neglects the influence by surface states [51]. Nevertheless, from our NW-FET data it is valid to state that the carrier/dopant concentration increases towards the bottom of the NW, exhibiting higher p-type conduction as opposed to the NW tip.

C. Atom probe tomography

To elucidate the origins of the spatial gradient in carrier conductivity and further identify the cause of the p-type behavior, local electrode APT and resonant Raman-scattering experiments were performed on the Si-doped GaAs(Sb) NWs. For the APT analysis, specimens were prepared by picking and welding individual NWs onto tungsten (W) probe tips using a dedicated NW-reference sample grown to an average length (diameter) of ∼3.8 μm (∼130 nm), that contains a thin AlGaAs/GaAs surface passivation layer. Since a single APT run cannot probe the entirety of a several micrometer-long NW, NWs were mounted in two different orientations on the W tip: with the tip upward to probe the top region of the NW and with the tip downward to characterize the bottom section

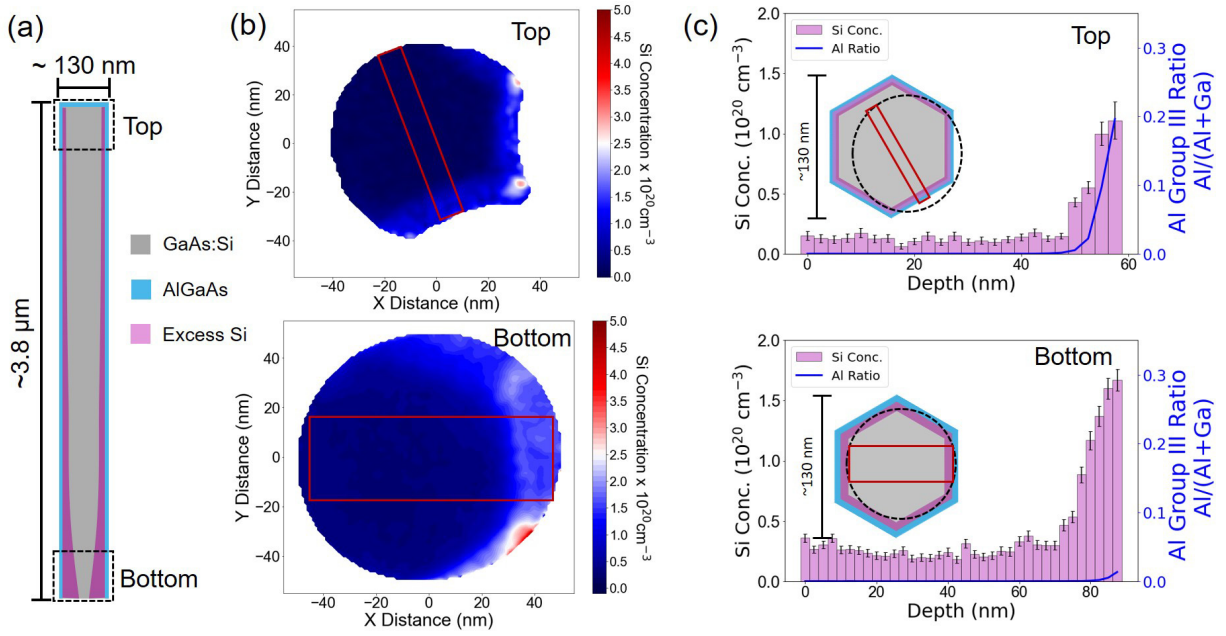

FIG. 4. (a) Side view schematic of the nanowire cross section showing the GaAs:Si core (gray), the AlGaAs shell (blue), and excess Si doping (pink). (b),(c) End view of Si concentration across the diameter shown as (b) 2D contour plots and (c) 1D profiles along the long axis of the red rectangles, averaged over the short axis. Upper (lower) panels refer to cross sections in the top (bottom) regions of the nanowire demarcated by the dashed boxes in (a). Insets in (c) show end view schematics; dashed black circles mark the region captured by the APT detector. The increase in Al mole fraction [blue plots in (c)] indicates the onset of the AlGaAs shell.

of the NW. Further details about specimen preparation as well as specifics of APT experiments can be found elsewhere [52]. Figure 4(a) shows a schematic of the NWs used for APT analysis designation of the top and bottom sections. Figures 4(b) and 4(c) show the Si distribution as (b) two-dimensional (2D) contour plots and (c) radial concentration profiles recorded over regions of interest (ROIs) indicated by red rectangles. The inset end view schematics in Fig. 4(c) indicate the region of the nanowire captured by the APT detector (dashed black circle). Although the field of view does not encompass the entire nanowire, the hexagonal faceting is reflected in the contour plots, providing a point of reference for plots of the Si concentration from the center of the NW through the outer AlGaAs shell. We note that the apparent curvature of facets in the upper plot of Fig. 4(b) results from ion trajectory aberrations, as discussed elsewhere [53], and that the observed asymmetry arises when the nanowire axis is not perfectly parallel to the detector axis. The onset of the AlGaAs shell can be identified by the increase in Al concentration [Fig. 4(c), blue lines]; the end view 2D contour plot of Al is shown in the Supplemental Material (Fig. S5 [39]). The ROIs selected in Fig. 4(b) to plot in Fig. 4(c) were chosen to be perpendicular to the {1–10} facets of the NW. The vertices between facet corners were excluded from the ROIs as the Si concentration is locally enhanced [bright red regions in Fig. 4(b)] by the presence of {112} nanofacets in similar NWs [30].

The APT data provide important insights into the Si distribution. First, the concentration in the center of the NW is uniform over most of the diameter, but is higher at the bottom of the nanowire. The Si concentration at the top is $\sim 1.3 \times 10^{19}$ cm^{-3} as we reported in Ref. [24], but is approximately twofold higher ($\sim 2.2 \times 10^{19}$ cm^{-3}) in the bottom region. Both concentrations exceed the minimum detection limit of $\sim 4 \times 10^{18}$ cm^{-3} for these data sets. This difference in dopant distribution between the top and bottom reflects the nonlinearly increasing growth rate of the NW over time (cf. Fig. 1), which is governed by the collection and diffusion of Ga adatoms to the growth front [28]. Note that according to Fig. 1(c), the average growth rate (approximated by NW length divided by growth time) is more than 3 µm/h for NWs exceeding lengths of >4 µm, while it is up to only half of that rate within the first 2 µm of growth. Hence, the lower growth rate in the earlier stages naturally induces larger dopant incorporation per time unit, and this difference correlates quantitatively fairly well.

An even more striking nonuniformity in the Si dopant distribution is found in the radial direction. As obvious from Fig. 4(c), the near-surface region of the GaAs(Sb) NW exhibits a drastic increase in the Si concentration by up to an order of magnitude close to the interface to the adjacent AlGaAs marker layer. This Si enrichment is found to be higher and more extended in the bottom part of the NW, reaching a concentration as high as [Si] $\sim 1.5 \times 10^{20}$ cm^{-3} and a width that spreads over 10 nm into the NW. By contrast, in the top part of the NW the enriched layer is much thinner (less than 5 nm) and exhibits only up to [Si] $\sim 0.5 \times 10^{20}$ cm^{-3}, i.e., a factor of ~3 lower Si concentration, in a region with comparable Al molar concentration as the bottom. Similar Si enrichment on the NW sidewall surfaces was recently also observed in catalyst-free Si-doped InAs NWs and explained in the framework of growth kinetics and thermodynamics [30]. From kinetics this can be mainly understood by the simultaneous sidewall growth taking place under the vapor-solid SAE process, with growth rates occurring much slower

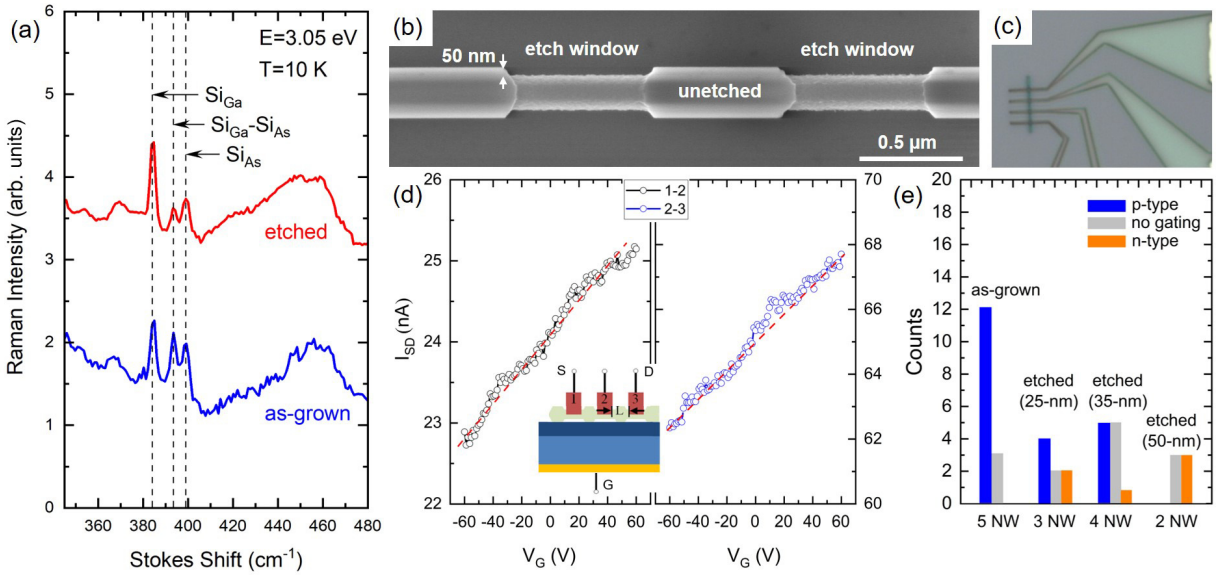

FIG. 5. (a) Raman spectra of the local vibrational modes in the Si-doped GaAs(Sb) NWs recorded for the as-grown sample (blue data) and for NWs etched by citric acid solution to remove the outer ∼15 nm of the NW surface (red data). The spectra are normalized with respect to the second-order phonon scattering feature of the GaAs host crystal at 460 cm^{-1}. (b) SEM image of a NW test structure showing the removal of NW material and reduction of the NW diameter by etching in dedicated windows. (c) Recessed S/D contacts are defined on the etched windows to realize back-gated NW-FETs. (d) Corresponding I_{SD}-V_G transfer curves with *n*-type behavior measured on two contact pairs on the same NW ($V_{SD} = 0.5$ V). (e) Histogram of typical distribution of *p*- vs *n*-type conductive behavior obtained from NW-FET measurements performed on several NWs and multiple contact pairs; as-grown NWs exhibit exclusive *p*-type nature, while NWs with etched recess junctions (depths of ∼25–50 nm) also reveal *n*-type behavior.

radially compared to axial growth [cf. Fig. 1(c)]. Hence, the increase in Si concentration observed at the perimeter of the contour plots in Fig. 4(b) reflects the growth interface, i.e., the {110} NW sidewall facets. The doping enrichment itself can further induce thermodynamic changes of the surface structure; for example, precipitation of Si-rich phases that modify surface reconstruction and surface strain as found in planar III-V semiconductor surfaces as well [54]. Moreover, the observation of Si enrichment on GaAs NW surfaces is also supported by first-principles calculations, suggesting that Si dopants either substitute for surface atoms due to favorable segregation energies or get trapped at subsurface sites [55].

D. Resonant Raman scattering

Resonant Raman scattering was further used as a sensitive technique to probe the lattice site occupancy of Si dopants in the GaAs(Sb) NWs, and evaluate the nature of the near-surface conductivity. Hereby, the scattering experiments were performed at 10 K in backscattering geometry on the same as-grown Si-doped GaAs(Sb) as depicted in Fig. 1(a). Similar to previous studies [17,22,24], excitation via a diode laser was employed at a photon energy of 3.05 eV, which is in resonance with the E_1 gap of GaAs [17], and which in addition limits the probing depth to only ∼10 nm [17,22]. The limited penetration depth precludes the use of an AlGaAs/GaAs passivation layer, and therefore is directly probing the prevalent doping characteristics in the NW sidewall surfaces. However, due to the generally low signal intensity of the Si-related local vibrational modes (LVMs), the entire NW array was probed, thus providing no further spatial differentiation between the bottom and top of the NWs.

The resulting Raman spectrum of the as-grown NW array is depicted in Fig. 5(a) (blue data), illustrating the presence of three dominant LVMs that reveal the respective site occupancies of the Si dopants: Si on Ga sites (donors, 383 cm^{-1}), on As sites (acceptors, 399 cm^{-1}), and as Si_{Ga}-Si_{As} pair complexes (394 cm^{-1}) [53]. Note that the detection limit for the Si LVMs is $\sim 10^{18}$ cm^{-3} [56,57], suggesting that the respective concentrations of all three occupancy sites are well above this level. In fact, the similar relative signal strengths of all Si LVMs are fully analogous to previous data of heavily Si-doped GaAs NWs [17,24], where not only the intended (i.e., *n*-type) Ga sites are occupied, but to a substantial degree the As sites as well as Si_{Ga}-Si_{As} pair complexes. Both Si_{As} and Si_{Ga}-Si_{As} pair complexes induce strong compensation and even *p*-type behavior [58,59], demonstrating the strong amphoteric nature of Si dopants. Such Si_{Ga}-Si_{As} pairs are also known to induce potential fluctuations in the host crystal lattice [60,61], as seen in prior optical emission studies [22], and these further affect carrier transport, primarily carrier mobility, as observed in excessively Si-doped III-V NWs [30]. In addition, the Si_{Ga}-Si_{As} pair complexes also give rise to the formation of Ga vacancies (V_{Ga}) [62], which are acceptorlike point defects that further contribute to enhancing *p*-type conductivity in GaAs [63].

The Raman-scattering data therefore provide direct support for the measured *p*-type NW-FET characteristics (cf. Fig. 3), given that both methods are very surface sensitive. The *p*-type surface conductivity is also expected from the exceedingly high Si dopant concentrations found in the surface

layer measured by APT ([Si] > 10^{19}–10^{20} cm^{-3}). Indeed, at such high Si doping densities incorporating on (110) GaAs surfaces (the case of NW-sidewall facets), distinct *p*-type conduction has been obtained before in planar layers, especially under conditions of high temperature growth [64,65] as employed here. On the other hand, under these conditions, incorporation of Si via the (111)B growth facet is expected to produce *n*-type behavior. This is well known from studies on planar (111)B reference layers [66], and further seen in our Raman data. Note, the probing depth of ∼10 nm in the Raman-scattering experiments slightly exceeds the width of the Si-enriched (*p*-type) surface layer measured in APT. Hence, it is not surprising that the LVM spectra show a distinct Si_{Ga} LVM signal as well, since the anticipated *n*-type region right below the Si-enriched *p*-type layer is also captured to a certain extent. Thereby, one has to consider that the Raman probing depth is defined via the exponential decay of light intensity (absorption length defined by intensity reduction to 1/*e* of its initial value) rather than by an abrupt cutoff.

E. Controlled removal of NW surface region

To verify this, and further attempt to retrieve the *n*-type conduction of the bulk part of the NW, the entire as-grown NW array was wet-chemically etched in a diluted citric acid (CA) solution (CA : H_2O_2 : H_2O with 1:3:200 volume ratio) [67]. The selected dilution ratio provides a slow etching rate of 0.8 nm/s that enables accurate control of etching depth with ±2 nm precision, as found from etch calibration studies. By adjusting the etching time, an ∼20-nm thin layer was removed from the NW-sidewall surfaces, reducing the originally ∼295-nm-thick GaAs(Sb):Si NW to a final diameter of ∼255 nm. Subsequent resonant Raman measurements were performed under identical conditions, resulting in a remarkable change in the relative signal ratios of the Si LVMs [see Fig. 5(a), red data]. Compared to the as-grown, untreated NWs, the occupancy of Si_{As} and Si_{Ga}-Si_{As} pair complexes is substantially reduced, leaving the signature of the Si_{Ga} LVM as the most dominant signal. Also, the relative signal intensity of the Si_{Ga} LVM is increased (factor of ∼1.7) in the etched NW, compared to that of the as-grown NW. These observations provide evidence for the effective removal of the Si-enriched surface layer, and with that the region of dominant Si-induced acceptor sites.

NW-FET devices were further fabricated from wet-chemically etched NWs, by selectively removing material from the NW surface in dedicated etch windows that are created by masking the NW in-between windows using EBL. Thereby, the etch windows define recess regions for source (S) and drain (D) contacts, whereas the regions between adjacent contacts remain largely unetched (except for some extended etching due to the isotropic nature of the CA solution). This was necessary in order to limit the formation of excess surface state densities in the NW channel, as etching results in surface roughening and the creation of larger numbers of dangling bonds [46]. Figure 5(b) illustrates the controlled local removal of NW material within the respective etch windows on a test structure prior to contact formation. The image confirms the desired uniformity in etching on all side facets, reducing the NW on each facet by ∼50 nm in this case. A similar NW-FET device layout, as used before, with either three or four recessed S-D contacts was employed [Figs. 5(c) and 5(d)] to measure the *I*-*V* characteristics under identical conditions.

Figure 5(d) shows an example of the obtained NW-FET transfer characteristics under the applied back gate for two separate contact pairs placed along different sections on the NW. Here, the data corresponds to sweeps in the forward voltage direction of V_G (full sweeps and hysteresis behavior are shown in the Supplemental Material, Fig. S6 [39]). Despite the overall weak gate modulation observed in these devices—as expected for highly doped NWs in back-gate geometry [30,48,51]—the I_{SD}-V_G transfer characteristics imply *n*-type conductive behavior for both contact pairs, evidenced by the lowered drain current towards negative gate voltages. This indicates that by the etching of the Si-enriched surface region and subsequent contact annealing, recovery of the anticipated *n*-type nature of the Si-doped GaAs(Sb) seems feasible.

The inversion from *p*-type characteristics as seen in devices from as-grown NWs (cf. Fig. 3) is, however, not universally observed in all measured NWs treated by CA etching. Figure 5(e) summarizes the variation of the observed transfer characteristics obtained from several NW-FET devices, which were constructed from NWs etched under different times (i.e., different etch depth) and compared to unetched, as-grown NWs. A set of typical transfer curves from this analysis is further illustrated in the Supplemental Material (Figs. S6 and S7 [39]). The histogram shows that as-grown NWs exhibit exclusively *p*-type conduction, and some devices have no gating action at all. This very distinct characteristic disappears for etched NWs, as the likelihood for *n*-type behavior becomes more prevalent. Yet, several devices fabricated within the same process run still show certain variation in conductivity, and the underlying reasons are not fully clear at the moment. It could be related to residual amphoteric behavior or variable densities of surface states amongst different NWs (or even in different sections of the same NW), which influence the relative sensitivity of the gate coupling [46,48]. Such variation may be induced, for example, by the observed gradient in the Si dopant incorporation along the NW as well as by nonuniformities in etching. Alternatively, contact formation upon annealing, and associated in-diffusion of contact metal may also play a critical role in how the final transport channel is defined. Indeed, we recognize some correlation between *n*- vs *p*-type conduction and the device resistance extracted from the I_{SD}-V_{SD} characteristics. Devices showing *n*-type behavior have, by trend, lower contact resistance (∼400 kΩ to a few tens of megaohms), while *p*-type devices exhibit typically higher resistances (>50 MΩ). Similarly, NW-FETs with recessed S/D junctions were also measured before annealing of contacts, resulting in high contact resistance (greater than a few hundred megaohms) and only *p*-type conduction, respectively. This suggests that by the absence of in-diffusion of the contact metal, large Schottky barrier depletion widths remain, which limit the efficient electron tunneling towards the *n* region for the formation of lower-resistance contacts. In turn, this confirms that contact annealing seems to be key for realizing *n*-type conduction in these NWs.

III. CONCLUSIONS

In conclusion, we demonstrated the interplay between spatial nonuniformities in Si dopant incorporation and the electrical transport characteristics of heavily doped, catalyst-free GaAs(Sb) NWs grown by selective area epitaxy on silicon. Highly nonlinear axial growth rates were found to be responsible for an approximately twofold change in Si dopant concentration along the NW, while even stronger Si dopant segregation was observed in the radial direction, yielding a several-nanometer-thick Si-enriched layer at the GaAs(Sb) sidewall surfaces. Due to the strong amphoteric nature of Si under such excess Si enrichment, NW-FET measurements, which are very sensitive to the near-surface regions, yielded *p*-type conductive behavior and further revealed a spatial gradient in the *I*-*V* characteristics along the NW that reflects the decreasing Si dopant concentration from the bottom to the top of the NW. Additional wet-chemical etching studies demonstrated successful removal of the Si-enriched *p*-type surface layer and the possibility for recovery of the intended *n*-type conduction, as shown by resonant Raman-scattering experiments and NW-FET characterization. These findings provide useful knowledge that motivates future work towards improved control of Si dopant incorporation and the realization of unambiguous *n*-type conductive transport in associated devices. For example, adjustments of the V/III ratio (i.e., growth rate) during NW growth could deliver a constant axial rate throughout [68] to inhibit the formation of axial dopant gradients, while lower, moderate doping may further limit the formation of excess Si enrichment in the radial direction. Such relationships with growth rate and Si-doping induced changes in free carrier density could also be revealed by probing coupled phonon-plasmon modes in spatially resolved Raman spectroscopy, as recently demonstrated [42]. In addition, establishing pure *n*-type transport in the NW via NW-FET devices will call for added strategies in contact formation (e.g., through optimized etching/annealing towards lower contact resistances) and improvement in gate coupling. As gate coupling is generally very challenging in highly doped NWs, improvements could be rendered possible either by adding top gates or using entirely different, e.g., non-metal-oxide type gates [48].

The data that supports the findings of this study are available within the paper and its Supplemental Material [39].

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