

## Local laser-induced solid-phase recrystallization of phosphorus-implanted Si/SiGe heterostructures for contacts below 4.2 K

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Si/SiGe heterostructures are of high interest for high-mobility transistor and qubit applications, specifically for operations below 4.2 K. In order to optimize parameters such as charge mobility, built-in strain, electrostatic disorder, charge noise, and valley splitting, these heterostructures require Ge concentration profiles close to monolayer precision. Ohmic contacts to undoped heterostructures are usually facilitated by a global annealing step activating implanted dopants, but compromising the carefully engineered layer stack due to atom diffusion and strain relaxation in the active device region. We demonstrate a local laser-based annealing process for recrystallization of ion-implanted contacts in SiGe, greatly reducing the thermal load on the active device area. To quickly adapt this process to the constantly evolving heterostructures, we deploy a calibration procedure based exclusively on optical inspection at room temperature. We measure the electron mobility and contact resistance of laser-annealed Hall bars at temperatures below 4.2 K and obtain values similar or superior to that of a globally annealed reference sample. This highlights the usefulness of laser-based annealing to take full advantage of high-performance Si/SiGe heterostructures.

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### I. INTRODUCTION

The versatility of band and strain engineering within heterostructures makes them compelling candidates for use in cryogenic transistors such as the high-electron-mobility transistor (HEMT) [1,2] and the heterojunction bipolar transistor (HBT) [3–6], as well as for qubit applications [7–11] that benefit from high carrier mobility, low electrostatic disorder, and low electrical noise. These devices often aim to minimize scattering sites and charge noise by utilizing undoped heterostructures [12]. Consequently, they require local doping to generate Ohmic contacts to the semiconductor, e.g., to the buried conduction layer of a Si/SiGe quantum well. However, this necessitates high-temperature annealing steps, approaching or even surpassing the growth temperature. This can lead to atom diffusion and intermixing at the interfaces [13]. In addition, the elevated temperature leads to the propagation of misfit dislocations through the quantum well, reducing the tensile stress and increasing the amount of scatter sites [14].

As local interface fluctuations become increasingly relevant and engineering precision at the atomic scale becomes a requirement [15], global annealing becomes a limitation, as its thermal impact potentially degrades the active region. This is especially relevant for strain-engineered structures such as silicon/silicon germanium (Si/SiGe) grown by molecular beam epitaxy (MBE) [16] as well as qubit devices [15,17–19]

based on Si/SiGe heterostructures. There, sharp interfaces are required for lifting the out-of-plane conduction band minima degeneracy (valley splitting) in the tensile-strained Si quantum well. Recently, Ge concentration profiles with monolayer resolution were introduced into the quantum well to compensate for the inaccessibility of atomistic abrupt changes in alloy concentration [17]. The advantage of having these layers becomes significantly reduced if they are smeared out due to thermally activated diffusion. Insufficient valley splitting is thereby considered the dominant limitation for scaling up Si/SiGe quantum computers, as local minima can lead to fast decoherence channels hampering coherent shuttling and operation at elevated temperature [20–22]. Ohmic contacts are required for these quantum computing applications, the operation temperature of which is below the temperature of liquid helium (4.2 K). This places a lower limit on the annealing temperature, as incomplete ionization, caused by freeze-out [23], has to be accounted for. This is critical as it can lead to a breakdown of conductivity in the contacts, reducing the signal-to-noise ratio and limiting the measurement bandwidth. Insufficient activation can even render the quantum well layer electrically inaccessible altogether.

Recrystallization through solid-phase epitaxy (SPE) in Si starts at temperatures exceeding 550 °C [24]. However, practical constraints on annealing times, coupled with the need to prevent freeze-out, often necessitate to include a global heating step of 700 °C and above in typical processes [25,26]. Laser annealing (LA) was previously studied in ion-implanted Si to improve sheet resistance [27]. It was also proposed as a

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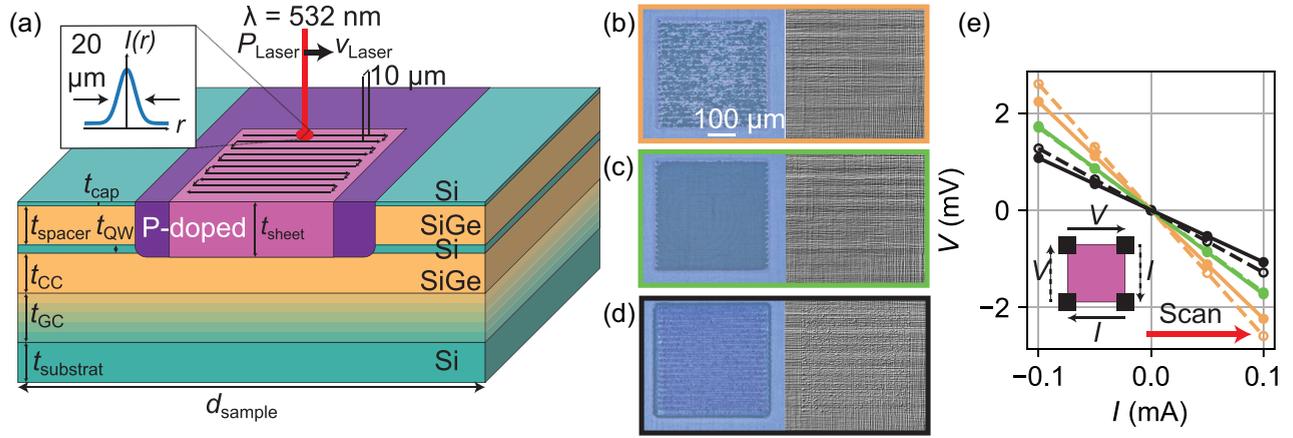


FIG. 1. Laser annealing and process evaluation. (a) Schematic of studied heterostructure (stack detailed in Table I) and laser annealing setup. A cw laser with  $\lambda = 532$  nm is scanned line by line (black line) over the sample and controlled via a shutter to only hit the designated area (pink) inside the implanted regions (purple). The tool allows control of the laser power  $P$ , scan speed  $v$ , and line spacing  $\Delta y$ . (b) Optical inspection (left) and c-DIC image (right) of a  $400 \mu\text{m} \times 400 \mu\text{m}$  square scanned with  $\{2.6 \text{ W}, 25 \text{ mm/s}\}$ , (c)  $\{2.6 \text{ W}, 2.5 \text{ mm/s}\}$ , and (d)  $\{6.2 \text{ W}, 2.5 \text{ mm/s}\}$  on wafer B. (e) Room-temperature current  $I$  versus voltage  $V$  characteristic for the squares shown in panels (b)–(d) (dot colors match frame colors). Data are obtained in van der Pauw geometry (black squares are electrical contacts in inset). Lines are linear least-square fits to the data.  $I$  is measured parallel to the laser scan line (solid dots, solid line) and perpendicular to it (open dots, dashed line) as sketched in the inset.

solution to form surface-localized junctions for monolithically stacked devices to prevent degradation of lower-lying structures [28,29]. Outside of dopant activation, laser annealing was used for relaxing SiGe layers grown on silicon on insulator (SOI) as a virtual substrate for strained Si channels [30] and for frequency tuning of superconducting qubits by local oxide thickness control [31]. However, no study was done on LA activated contacts in Si/SiGe, specifically for cryogenic use below 4.2 K.

In this work, we demonstrate activation of implanted phosphor donors in an undoped Si/SiGe heterostructure by local annealing with a continuous-wave focused laser beam. The area, which is scanned by the laser, makes an excellent Ohmic contact to a buried Si/SiGe quantum well operating down to 1.6 K and our LA process keeps the silicon surface topography intact for further device fabrication. We benchmark the LA performance by gated Si/SiGe Hall bar. The contact resistance and electron mobility are at least equal compared to a globally annealed reference Hall bar. We find that the laser power is the most critical process parameter, which depends on the details of the Si/SiGe heterostructure. We suggest a fast calibration method based on optical inspection after LA. Thus, LA is a viable alternative that can reduce the thermal budget and improve the quality of a Si/SiGe heterostructure in the active region, which is particularly interesting for SiGe quantum chips.

## II. MATERIALS AND METHODS

### A. Samples

All four investigated heterostructures follow the same scheme with differences in layer thicknesses as shown in Fig. 1(a). A  $\text{Si}_{1-x}\text{Ge}_x$  virtual substrate (VS), consisting of a graded-composition (GC) buffer with either stepwise or linearly increasing Ge content up to  $x$  and an additional constant-composition (CC) buffer is deposited onto a Si

substrate. This is followed by the growth of the active thin Si layer on the VS and then a second  $\text{Si}_{1-x}\text{Ge}_x$  spacer layer. The Si layer is tensile strained, since it is thinner than the critical thickness for plastic relaxation. Finally, the spacer is capped by a thin Si layer to prevent direct oxidation of the  $\text{Si}_{1-x}\text{Ge}_x$ . The wafers were grown using MBE or chemical vapor deposition (CVD) and all details of the four wafers (A–D) are summarized in Table I. All wafers were diced into  $10 \text{ mm} \times 10 \text{ mm}$  samples. After an RCA cleaning step (applied to wafers A–C, and wafer D was excluded from this clean as this would have resulted in complete removal of the Si capping layer; for details see Appendix C), all samples were ion implanted by a 20-kV accelerated phosphorus beam with a flux of  $5 \times 10^{15} \text{ cm}^{-2}$  hitting the sample at an angle of  $7^\circ$  to its normal. After annealing, the implanted areas form a conductive sheet. This is used to connect metal contacts on the surface to the two-dimensional electron gas (2DEG) that forms in the strained Si layer. From SRIM 2013 simulations [32] we expect a thickness of this sheet of  $t_{\text{sheet}} = 64 \text{ nm}$ , given by the condition of the concentration of P atoms being

TABLE I. Overview of the layer stack and growth conditions of the studied wafers.

Wafer	A	B	C	D
$x$	0.30	0.33	0.33	0.30
$t_{\text{cap}}$ (nm)	5.0	5.0	5.0	1.5
$t_{\text{spacer}}$ (nm)	30	35	55	45
$t_{\text{QW}}$ (nm)	10	10	10	10
$t_{\text{CC}}$ ( $\mu\text{m}$ )	2.0	1.75	1.75	0.70
$t_{\text{GC}}$ ( $\mu\text{m}$ )	3.0	0.25	0.25	3.75
Grading type	Linear	Step	Step	Linear
$t_{\text{substrate}}$ ( $\mu\text{m}$ )	725	725	725	425
Growth method	CVD	CVD	CVD	MBE

above  $1 \times 10^{20} \text{ cm}^{-3}$ . The maximum concentration is predicted to be 26 nm below the surface.

### B. Setup

LA is conducted by a custom-made MICROTECH Laser-Writer (model LW532). It is equipped with a solid-state continuous-wave  $\lambda = 532 \text{ nm}$  laser with a variable power  $P$  between 0.2 and 8 W. Its wavelength was chosen based on simulations of the heterostructure for high absorption and low transmission and/or reflectivity. The laser is focused down to a spot diameter of  $20 \mu\text{m}$  with a Gaussian profile. The sample is placed on a ceramic chuck mounted on top of a movable  $xy$  stage, the velocity of which can be varied between 0.1 and 25.0 mm/s along its fast axis. Pattern alignment and in-process monitoring are done via a charged-coupled device (CCD) camera positioned within the optical path. For operation, the laser spot is scanned back and forth over the sample along the fast axis with the scan velocity  $v$  and is stepped after each line along the slow axis with a fixed distance  $\Delta y = 10 \mu\text{m}$  as indicated in Fig. 1(a) (for a detailed discussion see Appendix A). To account for the inertia of the stage, the scan starts before the sample area for each line to ensure enough travel distance to reach the set scan velocity. The laser is controlled by a shutter with a reaction time of 10 ms, which blocks the laser during scanning to prevent heating outside the designated areas and transients if laser output power is switched.

### C. Optical and electrical characterization (room temperature)

In the calibration of the laser annealing process, it is essential to monitor the level of recrystallization, alterations in surface topography, and resulting electrical resistance for changing sets of process parameters. These criteria serve as crucial indicators of the success of the annealing step. Ideally, the calibration method should be fast and easily applicable, so that a large parameter space can be covered for each new heterostructure. To this end, it should involve minimal additional fabrication steps or added complexity. To achieve this, we utilize the fact that implantation damage induces a change in color, stemming from the difference in optical properties between crystalline and amorphous semiconductors [33]. Consequently, we can assess the degree of recrystallization by evaluating the extent of color change following the annealing process. This assessment can be done quickly by optical inspection. We examine the impact of LA on the surface topography by circular polarized light–differential interference contrast (c-DIC) [34] imaging. Optical inspection and c-DIC imaging are carried out using a Keyence VK-X3000 laser scanning microscope.

With this characterization in place, we study the dependence of total regrown thickness on laser power  $P$ , the dwell time of the laser (which is inversely related to the scan velocity  $v$ ), and the thermal conductivity or capacity of the surrounding material. For this, we anneal multiple squares with an edge length of  $400 \mu\text{m}$  with different parameter sets  $\{P, v\}$  on samples of each wafer. After LA, optical and c-DIC images are taken under a microscope. Depending on the set of parameters employed, we observe varying degrees

of color change in the annealed areas within the optical images. We cluster these into three categories: For  $\{\text{low } P, \text{ high } v\}$  we observe an inhomogeneous color change as shown in Fig. 1(b) (orange). The color change occurs preferentially in the middle of the scanned line. At this point, the only surface topology we observe in the samples corresponds to the typical cross-hatching pattern commonly found on the surface of Si/SiGe heterostructures [35]. The proportion of changed regions increases with  $\{\text{increasing } P, \text{ decreasing } v\}$  until a homogeneous color change is reached [Fig. 1(c), green], without an observable change in surface topology. When power (velocity) is further increased (decreased), bright spots appear in the optical image toward the middle of the scan line, shown in Fig. 1(d) (black). The spots are also visible in the c-DIC images.

Presumably, the initial temperature in the sample does not exceed the melting point. Therefore, regrowth takes place via SPE from the bottom up and increases in speed according to an Arrhenius equation for higher temperatures [36,37]. Thus, we attribute the inhomogeneous color change to a threshold range, where certain parts of the intensity distribution of the laser are already sufficient to heal the implanted damage over the full depth, while the remaining spots are only partly recrystallized [see Fig. 1(b)]. The homogeneous color change [Fig. 1(c)] indicates then that the entire implanted area has fully healed. Upon further laser power increase, we observe a change in surface topography as indicated by the appearance of the black dots in the c-DIC image [as seen in Fig. 1(d)]. We speculate that this indicates local exceeding of the heterostructure's melting point of approximately  $1220^\circ\text{C}$  [38]. At this point, a liquid phase locally develops, the volume of which extends further down as the LA time is increased [36]. After cooling below the melting point, the liquid phase crystallizes, with the underlying semiconductor serving as a seed. We aim not to change the surface during the process in order to keep further fabrication steps consistent. Consequently, we dismiss parameter sets where optical inspection indicates surface degradation.

In order to qualify the interpretation of optical inspection, we evaluate the electrical conductivity of the annealed areas first at 300 K. We measure the electrical resistivity of the three annealed squares in a four-probe van der Pauw (vdP) geometry at room temperature (RT) as shown color coded in Fig. 1(e). To this end we evaporate 150-nm-thick aluminum contact pads onto the corners of each square. We contact the four pads of a square with a needle probe station in which the needles are connected to a source measurement unit (SMU) via a multiplexer. The multiplexer allows us to switch the assignment of the current and voltage ports of the SMU to the needles. We conduct the experiment twice, once along the fast scan direction of the laser beam (indicated by solid dots and solid line) and once perpendicular to it (indicated by open dots and dashed line), and apply a linear fit to each data set. We observe a linear and thus Ohmic behavior for all measured squares and orientations. The extracted resistance decreases from the inhomogeneous (orange) to the homogeneous (green) to the surface degradation case (black). Notably, for the inhomogeneous and degradation squares, the resistance displays a dependence on the measurement orientation, with lower resistances observed when measured

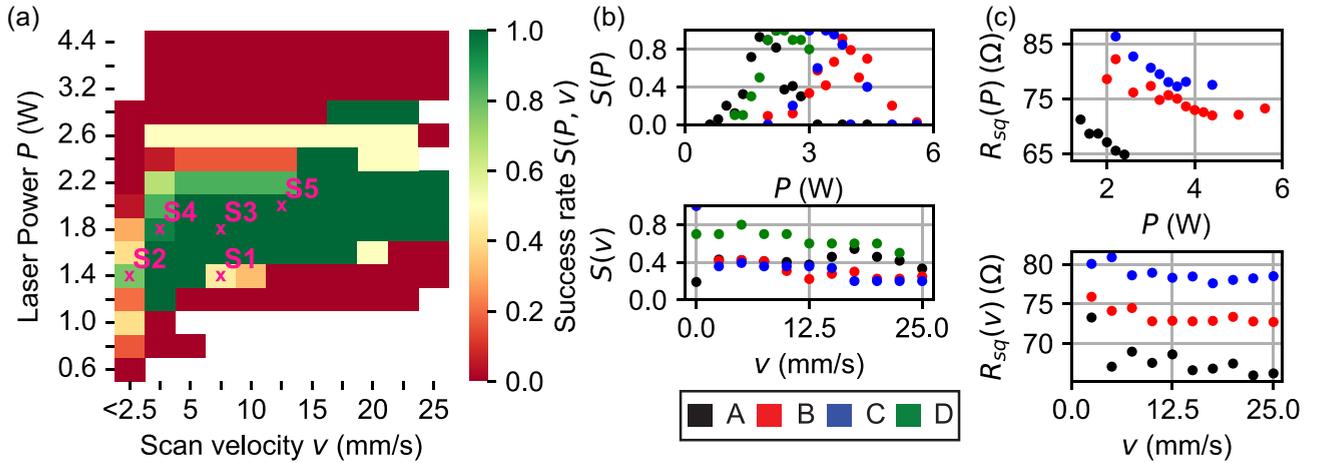


FIG. 2. Process calibration. (a) Map of success rate  $S$  as a function of parameter set  $\{P, v\}$  for wafer A. A successful parameter set is defined as exhibiting a homogeneous color change and no indication of surface morphology change. (b) Projected success rates  $S(P)$  (top) and  $S(v)$  (bottom) obtained by averaging along the  $v$  or  $P$  axis for wafers A–D (color coded). (c) Projected sheet resistances  $R_{sq}(P)$  (top) and  $R_{sq}(v)$  (bottom) of successfully annealed regions obtained by vdP measurements at 300 K.

along the laser scan line. This distinction is not observed in the case of the homogeneous sample. In the case of surface degradation, we cannot exclude small contributions to the electrical contacts caused by the increased surface roughness [Fig. 1(d)], which is not present in the inhomogeneous or homogeneous squares [Figs. 1(b) and 1(c)] and thus not relevant for these samples. Note that the decline in resistance in Fig. 1(e) matches our expectations, considering that the ratio of electrically active dopants has been observed to increase with temperature [39] and our optical study suggests that the temperature increases between each of the squares. Moreover, this temperature variation becomes more pronounced if the sample surpasses the melting point, as we assume in the surface degradation square. The reason for this is that the diffusion rate in the liquid phase significantly exceeds that in the solid phase [37]. This can explain the observed preferential direction of the resistance. Due to the Gaussian intensity profile of the laser, the temperature is highest toward the center of the laser spot that moves along the scan line. Conversely, perpendicular to the scan direction, the temperature minimum is found between two scan lines. In the inhomogeneous case, this implies the presence of remaining narrow amorphous regions which enhance the resistance along the current direction. On the other hand, in the surface degradation case, the melting predominantly occurs toward the laser center, generating areas with a high activation ratio interleaved with unmolten regions perpendicular to the scan line. In contrast, the homogeneous case achieves a consistent activation ratio without the presence of any amorphous or molten resistance elements. The electrical measurements validate our interpretation of the optical inspection in terms of the stage of recrystallization.

As such, optical inspection provides a rapid and effective means of assessing the feasibility of a parameter set  $\{P, v\}$  for a given heterostructure. We define a successful parameter set by the presence of a uniform color change without any discernible surface morphology alterations. This evaluation technique enables efficient calibration of the LA process for each new heterostructure.

### III. CALIBRATION RESULTS

Building upon the efficient determination of successful parameter sets through optical inspection, we focus on investigating how these parameter sets are influenced by changes in the heterostructure. This investigation is critical, as continuous optimization of various aspects of the Si/SiGe layer stacks necessitates adaptations in the laser annealing process. We systematically vary laser power  $P$  and scan velocity  $v$  to anneal squares onto samples of all four wafers and optically inspect the results. Several parameter sets are studied multiple times to assess process stability. We define the success rate  $S$  for a given parameter set  $\{P, v\}$  as the number of successful squares in relation to the total number of annealed squares. A map of  $S$  is shown for wafer A in Fig. 2(a). The maps for wafers B–D are shown in Appendix B. A parameter window with high success rates is observed (green area). This high-success parameter window is narrow in  $P$  and broad in  $v$ . Thus, the laser power is a more critical parameter for LA of wafer A. To compare the successful parameter windows among the wafers, we calculate projections of average success rates  $S(P)$  [ $S(v)$ ] along the  $v(P)$  axis, given by

$$S(i) = \frac{1}{N_j} \sum_j S(P, v) \text{ with } i \neq j \in [v, P], \quad (1)$$

where  $N_j$  are the number of tested parameter sets along each projection. The results are shown in Fig. 2(b). The  $P$  projection (top) shows a dependence of the success rate on laser power visible as a peak. The position of this peak varies for the four wafers studied, with a maximum distance between wafers A and B. The success rate maximum of wafer C is closer to the B peak and the D peak close to the one of A. The  $v$  projection (bottom) shows no systematic change of  $S(v)$  for all four wafers, which confirms that the scanning velocity is uncritical for all considered samples. The laser power, however, needs recalibration for all wafers. Note that we observed negligible change in the reflection coefficient at the laser wavelength among samples.

TABLE II. Minimum sheet resistances that are achieved with a successful parameter set for each wafer examined. Corresponding values for power  $P$  and scanning velocity  $v$  are given.

Wafer	$R_{\text{sq,min}} (\Omega)$	$P$ (W)	$v$ (mm/s)
A	64.4	2.4	15.0
B	70.1	4.4	25.0
C	74.4	3.6	2.5

For wafers A, B, and C, we conduct vdP measurements within each successfully annealed region. In Fig. 2(c), sheet resistance projections  $R_{\text{sq}}(P)$  [ $R_{\text{sq}}(v)$ ], obtained by employing the previously described method along  $v$  ( $P$ ), are shown. We observe a trend of decreasing resistance projection for increasing  $P$ , while the projections are constant in  $v$ . We obtain minimum sheet resistances of  $R_{\text{sq,A}} = 64.4 \Omega$ ,  $R_{\text{sq,B}} = 70.1 \Omega$ , and  $R_{\text{sq,C}} = 74.4 \Omega$ .

We compare the peak positions in  $S(P)$  for all four wafers with respect to the differences in layer thicknesses. We observe a grouping of wafers A and D, which were grown by different methods (CVD and MBE) and characterized by a substantial difference in underlying Si substrate thickness (725 and 425  $\mu\text{m}$ ). If the Si substrate thickness had a notable impact, this dissimilarity should dominate all other effects. Since this phenomenon is not evident in our observations, we conclude that even the thinner Si substrate serves as an adequate heat sink during the scanning process. This finding holds practical significance since Si substrate thickness is mainly linked to wafer size, a parameter that is typically fixed by the growing tools used and not easily modified. In terms of similarities, both wafers A and D share the characteristic of having a linearly graded buffer, while wafers B and C have a stepwise graded buffer. Additionally, when considering the combined thickness of the VS (including the GC and CC buffers), wafers A and D exhibit a thickness approximately twice that of wafers B and C. Upon examining the layer structures situated above the virtual substrate, we observe no systematic correlation between power requirements and layer thicknesses among these wafers. From these observations, we can deduce that the power requirement is predominantly influenced by the specifics of the VS. SiGe has a smaller heat conductivity [40] compared to Si. We explain the power dependence by the fact that the VS acts as a thermal resistance for the dissipation of the heat supplied by the laser. With increasing thickness, the heat flow to the substrate is reduced. Therefore, for a heterostructure with a thicker VS, a lower heat input, which is given by the laser power, is required to achieve the same surface temperature and thus regrowth rate. The grading of the VS plays a pivotal role in shaping the quality of the inter-VS interfaces and the distribution of strain within the structure [41], which can further modify thermal conductance. We attribute the further reduction of sheet resistance inside the successful parameter window to an increase in activation ratio with larger temperatures.

By employing fast optical calibration, we can establish a parameter range for each wafer, ensuring reliable activation. The minimum sheet resistances for each wafer as well as the used laser scan parameters are summarized in Table II.

The ability to quickly adapt the laser annealing process to different heterostructures is advantageous, especially given the ongoing optimization efforts in Si/SiGe quantum technologies. Our findings reveal that the optimal laser power can vary by nearly a factor of 2 between different wafers (A and B), although their upper layer stacks forming the quantum wells are nearly equivalent. With this calibration procedure in place, we can efficiently adapt the laser annealing process to accommodate each new iteration, keeping up with the progress in heterostructure design.

#### IV. LIQUID HELIUM CHARACTERIZATION

In the next step, we investigate the performance of LA contacts to undoped Si/SiGe quantum wells at 1.6 and 4.2 K. We select five parameter sets (S1–S5) from the high-success-rate window of wafer A [see Fig. 2(a)] and employ them to fabricate Hall bar structures. As later applications may be sensitive to the extent of which the thermal input is limited to the contact areas, we also study the lateral resolution of the LA process. For this purpose, we define the region to be annealed so that it ends directly at the junction between the implanted and the gated regions, in which carriers are accumulated by a positive gate voltage. In addition, we utilize each parameter set twice and alternate the orientation of the implanted structure with respect to the scan direction, denoted by  $x$  and  $y$  in Fig. 3(a), respectively. The addition of a star (\*) to the parameter name indicates samples where the fast scan axis was oriented along the  $y$  direction. The samples used in this process were implanted following the same recipe as the ones used for calibration. In Fig. 3(a), an optical microscope image captured after the LA treatment shows a homogeneous color change compared to the previous state observed after implantation. The implanted and subsequently annealed areas are shown in yellow at the example of the upper left pair of contacts. Furthermore, we fabricate reference samples from wafer A using a global annealing (GA) process at a temperature of 750  $^{\circ}\text{C}$  for a duration of 30 s under an argon atmosphere. The annealing process is carried out using an Annealsys AS-One rapid thermal processing (RTP) system. After the global annealing, a homogeneous color change and no change in surface morphology was observed. The subsequent fabrication steps are superimposed on the microscope image in different colors for clarity. The black represents the mesa etching step, defining the channel region. The orange signifies the region of metal contact pads that are directly evaporated onto the implanted regions. The red indicates the gate region, which is isolated from the channel and contacts by a deposited gate oxide layer. Each fabrication step outside of annealing was done in parallel on LA and GA samples to ensure comparability. Fabrication details are given in Appendix C.

##### A. Cryogenic contacts

To ensure proper connection of the LA contacts down to the 2DEG, we perform magnetotransport measurements at a temperature of 1.6 K. Details of the measurement setup are given in Appendix D. An exemplary measurement at a gate voltage of  $V_G = 0.6 \text{ V}$  is shown in Fig. 3(b). The structure used was annealed using LA parameter set  $S4^* = \{1.8 \text{ W}$ ,

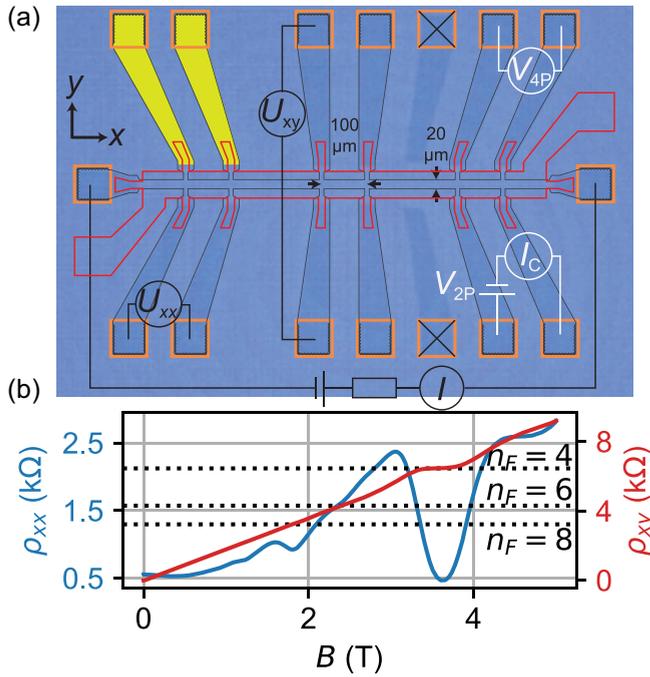


FIG. 3. Hall bar measurements. (a) Optical microscope image after LA of a sample with implanted contacts (shown in yellow as an example) for a Hall bar structure. Subsequent fabrication steps are indicated in black (mesa channel etch), orange (contact pad evaporation), and red (gate evaporation). Exemplary circuit diagrams for the two-point or four-point contact resistance (white) and magnetotransport measurements (black) are shown. The channel of the Hall bar has a width of  $20\ \mu\text{m}$  and the contact pairs have a spacing of  $100\ \mu\text{m}$  with a spacing of  $200\ \mu\text{m}$  between pairs. Implanted areas with crossed-out contact areas are test structures for fabrication and are not connected to the channel. (b) Longitudinal  $\rho_{xx}$  and transversal  $\rho_{xy}$  resistance obtained by magnetotransport measurements at a temperature of  $1.6\ \text{K}$  and a gate voltage of  $V_G = 0.6\ \text{V}$ . The structure was annealed using LA parameter set  $S4^* = \{1.8\ \text{W}, 2.5\ \text{mm/s}\}$ . The Hall resistance corresponding to the filling factors  $n_F = 4, 6, 8$  are indicated as a guide for the eye in the graph. An electron density of  $n = 3.5 \times 10^{11}\ \text{cm}^{-2}$  and an electron mobility of  $\mu = 1.6 \times 10^5\ \text{cm}^2/(\text{Vs})$  are obtained.

$2.5\ \text{mm/s}$ ). We observe a distinct plateau in the longitudinal resistance  $\rho_{xy}$  as well as oscillations in the transverse resistance  $\rho_{xx}$  which align with the characteristics of the integer quantum Hall effect. The plateau matches the quantized resistance value corresponding to a filling factor of  $n_F = 4$ .

The presence of two-dimensional (2D) features proves two important aspects. First, it confirms that the LA contacts retain their conductivity even at cryogenic temperatures, ensuring their suitability for low-temperature application. Second, the observation of 2D features verifies that the LA contacts have established contact with the 2DEG.

### B. Mobility

Having established the functionality of the LA contacts, in a next step we compare their performance with that of a GA reference sample. To this end, we measure the electron mobility  $\mu$  versus electron density  $n$  relation for the LA structure annealed with parameter set  $S4^*$  as well as for a GA

reference at  $1.6$  and  $4.2\ \text{K}$ . The results are shown in Fig. 4(a). We measure the voltages used to determine the electron density and mobility simultaneously on several pairs of contacts. We combine transverse and longitudinal voltages that share a contact or are measured from neighboring contacts in order to determine the charge carrier density and corresponding mobility separately for different segments of the channel. When calculating the longitudinal sheet resistance, we take into account the length of the segment. We then calculate the mean value of the electron mobilities at the same electron densities. We take care to stay below a critical gate voltage to prevent the charging of trap states in the heterostructure, oxide, or intervening interfaces, which would screen charged defects resulting in an artificially enhanced mobility [42,43]. We observe that the LA sample has a higher  $\mu$  at the same  $n$  compared to the GA sample. At  $1.6\ \text{K}$ , the LA sample reaches an electron mobility of  $\mu = 2.4 \times 10^5\ \text{cm}^2/(\text{Vs})$  at an electron density of  $n = 5.0 \times 10^{11}\ \text{cm}^{-2}$ . Meanwhile the GA sample shows a  $\mu = 1.7 \times 10^5\ \text{cm}^2/(\text{Vs})$  at the same  $n$ . The electron mobility of both samples decreases as expected when the temperature is increased to  $4.2\ \text{K}$ : we obtain  $2.0 \times 10^5\ \text{cm}^2/(\text{Vs})$  for the LA sample and  $1.5 \times 10^5\ \text{cm}^2/(\text{Vs})$  for the GA sample at the aforementioned density.

To better understand the measurement data, we plot  $\mu$  versus  $n$  in log-log form and examine the power-law dependence  $\mu \propto n^\alpha$  as shown in Fig. 4(b). The exponent  $\alpha$  depends on the type of the scattering mechanism limiting the mobility. We observe two regions for each sample, following a specific power law with different exponent  $\alpha$ . For the LA sample, we get a value of  $\alpha = 2.7$  at densities below  $n = 2.0 \times 10^{11}\ \text{cm}^{-2}$  and a value of  $\alpha = 0.7$  at densities above  $n = 3.5 \times 10^{11}\ \text{cm}^{-2}$ . For the GA sample, we obtain  $\alpha = 2.6/1.0$  in the same regions. This is consistent with previous electron mobility studies conducted in Si/SiGe heterostructures [43,44]. In those studies, the low-density scaling is attributed to be limited by the presence of remote charge impurities situated in the vicinity of the semiconductor-oxide interface. Calculations had predicted an exponent of  $\alpha_{\text{remote}} = 3/2$  in such scenarios [45,46]. However, it is commonly observed that larger exponents are encountered, which can be explained by incorporating local field corrections [47]. As the electron density in the quantum well increases, the influence of these remote impurities decreases, and electron mobility becomes limited by three-dimensional (3D) charge defects within the semiconductor bulk, characterized by an exponent  $\alpha_{3D} = 1/2$ .

At very low  $n$ , there is compelling evidence suggesting that the metal-to-insulator transition is primarily governed by disorder-driven electron localization [46]. The presence of an inhomogeneous distribution of charged defects leads to the formation of small and unconnected electron puddles within the system. A conduction path only forms when some of these puddles start connecting. The electron density  $n_p$  at this point follows the principles of percolation theory and gives insights about the extent of disorder in the device. To this end, we calculate the longitudinal conductivity  $\sigma_{xx}$  as a function of the density and fit the low-density regime (up to  $2.0 \times 10^{11}\ \text{cm}^{-2}$ ) according to percolation theory using  $\sigma_{xx}(n) = C(n - n_p)^{1.31}$  [48]. The results are shown in Fig. 4(c) for  $1.6\ \text{K}$  and in Appendix E for the  $4.2\ \text{K}$  data. We obtain identical  $n_p$  for the LA and GA samples at  $1.6\ \text{K}$  of  $n_p = 1 \times 10^{11}\ \text{cm}^{-2}$ .

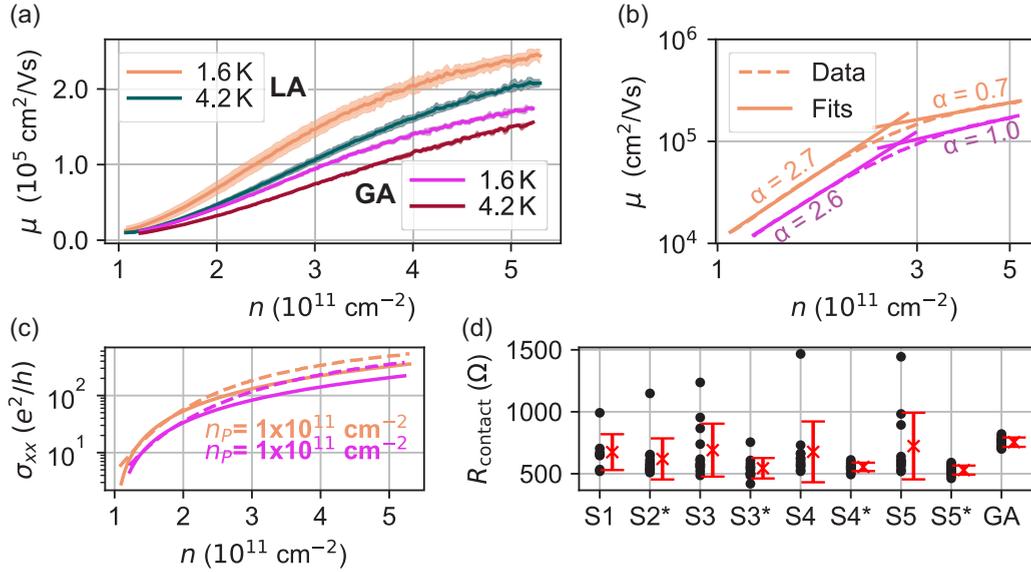


FIG. 4. Cryogenic transport measurements. (a) Mobility  $\mu$  versus electron density  $n$  for the laser annealed (LA) and globally annealed (GA) samples at 1.6 and 4.2 K. The average of all measured segments is shown as solid lines, while the standard deviation is given as shaded areas. (b) Log-log plot of mobility  $\mu$  versus electron density  $n$ . Data sets, corresponding to the color from panel (a), are shown as dashed lines while the two fits represent  $\mu \propto n^\alpha$  for low and high density. Each fit is shown in solid lines with corresponding power-law exponent  $\alpha$ . (c) Conductivity  $\sigma_{xx}$  versus electron density  $n$ . The data are shown in dashed lines, while the fits  $\sigma_{xx} = C(n - n_p)^{1.31}$  to the low-electron-density regime are shown in solid lines. (d) Contact resistance obtained for LA parameter sets as shown in Fig. 2(a) as well as a GA reference sample. Individual data points are shown as black circles while the red crosses indicate average resistance and resistance variance.

When we compare the performance of the LA and GA samples, we find that the LA sample exhibits improvements across all transport properties. Nevertheless, it is important to note that a recent comprehensive study assessing electron mobilities and percolation densities in state-of-the-art Si/SiGe heterostructures revealed a sample-to-sample variance on the order of, or even greater than, the differences we observe between the LA and GA samples [49]. Consequently, it is crucial to gather a more complete statistical data set to effectively distinguish the impact of the wafer level variability from the potential benefits of laser annealing.

Hence, we have shown that the transport properties of a LA sample compare favorably with those of a GA sample. The similarity in transport characteristics between the two annealing methods suggests that they are interchangeable. Combined with the reduced heat load in the active region, this supports the feasibility of laser annealing as a viable alternative for activation of ion-implanted contacts. This is especially relevant for applications at or below liquid helium temperature, where maintaining the integrity of the active regions is crucial for achieving high-performance quantum devices.

### C. Contact resistance

In addition to the carrier mobility, we measure and compare the contact resistance at liquid helium temperature (4.2 K) by employing a combination of two- and four-point measurements. Initially, we ramp the gate voltage to  $V_G = 1 \text{ V}$  to achieve a low channel resistance. The exact mobility in the channel is not relevant for this type of measurement. Subsequently, we sweep the voltage  $V_{2P}$  [see Fig. 3(a)] applied across two contacts on one side of the channel and measure

the corresponding current  $I_C$  using a lock-in amplifier. Additionally, to obtain the channel resistance, we measure the voltage drop  $V_{4P}$  across the two contacts on the opposite side of the channel with a second lock-in amplifier, effectively implementing a four-point measurement configuration. From this we can calculate the sum of the two contact resistances  $R_{i,j}$  using

$$R_{i,j} = R_i + R_j = V_{2P}/I_C - V_{4P}/I_C - R_{\text{setup}}, \quad (2)$$

where  $R_{\text{setup}}$  is the series resistance of the setup, which we determine by shorting two measurement lines as close as possible to the sample. By systematically permuting all possible contact combinations  $(i, j) \in \{1, 2, 3, 4, 5, 6\}$  on both sides of the channel, we can establish a system of linear equations and solve it for the single contact resistance  $R_{\text{contact},i}$ :

$$R_{\text{contact},i} = (R_{i,j} + R_{i,k} - R_{j,k})/2. \quad (3)$$

The calculated contact resistances  $R_{\text{contact}}$  for the investigated LA parameter sets (S1–S5) as well as a GA reference sample are shown in Fig. 4(d). In our investigation, we observe that all laser-annealed samples exhibit an average resistance that is lower than that of the reference sample. We find an average resistance for the GA sample of  $R_{\text{cont.,GA}} = 755 \Omega$  and a minimum for the LA samples of  $R_{\text{cont.,S5}^*} = 530 \Omega$ . However, notable variations in resistance values are observed among the LA samples, particularly for samples scanned along the  $x$  direction.

We attribute the increased variations observed for samples annealed along the  $x$  direction to insufficient overlap between the scanned and the implanted region. This inadequate overlap can lead to a remaining thin amorphous layer between annealed contact and the channel, which imposes a significant

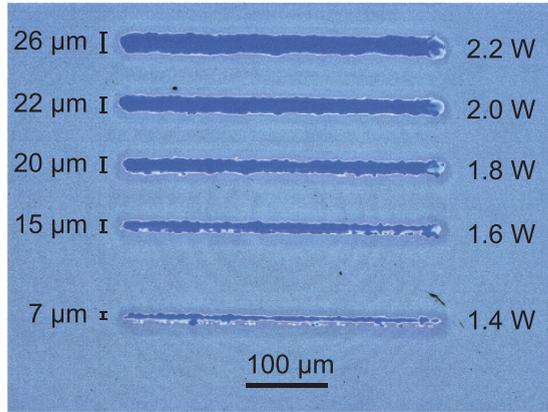


FIG. 5. Optical image of a flat implanted sample of wafer A after individual lines have been annealed with  $v = 10$  mm/s and increasing laser power  $P$ . The color change indicates recrystallization, which we use to determine the linewidth.

series resistance. This can be solved for arbitrary geometries where boundaries of the implanted regions are nonparallel by extending the scanned region beyond the boundaries of the implanted region by one scan-line spacing.

The careful selection of scan orientation relative to the contact geometry, guided by the calibrated LA parameter sets, has allowed us to form contacts at cryogenic temperatures with lower resistivity compared to globally annealed references. These contacts exhibit resistances at least one order of magnitude below the von Klitzing constant  $R_K \approx 26$  k $\Omega$  as a reference for the typical resistance of quantum devices. This emphasizes their suitability for high-performance quantum devices operating at temperatures below 4.2 K. This underscores the LA process being a more than suitable alternative to global annealing for cryogenic contact formation.

## V. CONCLUSION

Using local laser annealing, we have successfully demonstrated the activation of phosphorus-implanted contacts to a quantum well in undoped Si/SiGe with 530  $\Omega$  contact resistance at 4.2 K. In the process, we have developed a

calibration procedure capable of determining the success of annealing parameters based on optical inspection. We have discovered that the required laser power strongly depends on the details of the virtual SiGe substrate. This calibration procedure allows us to quickly adapt the annealing parameters to each new heterostructure to keep up with the constant optimization effort. When investigating the transport behavior of a laser-annealed Hall bar structure at a temperature range between 1.6 and 4.2 K, we observed that its performance was either comparable or even superior to that of a globally annealed reference sample, with respect to carrier mobility and contact resistance. We obtained an electron mobility of  $\mu = 2.4 \times 10^5$  cm<sup>2</sup>/(V s) at an electron density of  $n = 5.0 \times 10^{11}$  cm<sup>-2</sup> for a laser-annealed Hall bar. This study demonstrates that laser annealing is a viable alternative for forming ion-implanted contacts in cryogenic applications. The localized treatment of implantation damage provided by laser annealing offers the distinct advantage of minimizing heat impact on critical regions, making it a promising technique to use for quantum devices based on high-performance Si/SiGe heterostructures.

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## APPENDIX A: STEPS ALONG SLOW AXIS

We reduce the intrinsically three-dimensional parameter space  $\{P, v, \Delta y\}$  by setting the step size of the slow axis to a fixed value  $\Delta y = 10$   $\mu$ m. By annealing single lines (here with fixed  $v = 10$  mm/s for wafer A), we have determined the width of the recrystallized line depending on the power  $P$  as shown in Fig. 5. Linewidths of up to 40  $\mu$ m could be achieved ( $P = 3.8$  W) before signs of surface degradation began to

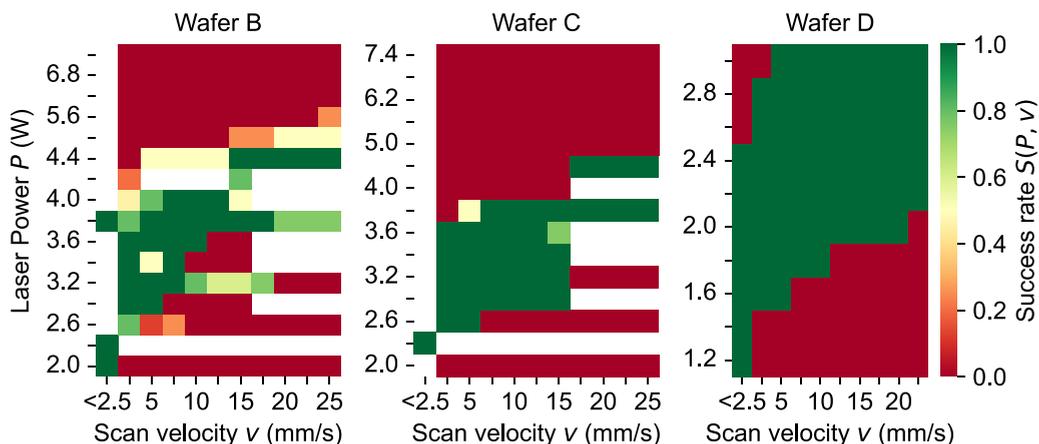


FIG. 6. Map of success rates  $S(P, V)$  for wafers B–D obtained by optical inspection of laser-annealed squares [cf. Fig. 2(a)].

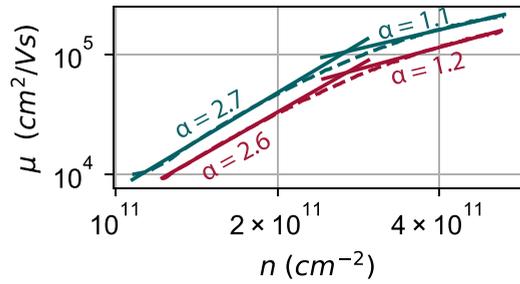


FIG. 7. Log-log plot of electron mobility  $\mu$  versus electron density  $n$  for LA and GA samples, measured at 4 K. Dashed lines indicate data, while solid lines show two-part-wise power-law fits. Colors correspond to the legend in Fig. 4.

appear. In later quantum devices, it can become very critical to limit the thermal input as much as possible to the contact regions. For this reason, we chose a small step size to maintain high spacial precision: We picked half of the linewidth of  $20\ \mu\text{m}$ , at which a mostly homogeneous color change along the fast scan direction was observed.

#### APPENDIX B: CALIBRATION RESULTS B–D

The maps of success rate  $S$  versus laser annealing parameters for wafers B–D are shown in Fig. 6.

#### APPENDIX C: HALL-BAR FABRICATION

After being diced into  $10\ \text{mm} \times 10\ \text{mm}$  pieces, the samples underwent a cleaning process using an RCA flow. This cleaning procedure involved consecutive room-temperature baths in Piranha ( $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$  3:1), SC1 ( $\text{NH}_3:\text{H}_2\text{O}_2:\text{H}_2\text{O}$  1:1:5), and SC2 ( $\text{HCl}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$  1:1:6) solutions, with interleaved hydrofluoric acid (HF) oxide strips and deionized-water rinsing steps. Afterwards, markers for layer-on-layer alignment were etched into the surface using reactive ion etching (RIE). Optical photoresist was used as a mask to define the contact areas. Implantation was carried out by the Institute of Ion Beam Physics and Materials (Helmholtz-Zentrum-Dresden-Rossendorf HZDR) in a Danfysik A/S (Denmark, Model

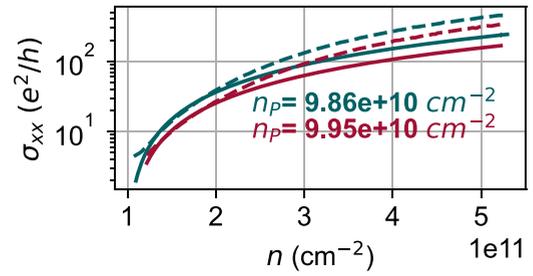


FIG. 8. Longitudinal conductance  $\sigma_{xx}$  versus carrier density  $n$  for LA and GA samples, measured at 4 K. Solid lines indicated fit functions consistent with percolation theory. Colors correspond to the legend in Fig. 4.

1050). Following the implantation, the resist mask was subsequently removed using a solvent, and an additional RCA cleaning step was performed. The samples were then subjected to either laser or global annealing, which was carried in the mentioned RTP system at  $750\ ^\circ\text{C}$  for 30 s in an argon atmosphere. After annealing, the active channel region was defined using a RIE process. To remove any possible native oxide, an HF dip was performed prior to the evaporation of the metal contact pads. The active region was isolated from the subsequently evaporated gate by a 20-nm-thick layer of aluminum oxide, deposited via atomic layer deposition.

#### APPENDIX D: HALL BAR MEASUREMENT SETUP

The current through the Hall bar is supplied by applying 5 V between two contacts using a lock-in amplifier [see Fig. 3(a)]. A  $100\ \text{M}\Omega$  resistor limits the current to  $I_{\text{max}} = 50\ \text{nA}$ . The longitudinal  $U_{xx}$  and transverse  $U_{xy}$  voltages are measured with separate lock-in amplifiers, which are all frequency synchronized with the first one.

#### APPENDIX E: 4 K MEASUREMENT RESULTS

The results of the power-law  $\mu \propto n^\alpha$  fit, obtained for the LA and GA samples at 4 K, are shown in Fig. 7. The colors used correspond to the legend in Fig. 4. Furthermore, the longitudinal conductance  $\sigma_{xx}$  versus mobility  $\mu$  plot for these samples, as well as the extracted percolation density, are given in Fig. 8.

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