Processing effect on spin-orbit torque switching and efficiency characterization in perpendicularly magnetized pillar devices

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Spin-orbit torque (SOT)-induced magnetization switching can be explained by either a single-domain coherent switching scenario or a domain-wall dynamics scenario, depending on the device size. In this study, we systematically investigate the processing effect on magnetic and SOT properties across a broad range of device sizes and geometries, from 5-μm Hall bars to submicrometer-sized pillars and magnetic tunnel junctions (MTJs), with an identical W/CoFeB/MgO magnetic heterostructure. We first examine the impact of the fabrication process and device size on the measured magnetic properties, where coercivity H_c enhances while reducing the pillar size. Next, the current-driven hysteresis loop-shift measurement is utilized to characterize the dampinglike SOT efficiency ξ_{DL}, which is found to be fairly size independent. In contrast, current-induced SOT switching shows that the critical switching current density J_{sw} increases significantly with the device size reduction, suggesting a strong correlation between J_{sw} and H_c. Nevertheless, the current-driven loop-shift phase diagram and the domain-wall depinning model provide a relatively consistent estimation of J_{sw}, verifying the applicability of these two methods in the studied pillar size range. Last, we compare the SOT switching results from a micrometer-sized Hall bar device and a micrometer-sized three-terminal MTJ device, where a consistent estimated dampinglike SOT efficiency can be reached. Our results give insight into the processing and size effects on magnetic devices and provide proper protocols for SOT efficiency and critical switching current density estimations.

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I. INTRODUCTION

Spin torque-based magnetic random access memory (MRAM) is now fast developing for embedded applications and has the potential to serve as a last-level cache due to its nonvolatile nature, fast operation speed, and low power consumption. The spin-orbit torque (SOT) MRAM prototype [1–4] proposed a decade ago leverages the spin Hall effect in heavy transition metals to form a three-terminal magnetic tunnel junction (MTJ) device architecture that can separate read path and write path without flowing a tremendous amount of current through the tunnel barrier. Therefore, compared to the conventional spin-transfer torque MRAM with two-terminal geometry [5–7], SOT MRAM can potentially give rise to more efficient magnetization switching and higher endurance. SOT MRAM devices can be further categorized into various types depending on the relative orientation between the anisotropy axis and the spin-polarization directions. For example, type-z SOT MRAM with perpendicular magnetic anisotropy (PMA) has the advantage of reaching higher storage density and shorter switching time (subnanosecond) compared to those with type-y configuration (in-plane anisotropy) [6,8,9]. Detailed research and development of type-z SOT MRAM devices is therefore critical for realizing energy-efficient SOT MRAM products.

However, the fabrication of a fully functional three-terminal MTJ device with high tunneling magnetoresistance (TMR) could be challenging and time-consuming. In the semiconductor industry, it is common to employ suitable test vehicles or testkey devices for preliminary property screening during the early stage of development. Micrometer-sized Hall bar devices with normal metal–ferromagnet magnetic heterostructures are therefore widely adopted as the test vehicle for preliminary SOT characterizations due to their more straightforward fabrication process and broader applicability. In an MTJ device, the magnetic state readout comes from the current perpendicular-to-plane resistance R_{MTJ} through TMR. In contrast, the magnetic state of a Hall bar device with PMA is detected through the transverse voltage arm employing the anomalous Hall effect (AHE) measurement [10–17], which can streamline the study of SOT properties and improve device development efficiency. However, it is essential to note that using Hall bar devices as test vehicles requires careful consideration, such as the device dimensions, which could significantly impact the switching dynamics [4,18–28]. To bridge the gap between the Hall bar device and MTJ, a magnetic pillar can be fabricated or patterned at the Hall-cross region. The size effects can then be investigated by defining various sizes of pillars on the Hall bar device. It is also crucial to know that, for micrometer-sized devices in the multidomain regime, magnetization reversal occurs due

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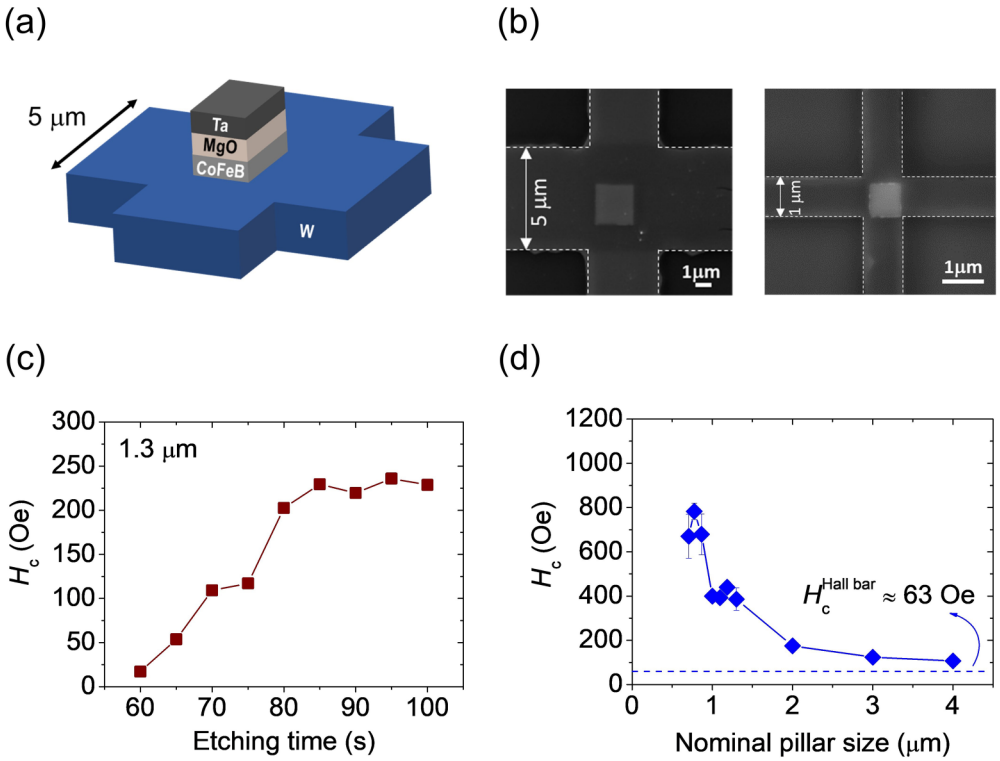

FIG. 1. (a) Illustration of pillar-shaped device on Hall bar. (b) SEM images of photolithography-defined pillar on 5-μm-wide Hall bar (left) and e-beam lithography-defined pillar on 1-μm-wide Hall bar (right). (c) H_c of pillar device vs etching time. (d) H_c as function of pillar size. Dashed line represents value for extended Hall bar.

to domain nucleation and domain-wall depinning (motion) nature [12,25,26]. In contrast, the magnetization reversal process is coherent rotation if the device size is less than 80 nm, which follows a single-domain scenario [4,20–23,27]. Thus, choosing an appropriate model to analyze the results obtained from various-sized pillar devices is critical.

In this work, we systematically characterize the SOT efficiency and perform current-induced SOT switching measurements on a wide range of devices, from 5-μm Hall bar to submicrometer-sized pillars (on the Hall cross) and MTJs with identical W-based magnetic heterostructures. First, we analyze the resistance and coercivity (H_c) change during the fabrication (Ar ion-beam etching) process, and we observe a noticeable increase in both when the magnetic pillar is formed out of the Hall bar. Next, SOT characterization results from current-induced hysteresis loop-shift measurement show a fairly constant dampinglike SOT (DL SOT) efficiency $|\xi_{DL}| \sim 0.35$ across all pillar sizes, suggesting the universality of the adopted technique. Current-induced SOT switching measurement shows that the critical switching current density (J_{sw}) increases with decreasing the pillar size, corresponding to the enhancement of H_c. We further utilize two methods: (1) domain-wall depinning model and (2) loop-shift phase diagram approach to estimate J_{sw}. By carefully taking the in-plane field and the Joule heating effect on H_c into account, we find consistent results that affirm the strong correlation between the estimated $|\xi_{DL}|$ and J_{sw}. Additionally, we adopt the domain-wall depinning model to estimate $|\xi_{DL}|$ from a W-based Hall bar device and a three-terminal MTJ device with an identical film-stack design, which yields a consistent DL SOT efficiency of $|\xi_{DL}| \sim 0.3$. These results highlight the validity of using a Hall bar as test vehicle for early-stage SOT study and the importance of using suitable models that take different effects acting on coercivity into account for analysis.

II. DEVICE FABRICATION AND SIZE DEPENDENCE OF H_c

Thin-film W(4)/CoFeB(1.4)/MgO(1.5)/Ta(2) (units in nanometer) magnetic heterostructures are prepared by magnetron sputtering. The multilayer stacks are deposited on a Si/SiO_2 substrate with a base pressure of 2×10^{-8} Torr. The metallic and oxide layers are deposited by DC and rf sputtering with Ar working pressure of 3 and 10 mTorr, respectively. The thin films are first postannealed at 300 °C in the vacuum chamber for 1 h to induce PMA. Next, the films are patterned into Hall bar devices with a current channel width of 5 μm through photolithography and subsequent Ar ion-beam etching (IBE). Next, we define a square pillar at the center of the Hall cross through either photolithography or e-beam lithography, as illustrated in Fig. 1(a). Pillar sizes $\geqslant 2$ μm are defined by photolithography, whereas sizes < 2 μm are defined using e-beam lithography. A scanning electron microscope (SEM) image of pillar devices fabricated using photolithography is shown in Fig. 1(b). Note that as pillar size shrinks, the Hall signal decreases and makes the readout difficult (see Supplemental Material, S1 [29]). Therefore, for pillar size < 1 μm, the width of the current channel and voltage arm are further

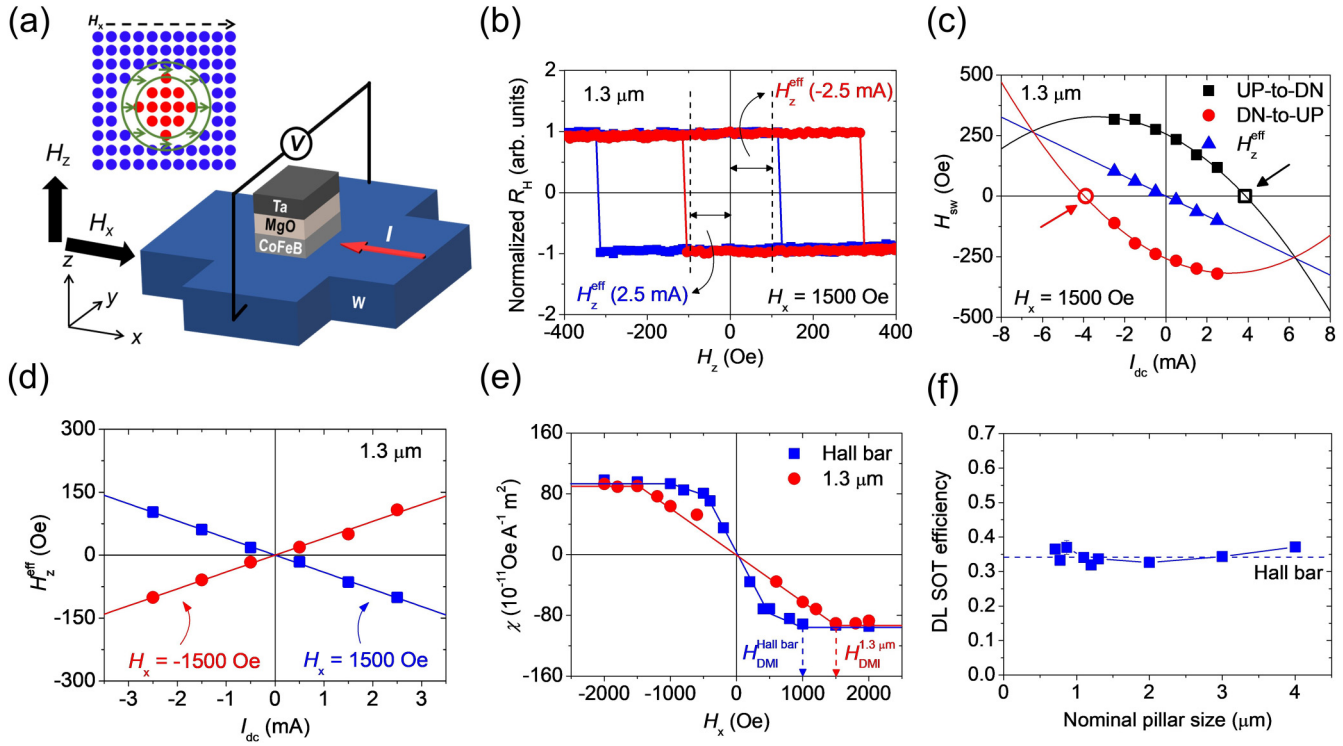

FIG. 2. (a) Schematic illustration of current-induced hysteresis loop measurement on pillar device. Top inset shows nucleated domain in CoFeB layer with domain-wall moments aligned parallelly to bias field H_x. Red (blue) dots represent $-z(+z)$ moments and arrows represent domain-wall moments. (b) Representative shifted loops under $I_{DC} = \pm 2.5$ mA and $H_x = 1500$ Oe for 1.3-μm pillar device. (c) Extracted switching field H_{sw} of up-to-down (black squares), down-to-up (red circles), and current-induced effective field H_z^{eff} (blue triangles) as functions of I_{DC} at $H_x = 1500$ Oe. Open circle and open square indicate estimated switching currents extrapolated from quadratic fittings of switching fields. (d) H_z^{eff} as function of I_{DC} at $H_x = \pm 1500$ Oe for representative pillar device. (e) DL SOT efficacy χ as function of H_x. (f) DL SOT efficiency as function of nominal pillar size. Dashed line represents value estimated from Hall bar device.

narrowed down to 1 μm using e-beam lithography and subsequent IBE to enhance the detected Hall signal, as shown in Fig. 1(b).

After either photolithography or e-beam lithography process, we employ IBE to pattern the pillars. Figure 1(c) summarizes H_c of the pillars obtained via AHE measurement as a function of the etching time. H_c initially increases with the etching time and then gradually saturates after the device is etched for 90 s, indicating the reduction of domain nucleation sites and/or domain numbers in the CoFeB layer. Notably, a precise etching method monitored by secondary ion mass spectrometer is developed to ensure the complete etching of CoFeB, which is essential for the quantitative characterization in the following sections (see more IBE details in Supplemental Material, S2 [29]).

To investigate the size effect on H_c, we perform the above-mentioned etching method to fabricate pillar devices with various lateral dimensions. As summarized in Fig. 1(d), H_c strongly enhances from ~ 63 Oe for the original Hall bar to as large as 800 Oe as the pillar size is reduced down to 800 nm, which again can be attributed to the reduction of domain nucleation sites and/or number of domain within the pillar [29]. Previous works pointed out that the increase of H_c in decreasing device size could also be correlated to the change of demagnetization factor and effective perpendicular magnetic anisotropy [19,27].

III. SIZE DEPENDENCE OF CHARACTERIZED SOT EFFICIENCY ξ_{DL}

To characterize the dependence of SOT efficiency on device size, we conduct hysteresis loop-shift measurement [10,11,30,31] on a series of pillar devices, as illustrated in Fig. 2(a). A DC current (I_{DC}) is injected into the current channel and an in-plane bias field (H_x) is applied along the x axis, and the Hall resistance is detected along the transverse y direction. With increasing H_x, the domain-wall moments in any nucleated domains start to align with this field [31]. The DL SOT then exerts on the domain-wall moments, serving as an out-of-plane effective field H_z^{eff} that further facilitates domain expansion [26,31]. Note that when H_x is sufficiently large and comparable to the Dzyaloshinskii-Moriya interaction effective field (H_{DMI}), the domain-wall moments are parallelly aligned with H_x (full Néel configuration), resulting in a maximized SOT efficiency (more details in Refs. [26,32–34]). Representative results obtained from a 1.3-μm pillar device are shown in Figs. 2(b)–2(d). Figure 2(b) shows the shifted hysteresis loops with $I_{DC} = \pm 2.5$ mA and $H_x = 1500$ Oe. The sharp magnetization reversal of the hysteresis loop is a feature of small-sized pillar devices. By extracting the shift of hysteresis loops under various currents, the switching fields (H_{sw}) and current-induced effective fields (H_z^{eff}) are summarized in Fig. 2(c), where H_z^{eff} is found linearly proportional to the

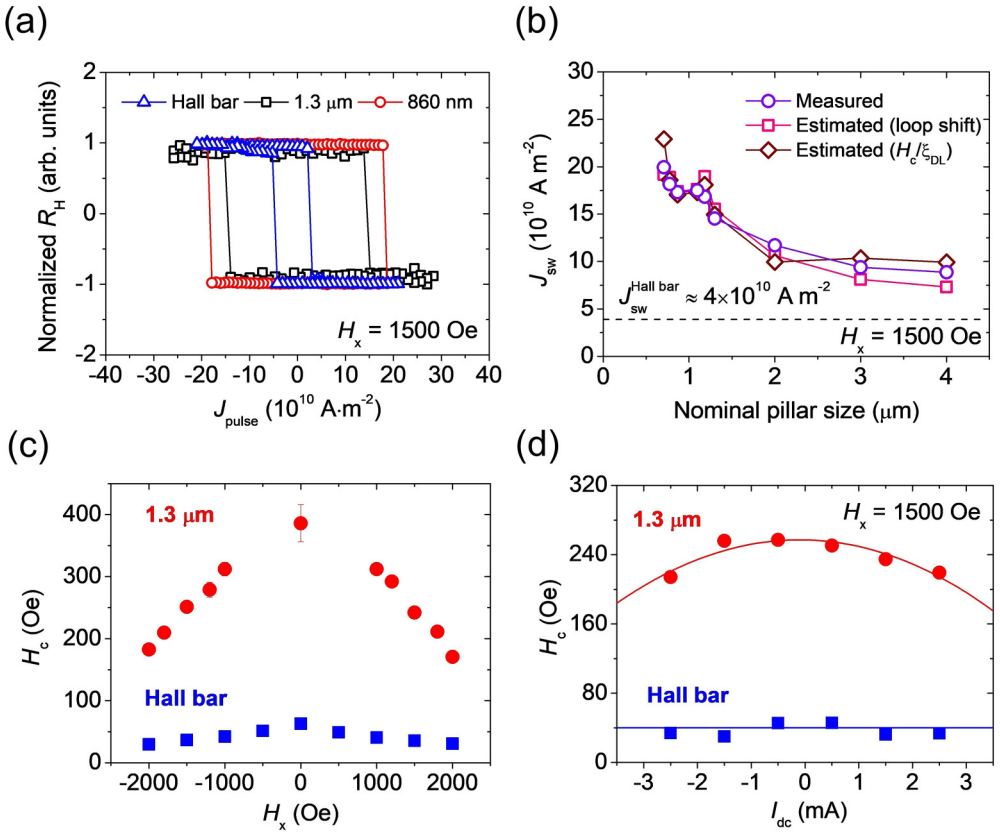

FIG. 3. (a) Representative current-driven switching loops of Hall bar, 1.3-μm pillar, and 860-nm pillar device. (b) Critical switching current densities J_{sw} as function of pillar size. Estimated results are extracted from switching field extrapolation [as shown in Fig. 2(c)]. Dashed line presents J_{sw} of Hall bar. (c) H_c vs in-plane bias-field H_x. (d) H_c vs. applied current I_{DC} under $H_x = 1500$ Oe.

applied I_{DC}. The opposite sign of the slopes at $H_x = \pm 1500$ Oe shown in Fig. 2(d) corresponds to the opposite orientation of the domain-wall moment. The extracted DL SOT efficacies $\chi = H_z^{eff}/J_{DC}$ vs H_x for a Hall bar and a 1.3-μm-wide pillar device are summarized in Fig. 2(e), where the magnitude of χ saturates at $\approx$90 Oe/10^{11} A m^{-2} for both devices. The fields to saturate χ are extracted to be $|H_{DMI}| \approx$ 1000 Oe (the maximum among various nucleated domains) for the Hall bar and $|H_{DMI}| \approx 1500$ Oe for the 1.3-μm pillar device [10]. It is noted that the H_{DMI} extracted by hysteresis loop-shift measurement only presents a rough estimation of the upper bound of H_{DMI} due to the multidomain nature of the tested devices. Also note that the current shunting effect has been considered using a parallel circuit model to estimate J_{DC}.

The DL SOT efficiency (ξ_{DL}) can be further estimated through [10,32]

$$|\xi_{DL}| = \frac{2e}{\hbar}\left(\frac{2}{\pi}\right)\mu_0 M_s t_{CoFeB}\chi, \quad (1)$$

where M_s represents the saturation magnetization of CoFeB $\approx$1200 emu/cc (obtained by a vibrating sample magnetometer). Figure 2(f) summarizes the DL SOT efficiency of pillar devices with various sizes. It shows that the DL SOT efficiencies are fairly consistent ($\sim$0.35) among Hall bar devices, micrometer-sized and submicrometer-sized pillar devices. This result implies that even though the current-induced hysteresis loop-shift measurement is based on a multidomain scenario, it is still feasible to estimate the DL SOT efficiency from micrometer-sized Hall bar devices and pillar-shaped devices with dimensions down to 800 nm. Note that another popular SOT characterization technique that employs Hall bar as test vehicle, the harmonic Hall voltage approach, is usually performed in the saturated state. Under such circumstance, the magnetization remains in a quasiuniform configuration and can be explained by a macrospin model to potentially simplify the characterization protocol. However, the predicament of calibrating the planar Hall correction and the thermal effects inherent in this method can potentially lead to incorrect estimation. The plight of these inconsistent SOT efficiency estimations still remains unresolved [35–40]; therefore, in this work we focus on only the loop shift and the switching approaches.

IV. SIZE DEPENDENCE OF SOT SWITCHING CURRENT DENSITY J_{sw}

We further perform current-induced SOT switching measurements on pillar devices with various sizes. The measurement scheme is similar to Fig. 2(a) with applying different amplitudes of pulsed currents (pulse width $t_{pulse} = 50$ ms) and an in-plane bias field H_x on the device. Representative current-induced switching loops of a Hall bar, a 1.3-μm-wide pillar device, and an 860-nm-wide pillar device under $H_x = 1500$ Oe are summarized in Fig. 3(a). J_{sw} is enhanced when the device size is scaled down. We further outline the J_{sw} under $H_x = 1500$ Oe as a function of pillar size in Fig. 3(b).

The observed increase of J_{sw} while reducing pillar size is consistent with previous studies and can be well explained by the reduction of the domain nucleations and domain-wall propagations [21,23,28].

In our micrometer-sized and submicrometer-sized devices, the magnetization reversal process is typically governed by domain nucleation and the domain-wall depinning (see Supplemental Material, S3 [29]). To further examine the correlation between J_{sw} and previously estimated DL SOT efficiency, it has been proposed that the relation between J_{sw} and ξ_{DL} in this regime can be evaluated through [12,25,26,41]

$$J_{sw} = \frac{2e}{\hbar}\left(\frac{2}{\pi}\right)\mu_0 M_s t_{CoFeB}\left(\frac{H_c}{|\xi_{DL}|}\right). \quad (2)$$

Here, we emphasize that the H_c employed in this estimation must first account for its in-plane bias-field dependence since H_c reduces when increasing H_x [42,43], as shown in Fig. 3(c). H_c shows a significant reduction with increasing H_x for the 1.3-μm-wide pillar device while it decreases less but not negligibly for the Hall bar. Moreover, as presented in Fig. 3(d), the Joule heating effect is also pronounced in the pillar device. H_c of the 1.3-μm-wide pillar device under $H_x = 1500$ Oe with various currents is estimated from $\frac{H_{sw}^{UP-to-DN} - H_{sw}^{DN-to-UP}}{2}$ in Fig. 2(c). The obvious quadratic relation between such H_c and I_{DC} suggests that the Joule heating should also be accounted for to estimate the depinning field accurately [4,44–46]. In contrast, the Joule heating effect is less noticeable, and H_c reduces only slightly for the Hall bar device (see more details in Supplemental Material, S4 [29]). Failure to consider these effects would result in overestimating J_{sw} from ξ_{DL} (or ξ_{DL} from J_{sw}). To show the validity of Eq. (2), we estimate J_{sw} with the ξ_{DL} obtained from loop-shift measurement and the H_c obtained from the quadratic fitting in the loop-shift phase diagram [Fig. 2(c)] under H_x and I_{sw}. As shown in Fig. 3(b), the H_c/ξ_{DL}-estimated J_{sw} is consistent with the measured J_{sw}, confirming the strong correlation between DL-SOT efficiency and critical switching current density. It is noted that we also measure J_{sw} under various H_x, and ξ_{DL} estimated from a much simpler macrospin model shows an unreasonably large SOT efficiency (∼–2.88), suggesting the assumption of coherent switching is inapplicable to pillar devices in both micrometer-sized and submicrometer-sized regimes (see Supplemental Material [29] for details).

Notably, Zhu *et al.* [25] have reported that the domain-wall depinning model fails to estimate the J_{sw} (or ξ_{DL}) even considering the decrease of J_{sw} due to H_x. However, here we highlight the importance of H_c reduction due to both H_x and the Joule heating. Alternatively, one can also directly use the loop-shift phase diagram [Fig. 2(c)] to estimate the critical switching current density without using Eq. (2). The critical switching current density can be directly extracted by performing quadratic fittings to the up-to-down and down-to-up switching fields under various currents and then extrapolating them to the x axis. The extracted J_{sw}s are denoted in Fig. 2(c) as the open symbols. The loop-shift estimated J_{sw} summarized in Fig. 3(b) also shows a consistent trend compared to the directly measured results.

V. SOT SWITCHING: HALL BAR VS THREE-TERMINAL MTJ DEVICE

Based on previous analysis, we expand the scope of the study to three-terminal MTJ devices. The tested thin film has the structure of Ta(2)/W(4)/CoFeB (1.8)/MgO(1.5)/CoFeB(2)/W(0.5)/Ta(4), which is further postannealed at 400 °C for 20 min in vacuum to induce PMA. W(4) serves as the SOT source. The thinner CoFeB(1.8) is the free layer, and the thicker CoFeB(2) is the fixed layer. Multiple thin films with the same layer design are then fabricated into a Hall bar device and a three-terminal MTJ device for SOT switching measurement. Figure 4(a) shows the AHE result of a Hall bar device, in which the two-step hysteresis loop consists of magnetization reversal of the free and the fixed CoFeB layers. Current-induced SOT switching measurement is then performed on the Hall bar device, as shown in Fig. 4(b). The magnetization reversal is confirmed from the free layer through the Hall resistance change. The switching polarities are opposite under $H_x = \pm 1000$ Oe, which follows the SOT symmetry.

Figure 4(c) shows the structure and the measurement scheme of a three-terminal MTJ device. The bottom Ta(2)/W(4) layers are patterned into a 30-μm-wide strip, and the rest of the layers are etched with IBE to form a micrometer-sized magnetic pillar with lateral dimensions of $10 \times 10\,\mu m^2$. The MTJ resistance R_{MTJ} is measured in response to an out-of-plane field (H_z) or pulsed currents under H_x. Figure 4(d) shows both major and minor loops of R_{MTJ} vs H_z with a TMR ratio ≈14%. The switching of the free (fixed) layer is observed in the minor (major) loop at $|H_z| \approx 100$ Oe (230 Oe). Compared to Fig. 4(a), the switching fields of the free layer and the fixed layer are higher in MTJ than those in the Hall bar device, which is attributed to the reduced lateral dimensions of the ferromagnetic layer in MTJ. It echoes the results in the previous section that the domain-wall number is less in the patterned pillar-shaped device.

Current-induced SOT switching is then performed on the three-terminal MTJ, as shown in Fig. 4(e). Compared to the Hall bar device [Fig. 4(b)], the higher J_{sw} of the MTJ device is consistent with the larger H_c observed. The critical switching current densities under various H_x are extracted from the Hall bar and the MTJ device, as shown in Fig. 4(f). Both devices follow a similar $H_x - J_{sw}$ dependence, except that a higher J_{sw} is observed in the MTJ device under the same H_x, which results from the higher H_c in the MTJ device. Finally, to directly estimate the DL SOT efficiency from MTJ devices, the domain-wall depinning analysis should be applied, where $\chi = H_c/J_{sw}$. It shows that χ for both the Hall bar and the MTJ device is $\approx 80\,\text{Oe}/10^{-11}\,\text{A m}^{-2}$, corresponding to a DL SOT efficiency ≈0.3, which is close to the results of Figs. 2(e) and 2(f). Again, the validity of the domain-wall depinning analysis for estimating DL SOT efficiency is verified by using a three-terminal MTJ device.

It is finally noted that in this work we delve into W-based Hall bar, pillar-shaped, and fully patterned MTJ devices, since W is one of the most commonly employed spin Hall source materials for contemporary CoFeB/MgO-based MTJ. However, heterostructures or devices based on different spin Hall materials might behave differently. We hope our present work

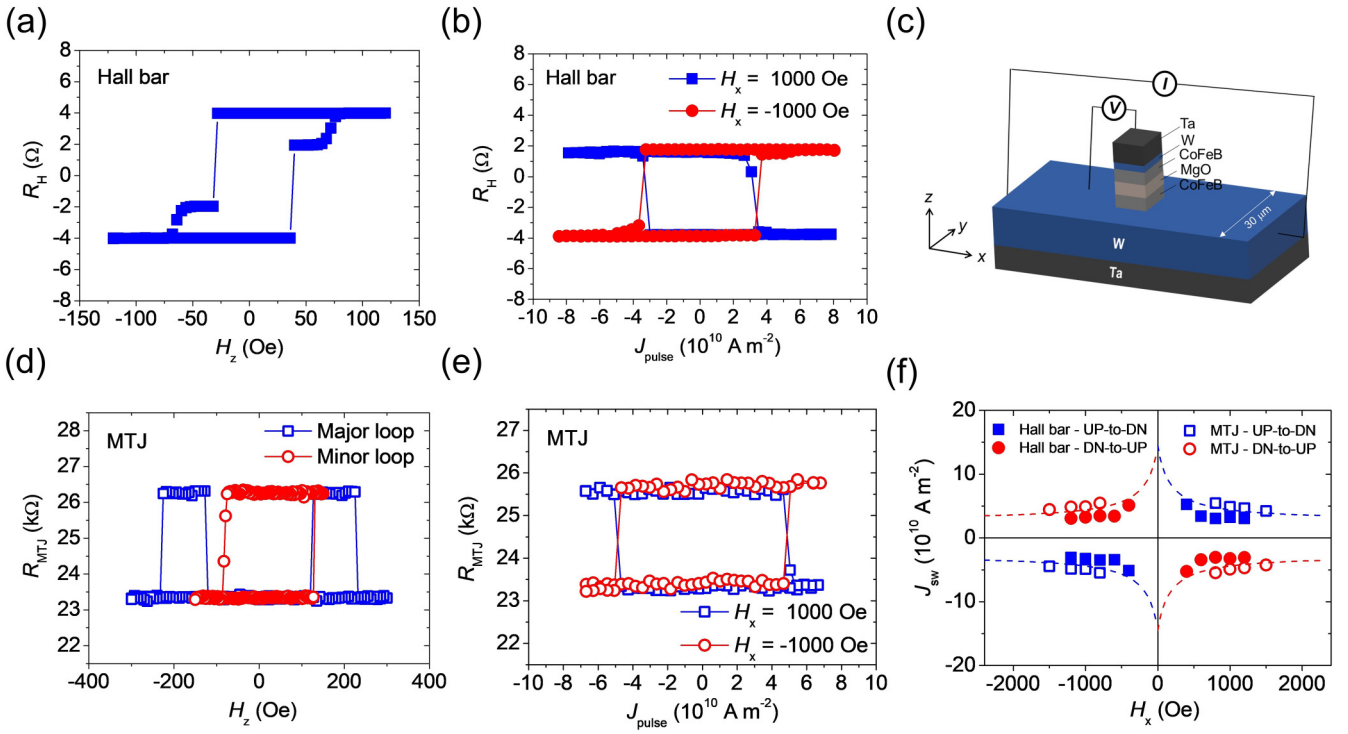

FIG. 4. (a) Representative AHE loop obtained from Hall bar device with MTJ layer stack Ta(2)/W(4)/CoFeB(1.8)/MgO(1.5)/CoFeB(2)/W(0.5)/Ta(4). (b) Representative current-induced switching loops under $H_x = \pm 1000$ Oe of Hall bar device. (c) Structure and measurement scheme for three-terminal MTJ device with pillar size $10 \times 10\,\mu m^2$ and current channel width 30 μm. (d) TMR major and minor loops. (e) MTJ resistance as function of J_{pulse} under $H_x = \pm 1000$ Oe. (f) Switching-phase diagram ($J_{sw} - H_x$) from Hall bar device and three-terminal MTJ device. Solid (open) symbols represent J_{sw} extracted from Hall bar (MTJ). Dashed lines represent guidelines for eyes.

could spark future studies to explore other materials systems using the proposed characterization protocols.

VI. CONCLUSION

In conclusion, we systematically analyze the fabrication process and the size dependence of both magnetic and SOT characteristics of various types of devices. H_c shows a substantial enhancement when the device size is reduced, which can be attributed to the reduction of the domain nucleation sites or the hindered domain-wall motion. The DL SOT efficiency of pillar devices is characterized through hysteresis loop-shift measurement, where the value of ξ_{DL} remains fairly constant across varying pillar sizes. In addition, current-induced SOT switching experiments reveal that J_{sw} exhibits a noticeable increase with decreasing pillar size, corresponding to a similar trend from H_c. The switching-phase diagrams of submicrometer-sized devices show trends that cannot be quantitatively described by the macrospin model. Therefore, a domain-wall depinning model is required to accurately estimate J_{sw} from the characterized SOT efficiency, in which the H_c reduction from both in-plane bias-field H_x and the Joule heating effect are also considered. Additionally, the J_{sw} estimated from the loop-shift phase diagram are consistent with those obtained directly from switching measurements. These findings highlight the strong correlation between ξ_{DL} and J_{sw}, even in micrometer-sized devices that do not follow a single-domain behavior. Finally, we point out that Hall bar devices can serve as effective test vehicles for characterizing SOT efficiency and J_{sw} before investing heavy resources in MTJ (three-terminal SOT device) fabrication, as long as the processing-correlated factors are correctly taken into account while performing analysis.

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W.-B.L. conceived the experiments, fabricated the devices, performed the analysis of the data, and drafted the manuscript; C.-Y.L. performed the hysteresis loop-shift measurement and current-induced SOT switching measurement; T.-Y. Cheng fabricated the magnetic tunnel junction; C.-C.H. performed the current-induced SOT switching measurement; T.-Y. Chen performed the analysis of the data; and C.-F.P. proposed and supervised the study.

The authors declare no competing interests.

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