Proximity effect in PbTe-Pb hybrid nanowire Josephson junctions

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Semiconductor-superconductor hybrid nanowires are a leading material platform for the realization of Majorana zero modes. The semiconductors in previous studies are dominantly InAs or InSb. In this paper, we show the induced superconductivity in PbTe nanowires epitaxially coupled to a superconductor Pb. The Josephson junction devices based on this hybrid reveal a gate-tunable supercurrent in the open regime and a hard superconducting gap in the tunneling regime. By demonstrating the superconducting proximity effect, our result can enable Majorana searches and other applications, such as gate-tunable qubits in a new material platform.

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I. INTRODUCTION

A semiconductor nanowire coupled to a superconductor is an intriguing quantum system owing to the proximity effect. One example is the gate-tunable Josephson junction [1], which plays a key role in the gatemon superconducting qubit [2]. Moreover, the interplay between strong spin-orbit coupling of the semiconductor and Zeeman energy may lead to topological phases hosting Majorana zero modes [3–7]. InAs and InSb nanowires are the semiconductors commonly used in those studies due to several practical reasons, e.g., the well-established state-of-art device fabrication and control [8–10], epitaxial growth of superconductors [11–13] and the strong spin-orbit interaction [14,15]. These advantages are crucial and indeed have enabled tremendous experimental progress on possible Majorana signatures [16–22]. The current roadblock is device disorder, which has to be improved first before further progress [23–34].

To overcome this challenge, PbTe nanowires have recently been proposed as a potentially better candidate [35]. The hope is that the large dielectric constant (∼1350) in PbTe can significantly screen charge disorder. Moreover, growing PbTe on a lattice-matched substrate, CdTe, can further reduce the substrate disorder [36]. Finally, capping the PbTe with CdTe can push the surface disorder away from the core region of the device. Quickly, experimental efforts [36–40] have been carried out on the growth of PbTe nanowires with transport characterizations on the field effect mobility, weak antilocalization, Aharonov-Bohm oscillations, and quantum dots. So far, the key question of whether superconducting proximity effect in PbTe nanowires exists is still pending. Here, we demonstrate the induced superconductivity in PbTe nanowires coupled to a superconductor Pb. Two hallmark transport signatures can be revealed in the Josephson junction (JJ) devices based on this hybrid: a gate-tunable supercurrent in the open regime and a hard superconducting gap in the tunneling regime. Our results fulfill one necessary condition in a new material platform for Majorana explorations and other quantum devices, e.g., hybrid qubits [2].

Figure 1 shows the scanning electron micrograph (SEM) of a PbTe-Pb nanowire (device *A*) and its schematic. The nanowire growth is similar to that in Ref. [36] with minor modifications. The CdTe substrate was first covered by Si_xN_y. Nanowire-shape trenches were defined by etching Si_xN_y. The chip was then loaded into a molecular-beam epitaxy (MBE) chamber. The substrate was cleaned with Ar treatment, annealed at 240.6 °C and then followed by selective area growth of the CdTe buffer. This procedure ensures that the PbTe nanowire is spatially separated from the disorder generated during the substrate cleaning. PbTe was then grown, followed by the Pb film deposition at a tilted angle without breaking the vacuum. The standing wall shadowed part of the PbTe nanowire forming a JJ. The chip was then capped by CdTe. Figure 1(a) is the SEM after growth, and Fig. 1(b) is the JJ layer structure (not in scale).

For the device fabrication, most of the Pb film on the substrate was etched away to prevent a short circuit. Source/drain electrodes and a side gate were evaporated. Ar-plasma etching was performed before the evaporation to remove the CdTe capping in the contact regions. Figures 1(c) and 1(d) show the SEM and a three-dimensional schematic of the final device. For the growth and fabrication details, see

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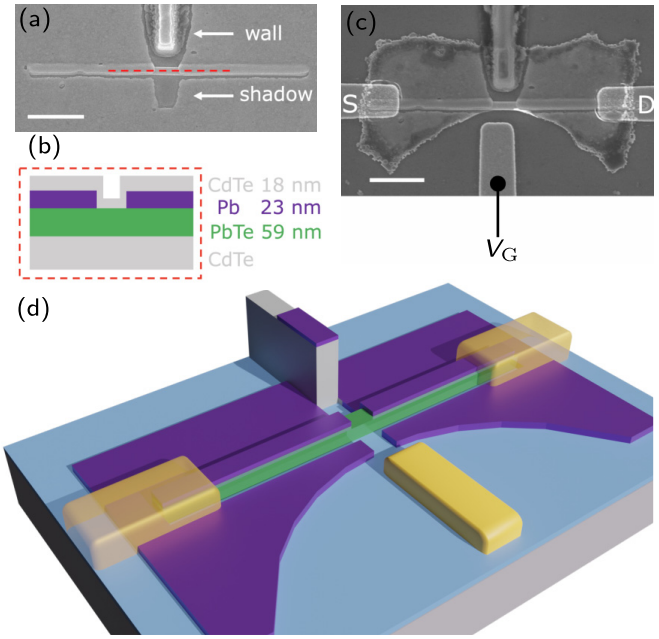

FIG. 1. (a) SEM of a PbTe-Pb nanowire. Scale bar, 1 μm. (b) The JJ schematic, cut at the red dashed line in (a). Layer thickness on the right. (c) SEM of device *A*. Scale bar, 1 μm. Contacts and gate, Ti/Au (10/65 nm). (d) Device schematic.

Appendix A. The device was measured in a dilution fridge, base temperature of $T \sim 15$ mK, using the standard two-terminal method.

II. JOSEPHSON SUPERCURRENT

Figure 2(a) shows the I-V characteristic of the JJ as a function of gate voltage (V_G). The "white triangle" is the gate-tunable supercurrent, see Fig. 2(b) for line cuts. A series resistance (R_{series}), including the filters (∼3.5 kΩ) and contact resistance (∼400 Ω), is subtracted from the raw two-terminal I-V curve, see Fig. S1 in the Supplemental Material [41]. The current sweeps from negative to positive. The switching current I_s is defined by the jump from the superconducting to the resistive branch. I_s of 78 nA translates to a Josephson energy $E_J = \hbar I_c/2e \sim 160$ μeV, well exceeding the typical E_J (90 μeV) for a gatemon [2]. We expect the critical current I_c to be close to I_s since the fridge T is much less than E_J (∼1.8 K). The "switching point" from the resistive to the superconducting branch (the negative current bias) defines the retrapping current I_r. I_r is close to I_s, suggesting that the JJ is in the overdamped regime.

To study the PbTe-Pb interface transparency, Fig. 2(c) shows an I-V curve over a larger I range. The linear fit (red dashed line) for $V > 2\Delta$ scales with the normal-state resistance $R_n \sim 941\ \Omega$. Δ is the size of the superconducting gap (see Fig. 3). The excess current, $I_{excess} \sim 307$ nA, is estimated based on the I intercept. We then calculate $eI_{excess}R_n/\Delta \sim 0.69$, which can be further used to estimate the junction transparency (∼0.65) [42,43]. Figure 2(d) shows the transparency as a function of V_G. The transparency [equals to $1/(1+Z^2)$] is calculated by solving the equation of Z: $eI_{excess}R_n/\Delta = 2(1+2Z^2)\tanh^{-1}[2Z\sqrt{(1+Z^2)/(1+6Z^2+4Z^4)}][Z\sqrt{(1+Z^2)(1+6Z^2+4Z^4)}]^{-1} - 4/3$ [44]. The red (blue) dots used I_{excess} and R_n extracted from the positive (negative) bias axis in Fig. 2(c). The maximum transparency exceeding 0.8 indicates a high quality PbTe-Pb interface. Note that the extracted transparency here is probably underestimated since Δ of 0.42 meV (in the tunneling regime) is used. Δ in the open regime is smaller (see Fig. 3). For detailed analysis of I_{excess}, I_s, and R_n, see Fig. S2 in the Supplemental Material [41].

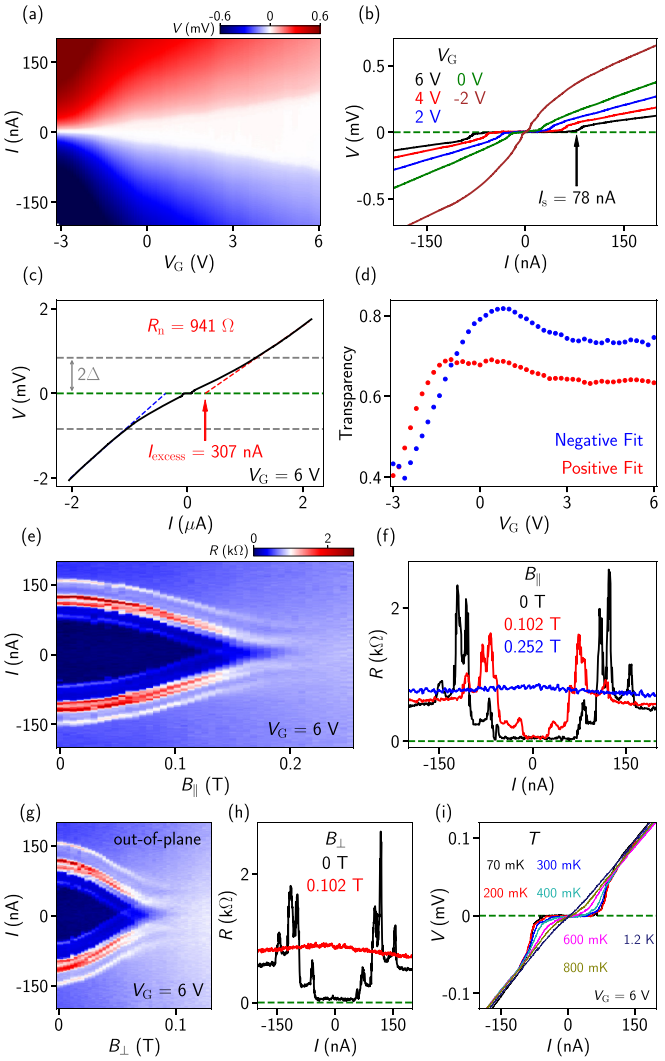

FIG. 2. Supercurrent in the open regime of device *A*. (a) I-V characteristic as a function of V_G. $B = 0$ T. (b) Line cuts from (a). (c) I_{excess} and R_n estimations of an example I-V trace. (d) Estimated PbTe-Pb interface transparency. Red and blue dots are based on the I_{excess} and R_n extracted from the positive and negative bias branches, respectively. (e) R versus I and B. $R = dV/dI$. B is parallel to the nanowire. (f) Line cuts from (e). (g) R versus I and B. B is perpendicular to the substrate. (h) Line cuts from (g). (i) T dependence.

Figures 2(e) and 2(f) show the magnetic-field (B) dependence. B is roughly parallel to the nanowire. For clarity, the differential resistance $R = dV/dI$ is presented. I_s decreases monotonically, suggesting that the orbital effect in PbTe does not play a significant role. In Fig. S3 of the Supplemental

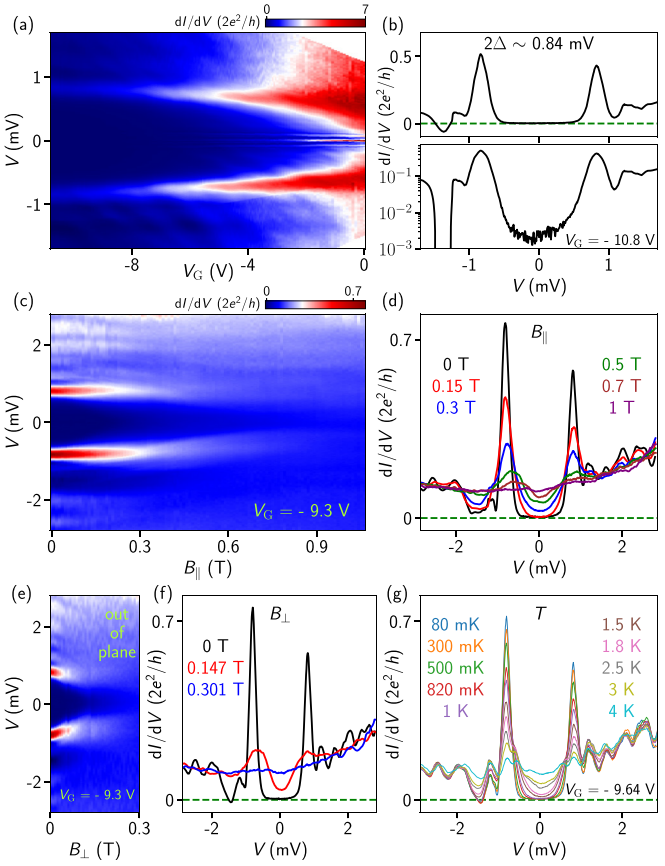

FIG. 3. Superconducting gap in the tunneling regime of device *A*. (a) dI/dV versus V for more negative V_G. $B = 0$ T. (b) A line cut in the tunneling regime, plotted in linear (upper) and logarithmic (lower) scales. (c) B (parallel to the nanowire) dependence of the gap. (d) Line cuts from (c). (e) B is perpendicular to the substrate. (f) Line cuts from (e). (g) T dependence of the gap.

Material [41], we show another device, which resolves clear supercurrent interference possibly due to the orbital effect. In Figs. 2(g) and 2(h), B is aligned perpendicular to the substrate (Pb film), and the supercurrent is suppressed at ~0.07 T. This field value is roughly consistent with the critical field (0.08 T) of the bulk superconductor Pb. For the parallel B, the critical field is two times larger, indicating less orbital effect in the Pb film (the effective Pb area perpendicular to B is smaller due to the thinness of the film). The multiple peaks are subgap features, a likely result from multiple Andreev reflections (MARs) [45]. For completeness, we show the T dependence of the supercurrent in Fig. 2(i). The supercurrent is fully suppressed at $T \sim 1$ K, much smaller than that of the bulk Pb (~7 K).

III. HARD SUPERCONDUCTING GAP

Driving V_G more negatively lowers the junction transmission and reaches the tunneling regime. The differential conductance dI/dV resolves the superconducting gap as shown in Fig. 3(a). The two peaks, symmetrically located at $V \sim \pm 0.84$ mV, correspond to the 2Δ coherence peaks, see Fig. 3(b) for the line cut. The negative differential conductance outside the gap (next to the coherence peak) is typical for S-NW-S devices (S for superconductor and NW for nanowire) [9]. The subgap conductance reaches zero (close to the measurement noise), suggesting a hard gap. The conductance ratio for outside gap versus subgap is close to two orders of magnitude. Note that for S-NW-S devices, the tunneling conductance reflects the convolution of two density of states (DOS). To directly reveal the superconducting quasiparticle DOS, an N-NW-S device (N for normal metal) is more appropriate. More positive V_G in Fig. 3(a) reveals a sharp zero-bias conductance peak, caused by the supercurrent. The other subgap peaks in Fig. 3(a) are likely MARs [45] (see Fig. S2 in the Supplemental Material [41]).

The size of the induced gap $\Delta \sim 0.42$ meV is significantly smaller than the bulk gap of Pb, estimated based on the formula $\Delta = 1.76 k_B T_c \sim 1.1$ meV ($T_c \sim 7$ K). In a recent work on InAs epitaxially coupled to Pb [46], an induced gap of 1.1–1.5 meV is reported with the Pb film thickness being 9–50 nm. As a comparison, our Pb film thickness is ~23 nm. The relatively small-induced gap suggests that the PbTe-Pb JJ is in the intermediate coupling regime rather than the strong-coupling regime. The advantages and disadvantages for strong and intermediate couplings have been extensively studied in theory [47–50]. Most of the current hybrid nanowires (InAs-Al, InAs-Pb, and InSb-Al) are in the strong-coupling regime. Our device provides a platform for the intermediate coupling case, shedding light on, e.g., the role of disorder in the superconductor [51,52].

Another notable feature in Fig. 3(a) is the variation of the gap size: The gap "shrinks" for more positive V_G's (see Fig. S2 in the Supplemental Material [41]). We have independently calibrated the fridge filters and confirm that this shrink is not due to an overestimation of R_{series} and its shared bias voltage. A possible explanation for the shrink is the gate-tunable superconductor-semiconductor coupling [53]. More positive V_G "drags" the electron wave functions more into the PbTe (less in Pb), leading to a smaller induced gap. Although the side gate has a "finger" shape, the large dielectric constant of PbTe can bend the electric field lines such that V_G can also tune the proximitized PbTe parts [39].

Figures 3(c)–3(f) show the B dependence of the gap, resolving a critical field of ~0.9 T for parallel B and ~0.3 T for perpendicular B. The difference indicates the reduced orbital effect for parallel B. To achieve higher critical field, thinner (~10-nm) Pb film is desired [46]. The critical field of the gap in Fig. 3 is much larger than the critical field of the supercurrent in Fig. 2, possibly due to the induced gap in the tunneling regime being larger than that in the open regime.

The small oscillations outside the gap in Figs. 3(d) and 3(f) [also visible in Fig. 3(a)] are reminiscent of those in Ref. [54]. Since the PbTe-Pb interface is rather flat, the oscillations are likely caused by the nonuniform CdTe substrate. Although the substrate was initially flat, PbTe growth requires heating the substrate to 318.5 °C to have selectivity. This temperature can evaporate/decompose part of the CdTe substrate, resulting in a rough PbTe-CdTe interface (see Fig. S4 in the Supplemental Material [41]). The rough substrate can cause electron backscattering and those Fabry-Pérot-like oscillations. This nonuniformity is random and surely degrades the device quality (e.g., junction transparency) and should be minimized in future optimizations. In Fig. S3 in the Supplemental

Material [41], we show two additional devices (*B* and *C*), which cannot be pinched off, possibly due to this random substrate disorder. When the substrate disorder level is high and creates many carriers, the device becomes metalliclike. The gate can no longer pinch the JJ off. The bipolar gate dependence of the supercurrent in Fig. S3(g) in the Supplemental Material [41] resembles the metallic supercurrent field-effect transistors [55,56], consistent with the interpretation above. The difference among devices *A* and *B* and *C* suggests that better and more controllable device growth is needed in future studies to minimize the substrate disorder. For reproducibility, we show two more devices (*E* and *F*) in Fig. S5 in the Supplemental Material [41]. The main feature of device *A* can also be resolved in those two devices: a gate-tunable supercurrent in the open regime and a superconducting gap in the tunneling regime.

Figure 3(g) shows the T dependence. The gap is completely "washed out" at ∼4 K. The small oscillations, however, are still present. This is consistent with our interpretation above: The normal scattering (Fabry-Pérot-like) can have a different energy scale than the superconducting correlations. In Figs. 3(d) and 3(f), the oscillations can be suppressed, possibly due to the accumulated phases induced by *B*.

IV. TEM CHARACTERIZATION

After the transport measurement, we cut the device using a focused ion beam and performed the high-resolution scanning transmission electron microscopy (STEM). Figure 4(a) shows the image of the cross-sectional lamella from another device (device *B*). The lamella of device *A* was damaged by the focused ion milling (see Fig. S4 in the Supplemental Material [41]). Devices *A* and *B* were grown and fabricated together (on one same substrate chip). The transport study of device *B* is shown in Fig. S3 in the Supplemental Material [41]. The HAADF image in Fig. 4(a) clearly shows different material layers with sharp interfaces. The green arrow points to a dark line region in the CdTe(001), likely the residue of Ar treatment during the substrate cleaning. By growing the CdTe buffer before PbTe, we can "bury" this disordered region in the CdTe, away from the PbTe nanowire. We find that this buffer growth can significantly improve the device quality compared to our previous study [36]. The violet arrow indicates a corner of the Pb film, which was damaged during the lamella preparation. For additional STEM analysis on device *B*, see Fig. S6 in the Supplemental Material [41].

Figures 4(b)–4(d) show the atomically resolved STEM images at three key interfaces: the Pb-CdTe (capping), the PbTe-CdTe (substrate buffering) and the PbTe-Pb. The PbTe and CdTe are lattice matched [Fig. 4(c)]. The PbTe-Pb interface is also sharp but with mismatched dislocations. This disorder could be reduced in the future by growing a thin layer of CdTe between the PbTe and the Pb growth. The CdTe capping in Fig. 4(b) prevents the oxidation of the Pb film underneath. The lattice mismatch between Pb and CdTe is a disorder source in the superconductor, which may enhance the proximity effect [47]. The EDX maps of the four elements Pb, Te, Cd, and Si (for the dielectric mask) are shown in Figs. 4(e)–4(h). Both the STEM and the EDX suggest little interlayer diffusion.

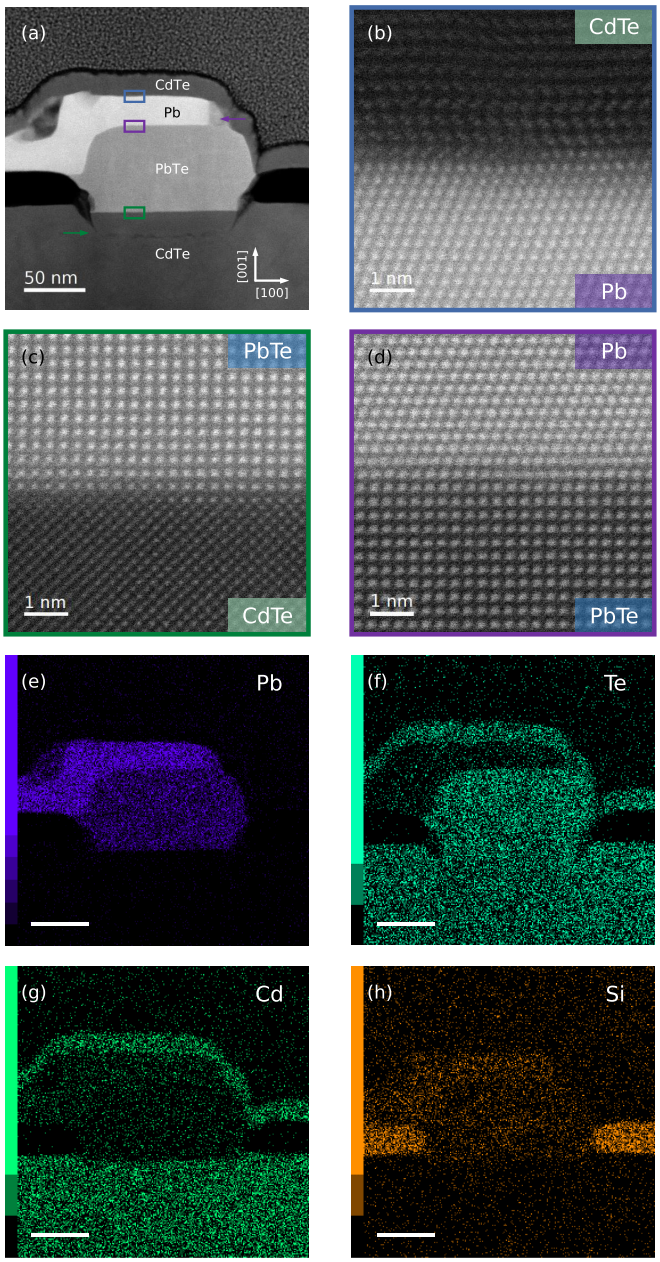

FIG. 4. STEM analysis of device *B*. (a) The high-angle annular dark field (HAADF) image of the nanowire cross section with crystal directions labeled. (b) Atomically resolved image near the Pb-CdTe (capping) interface, see the blue box in (a). (c) Image of the PbTe-CdTe interface, see the green box in (a). (d) Image of the PbTe-Pb interface, see the violet box in (a). (e)–(h), energy-dispersive x-ray spectroscopy (EDX) maps of Pb, Te, Cd, and Si, respectively. Scale bar, 50 nm.

V. CONCLUSION

To summarize, we have studied the superconducting proximity effect in PbTe-Pb hybrid nanowires. Josephson junction devices based on this hybrid can reveal a gate-tunable supercurrent in the open regime and a hard-induced superconducting gap in the tunneling regime. Although the device is far from perfect, and more optimizations are desired (e.g., substrate uniformity), our paper shows that the combination

of PbTe and Pb could work as a new material platform for Majorana searches.

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APPENDIX: DEVICE GROWTH AND FABRICATION

1. Substrate fabrication

Shadow walls and markers. Hydrogen SilsesQuioxane (FOx-16, Dow Corning), the HSQ resist, was spun onto the CdTe (001) substrate at 2000 rpm for 60 s and then baked at 150 °C for 60 s. An electron-beam lithography (EBL) was then performed to write the shadow-wall and marker patterns. The chip was immersed in tetramethylammonium hydroxide for 180 s to dissolve the unexposed resist regions.

Si_xN_y mask. The chip was then covered by a thin film of Si_xN_y (30–40 nm) using the plasma-enhanced chemical vapor deposition. Then AR-P 672.045 resist was spun at 4000 rpm for 60 s and baked at 130 °C for 10 min. Another EBL was performed to write the designed nanowire trenches and the markers (for alignement during the device fabrication). The chip was then developed in an Isopropanol (IPA) solution, MIBK:IPA=1:3, for 40 s. Reactive ion etching (CHF_3 with O_2) was used to etch away the trenched regions of the Si_xN_y film. The resist was removed in acetone, and the substrate was cleaned in oxygen plasma for 8 min at a power of 60 W. The CdTe chip covered by a Si_xN_y mask was ready for the next stage growth.

2. Selective area growth of PbTe nanowires and Pb deposition

PbTe nanowires. The chip was loaded into an ultra-high-vacuum MBE chamber (base pressure less than 2.0×10^{-10} mbar). To remove the native oxide layer of CdTe, Ar bombardment was performed at a beam energy of 0.9 keV and a beam current density of 0.7 $\mu A\,cm^{-2}$. The chip was then annealed at ∼250 °C for 50 min. A CdTe buffer layer was grown at ∼270 °C with a beam flux of ∼10 nm/h. Then, PbTe nanowires were grown at ∼320 °C with a beam flux of ∼0.6 nm/min under Te atmosphere.

Pb deposition. The Pb film was *in situ* deposited at another sample stage in the same MBE chamber. The substrate was cooled to ∼100 K with liquid nitrogen during the deposition. Finally, a CdTe layer (10–15 nm) was grown to cap the entire chip. To prevent discontinuous island formation of the Pb film, a good thermal contact between the liquid-nitrogen stage and the sample holder (tight clamp) is needed. In addition, the CdTe capping should be performed right after the Pb film growth at liquid-nitrogen temperature before warming up. In this way, a continuous thin Pb film (sub-10-nm-thick) can be obtained.

3. Device fabrication

Pb etching. To prevent a short circuit between the source and the drain electrodes, most of the Pb film on the substrate needs to be etched away. First, the device regions were manually coated by the AR-P 671.05 resist using a toothpick. Pb film on the edges was then etched in an ATC-IM ion milling system (Ar ion milled for 260 s). The resist was removed in acetone. The chip was coated by a bilayer of AR-P 671.05 at 4000 rpm (∼490-nm thick for each layer). Then, the resist was vaccum pumped (no hot plate baking) followed by an EBL to write the etching patterns. After developing in diluted MIBK for 50 s and IPA for 30 s, a second ion milling was performed to remove the Pb film on the substrate near the nanowire. The resist was removed in acetone.

Contacts and gate. The standard EBL was performed to evaporate Ti/Au (10/65 nm). Resist, 490-nm-thick AR-P 671.05. Before evaporation, argon etching (160 s, 50 W, 5.4×10^{-2} Torr) was performed in the load lock to remove the CdTe capping in the contact regions. Lift-off in acetone overnight, followed by IPA and nitrogen gun blow dry.

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