Controlling the fixed negative charge formation in Si/high-*k* interfaces

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High-*k* dielectrics Al_2O_3 and HfO_2 are widely used in combination with Si to produce electronic components and solar cells. A negative fixed charge is known to appear at Si/high-*k* material interface after high-temperature annealing, yet the formation mechanism of the negative charge is poorly understood. In this work, we investigate the parameters affecting the charge formation to provide a better understanding and control of the charge in deposition and postprocessing steps. We observe negative charge formation in the interface after annealing by capacitance-voltage measurement. We demonstrate the effects of annealing temperature and high-*k* film thickness on the charge formation. We further discuss the mechanism of the charge formation and present results supporting one recently suggested mechanism explaining the negative charge as an acceptor state in the interface. We observe a structural modification of the interface produced by annealing with photoelectron spectroscopy as a core-level shift in SiO_2 binding energy. We investigate the electrostatic potential and electron distribution in the interface by *ab initio* calculations to understand the effect of the structural modification on the electronic structure of the interface.

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I. INTRODUCTION

Metal oxide semiconductor (MOS) junctions are the basic building blocks found in many semiconductor components such as transistors and memory cells. The MOS structures have been successfully utilized in components for decades by improving them along the way. High-*k* dielectric materials, e.g., Al_2O_3 and HfO_2, were introduced to semiconductor component production to replace the previously utilized SiO_2 to allow below sub-1-nm equivalent oxide thickness (EOT) [1,2]. Even though high-*k* metal oxides have been successfully applied to devices for a relatively long time, not all of their properties are well understood yet. One of these properties is a fixed negative charge, which can appear when the high-*k* materials are integrated into the Si surface. The charge has been previously observed and it is even utilized in, e.g., solar cell passivation to generate field-effect passivation to the cell surface to reduce electrical losses due to Si surface defects [3,4]. However, the origin of the negative charge is still unknown although the formation mechanism and effects of the charge have been investigated in several studies. Understanding the origin of the charge and the formation mechanism is important in order to control the charge formation during MOS structure fabrication and later processing steps [5,6]. The specific subject of charge formation is also relevant in general in understanding the physics of the MOS structure [7]. In this study, we have investigated the conditions in which the negative charge forms in the MOS structure to understand the formation mechanism.

A fixed negative charge is typically observed in Si/high-*k* material interfaces after annealing. During device manufacturing, these interfaces are subjected to many such annealing steps which may generate the negative charge [8]. Thus, it is important to understand the formation mechanism in order to avoid charge formation as the charge can deteriorate the device performance. On the other hand, solar cell structures are annealed on purpose to generate the negative charge that creates a passivating electric field on the Si surface. In this so-called field-effect passivation, the negative charge generated to the Si/high-*k* material interface pushes electrons in the interfacial Si toward the Si bulk away from the interface defects increasing the carrier lifetime significantly [4]. By understanding the charge formation process, the processing conditions can be optimized to maximize the interface charge without degrading the cell structure in the process.

The negative charge is widely observed in different types of Si/Al_2O_3 junctions ranging from solar cells to MOS transistor gates. The negative charge is also observed in Si/HfO_2 material system, even though HfO_2 is considered to be charge neutral material with Si as the two have the same coordination number [9,10]. Several different mechanisms for charge formation have been presented of which two mechanisms have gathered the most support. The first mechanism explains the charge formation as an interface dipole caused by the junction of two different materials, contributing the charge generation to the bond between the two different materials [11]. In this mechanism, the dipole could form, e.g., because of variation in electron screening at the interface or because of different band offsets of the materials [10,12]. However, it is yet unclear how such mechanisms could be caused by annealing the interface. The second mechanism explains the charge formation

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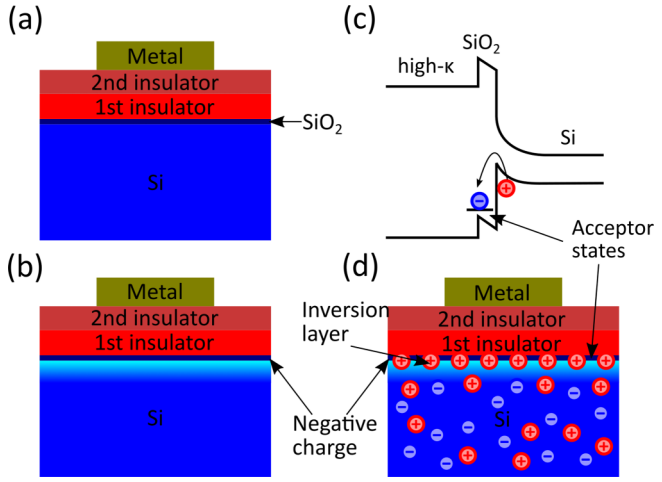

FIG. 1. Schematic figure of the multilayer stack and presentation of the negative charge, electronic structure, and carrier distribution in the modified interface. (a) Sample stack structure including multilayer insulator structure and naturally occurring SiO_2 layer. (b) Location of the negative charge and its induced electric field in the topmost Si atom layers. (c) Electronic structure of the stack with negative charge with the previously proposed acceptor state [15]. (d) The carrier distribution on the *n*-type sample with the negative charge demonstrating the inversion layer formation.

by an intermediate interface material causing the charge. The intermediate interfacial material forms at the interface during the annealing by reactions and bonding between silicon, interfacial Si oxides, and the high-*k* material [13,14]. The material introduces electronic states in the interface, which are the cause of the negative charge. One likely explanation is an acceptor state in the SiO_2 gap below the Si valence band, which forms because of SiO_2 and high-*k* material bonding. The acceptor level located below the Si valence band maximum traps an electron, which would be the source of the negative fixed charge [6,15,16]. Figure 1 shows a schematic of the charge formation Si/high-*k* insulator interface and the carrier distribution in the structure. Recent studies support this mechanism either directly describing a similar mechanism or by attributing the negative charge to a structural modification although describing it as an interface effect [5,17]. Our results in this study support the structural modification and acceptor state formation mechanism. In this study, we have investigated the formation mechanism and structure of the intermediate interfacial material.

Several explanations have been provided for the mechanism taking place at the Si/high-*k* interface. Different Al or Hf coordination number is a possible explanation for the source of the negative charge [10,16]. The high-*k* materials deposited by atomic layer deposition (ALD) are typically observed to be stoichiometric and amorphous. However, the interface part may not be stoichiometric because of initial growth conditions leaving the possibility of having O defects in the interface [1,10]. Especially, the postannealing can change the Al or Hf coordination by introducing oxygen vacancies or interstitials. Oxygen vacancies can be generated by reactions between interfacial Si atoms and O from the high-*k* layer [13]. Such reactions would produce an interface alloy with more interfacial SiO_x and reduce the Al or Hf to a more metallic state [6]. Furthermore, the reactions could generate an acceptor state in the SiO_2 gap [15,18–20]. An increase of SiO_2 in the interface after annealing supports this [6]. On the other hand, O interstitials in the Si/high-*k* interface have been suggested as one possible source of the negative charge. The interstitial oxygen could remain as a point defect in the amorphous ALD films and cause the charge as they are negative ions [8]. However, the negative charge formation by ultrahigh vacuum (UHV) annealing and observation of increased interfacial Si oxide after the UHV annealing oppose the idea of interstitial oxygen causing the negative charge. In such annealing conditions, interstitial oxygen would be reduced as the diffusion of external elements is excluded and the remaining interstitial oxygen would react to form the Si oxide [6,21]. Finally, similar charge formation is observed also in MOS structures other than high-*k* oxide, in which the charge formation mechanism might be similar to the mechanism in the Si/high-*k* system [7].

Charge formation requires postannealing in relatively high temperatures above 300 °C, which further indicates that structural modification of the interface is behind the negative charge. The required postannealing temperature is higher than the ALD deposition temperature, thus indicating annealing-induced structural modification. Such modification could be for example internal diffusion or rearrangement of the Si/high-*k* interface [5,8,13,14,21,22]. A small amount of charge observed without high-temperature postannealing can be attributed to high deposition temperature or other processing steps such as postmetallization annealing. Postannealing is also observed to reduce the interface defect density D_{it} [8,23]. D_{it} states are the defect-induced levels in the Si gap, which act as recombination centers and interface trap states. After the high-*k* deposition, the interface is not in an energetically favored state. The postannealing allows these energetically unfavorable states to be modified and the proposed acceptor states are generated simultaneously. However, the acceptor levels are different from the D_{it} as the acceptor levels are located in the SiO_2 band gap below the Si valence band [8,15]. Higher postannealing temperatures up to 500 °C will lead to a higher charge. In this study, we have investigated postannealing temperatures in the range 250–500 °C to investigate the effect of temperature on charge formation. Incremental annealing steps were utilized to observe the charge increase.

The thickness of the active interface layer producing the negative charge is not yet known. Investigations of the SiO_2 interlayer thickness suggest that several-nanometer thickness reduces the amount of negative charge observed from the interface [24,25]. Controlling the negative charge by controlling the SiO_x layer thickness has been suggested [25,26]. Moreover, a high charge has been observed from the interface prepared with as little SiO_2 as possible [6]. These results suggest that the small amount of SiO_2 which unavoidably forms in the interface during high-*k* deposition is enough for the charge formation. However, the thickness of the required high-*k* material is yet unclear. In this study, we investigated the effect of high-*k* material thickness on the charge formation by annealing high-*k* layers with different thicknesses on Si to generate the charge to the interface. The layers were capped with a thicker nonannealed high-*k* layer to fabricate MOS

capacitors. We also attempted to observe the altered material structure within the interface by x-ray photoelectron spectroscopy (XPS), which would give us information about the effect of the material thickness on the alloying of the interface.

The presence of a fixed charge in the interface can be observed with MOS-capacitance measurement. A fixed negative charge pushes majority carriers away from the interface deeper into the silicon bulk in *n*-type silicon. This creates a layer of minority carriers, i.e., depletion region, to the interface. The minority carrier layer acts as a reservoir from which the minority carriers can contribute to the MOS capacitance. Typically, in the MOS-capacitance measurement without the fixed charge, no response, i.e., no capacitance in inversion, is observed from the minority carriers with high, over 1 kHz, measuring frequencies. This results from the minority carrier lifetime, which is too long for the carriers to be generated and recombined fast enough to respond to the measurement signal. However, the minority carriers from the reservoir can respond to the measurement signal by moving in and out of the reservoir layer. Thus, the negative charge causes a low-frequency-like capacitance to appear at high frequencies. The minority carriers move from outside of the capacitor contact area to under it and back to the reservoir allowing the capacitor to charge and discharge at high frequencies [27]. Thus, the mechanism has been named peripheral inversion [5]. The negative charge induced inversion capacitance has distinct behavior, which allows us to separate it from other types of interface effects in *CV* measurement. The capacitance will decrease as a function of frequency as fewer minority carriers can respond to the measurement signal and the response from the bulk minority carriers is lost because of slow generation and recombination. The capacitance will also decrease as a function of contact area as the ratio between circumference and area reduces, thus fewer minority carriers per area can contribute to the charging and discharging of the capacitor. Inversion capacitance will also saturate to a constant value as a function of bias voltage when the depletion region reaches the inversion layer bottom. This allows distinguishing negative charge induced inversion capacitance from the inversion capacitance caused by interface traps, which reduces at higher bias voltages [5,27].

II. EXPERIMENTAL METHODS

The samples were 6×12 mm Si pieces from *n*-type 10-Ω cm CZ wafer. The samples were cleaned with standard RCA clean and the surface oxide was removed with 5% hydrofluoric acid prior to loading them into ultrahigh vacuum (UHV) equipment to avoid any contamination and preserve the surface of the sample as oxygen free as possible. The dielectric materials were deposited by ALD in a reactor connected directly to the UHV system. Al_2O_3 was deposited at 180 °C using trimethylaluminum and water as precursors. HfO_2 was deposited at 130 °C using tetrakis-dimethylamidohafnium and water as precursors. The precursor water was type 1 ultrapure water with resistivity over 20 MΩ cm. The multilayer samples were prepared with two separate ALD depositions with the charge generating annealing at 400 °C in between the depositions in the UHV system without breaking the vacuum. After deposition, the sample was taken out from the UHV system. The insulator thickness was measured with an ellipsometer. MOS capacitor samples were prepared by sputter-coating circular 200-μm-diameter Cr/Au pads on top of the oxide using a shadow mask. After metal deposition, the samples underwent 250 °C postmetallization annealing in UHV. Samples for XPS measurement were prepared with a single thin high-*k* layer and the samples were annealed in the UHV system after deposition without breaking the vacuum.

The charge-generating annealing for the samples was done in the UHV system at several postannealing temperatures. *CV* and D_{it} measurements were carried out with an HP 4284A LCR meter and leakage current was measured with an HP 4145B semiconductor parameter analyzer. D_{it} was obtained by measuring conductance and capacitance as a function of frequency and bias voltage. D_{it} was extracted at the maximum conductance using conductance approximation [28]. XPS spectra were measured from samples with different high-*k* layer thicknesses to observe the effect on the interface material structure when the negative charge is generated. XPS measurement was carried out using a monochromated Al Kα source with $h\nu = 1487$ eV photon energy. The XPS spectra were analyzed with the ORIGIN 2016 program by removing the Shirley background shape and fitting Voigt peak functions to the spectra. Known binding energy shifts for Si oxidation state components were used in the analysis [6,29].

III. COMPUTATIONAL METHODS

Ab initio density functional theory (DFT) computations were carried out to better understand the structural properties of the interface and the electronic state formation in the interface. The computational studies were carried out with the Vienna Ab-initio Simulation Package (VASP) program using the projector augmented wave method (PAW) and Perdew-Burke-Ernzerhof (PBE) functionals [30]. In the calculations, the plane wave cutoff energy was set to 500 eV and the structures were relaxed to 10^{-3} eV/Å. The structural models were built using diamond Si(100), β-cristobalite SiO_2, and tetragonal models for HfO_2 and Al_2O_3. The models were lattice-matched together by rotating the β-cristobalite SiO_2 cell by 45° [31]. The tetragonal models for the insulators were chosen to allow lattice matching with the tetragonal Si/SiO_2 structure. The calculation requires periodic, i.e., crystalline, structure, even though the oxides used in experiments are amorphous. Similar models have been utilized in similar calculations previously [12,31]. The negative charge generating structural modification was introduced by substituting one Si atom in the SiO_2 with Al or Hf ion. Both bulk and slab models were built of similar structures to investigate the electrostatic potential and charge distribution. Slab model calculations included a 10-Å vacuum on the top and bottom of the cell to calculate the vacuum level potential. Thus, different models could then be compared with each other by aligning the electrostatic potential with the vacuum potential. Bulk models were constructed to calculate the electron distribution in the interfaces to understand the acceptor state formation and field-effect passivation by adding a free electron to the relaxed structure. Bulk models included two equivalent interfaces to accurately model the interface effect.

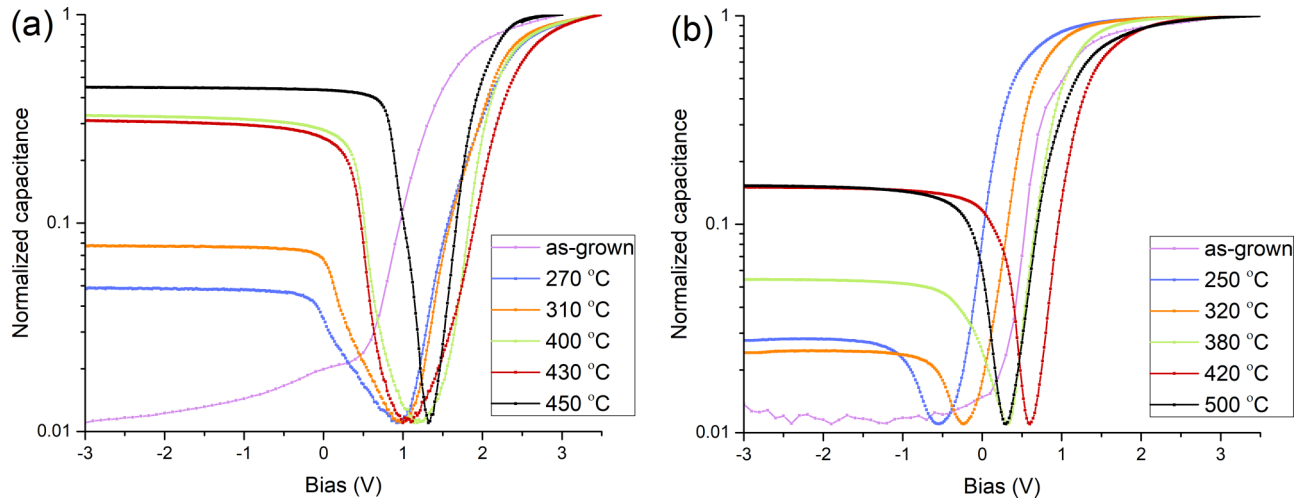

FIG. 2. High frequency *CV* curves measured at 1 MHz from samples with 6 nm (a) Al_2O_3 and (b) HfO_2 dielectric after postannealing at different temperatures. Inversion capacitance is seen to increase with increasing temperature. Inversion is on the negative bias, i.e., on the left side.

IV. RESULTS AND DISCUSSION

Investigation of the annealing temperature gives us information about the formation conditions of the negative charge. High-frequency *CV* curves of samples with 6 nm oxide measured at 1 MHz after charge generating postannealing with different temperatures are shown in Fig. 2. A significant charge is generated already in 300−400 °C temperature, which is observed as an increased capacitance value at the negative bias side, i.e., at inversion. An additional charge can be gained by using even higher temperatures. This information suggests that the structural modification will happen at below 400 °C in the interface and an additional charge could be gained by increasing the annealing time [8]. In Fig. 2, a shift of the *CV* curve accumulation step can be seen to shift toward positive bias with increasing annealing temperature. The accumulation step position can be used to estimate flat band (FB) voltage, which suggests an increase of negative charge as the step moves toward positive bias. Notably, the step position moves back toward negative bias at the highest annealing temperatures systematically although the capacitance value at inversion is not reduced. Furthermore, the accumulation step in the *CV* curve becomes steeper with higher annealing temperatures indirectly indicating lower electrical losses in the interface, i.e., lower interface defect density. Based on these results we expect that the observed FB shift toward negative bias at high temperatures is linked to the other changes in the interface that we observe as steepening of the accumulation step and thus the negative charge is not reduced in the interface at high temperatures.

The thickness of the interfacial material generating the negative charge has been yet unknown. Our investigation with different high-*k* material thicknesses gives insight into the minimum required interface material thickness, which is still able to generate the charge. Figure 3 shows *CV* curves measured at 1 MHz from samples prepared with different thicknesses of high-*k* material layers subjected to charge-generating annealing. The thickness of the annealed layer is presented in Fig. 3 and the total thickness of the stack in all samples was 6 nm. The figure shows increased capacitance in the inversion, i.e., negative bias, even with a very thin charge generating high-*k* layer. However, a significantly higher charge is generated with thicker high-*k* layer thickness suggesting that the charge-generating part of the interface extends along several atomic layers in the interface. This suggests that several atomic layers of high-*k* material are required to form the negative charge-inducing defect state. However, for the negative charge to be effective in creating the inversion layer to the top of the Si, the negative charge must be located at the high-*k*/SiO_2 interface. Transferring the charge further away from the interface has been shown to quickly reduce the inversion layer [32,33]. Thus, the thickness of the high-*k* layer does not indicate the distance of the charge from the interface, i.e., the charge is not located in the high-*k* material. Previously we have observed an increase in interfacial SiO_x when the negative charge is present [6]. These results together indicate that the structural modification takes place along several atomic layers in the interface, i.e., intermediate interface material layer with significant thickness is generated. *CV* curves measured at lower frequencies are show in the Supplemental Material [34].

Interface defect density was investigated to understand the possible effect of defects on the negative charge. Interface defect state density (D_{it}) was observed to be approximately $1\times10^{13}\,eV^{-1}\,cm^{-2}$ in the samples. The defect state density was observed to be almost the same in samples with different postannealing temperatures and in multilayer samples. We note that the observed D_{it} is relatively high, which is likely why we do not observe large changes in it. We attribute the large D_{it} value to the large contact area combined with our inability to prepare the samples in a cleanroom environment, which unavoidably leads to some contamination of the MOS structure. However, we note that we do not observe the D_{it} to have any effect on the negative charge and our observations are similar to those with lower D_{it} values reported previously [6]. Moreover, the negative fixed charge is fixed interface charge Q_{fix}, thus it is not directly related to D_{it}.

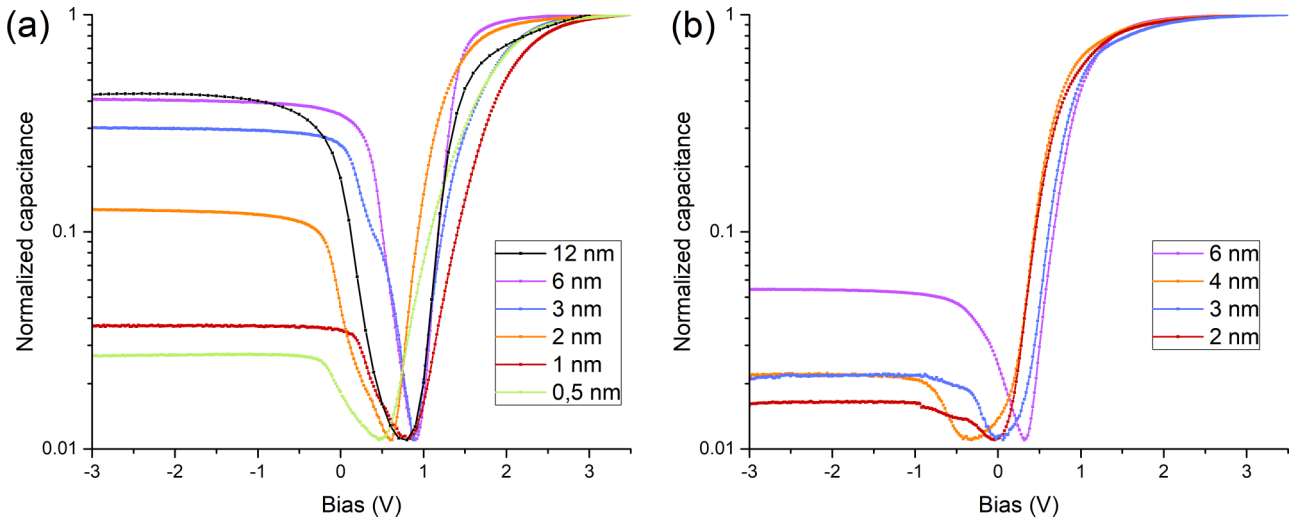

FIG. 3. High frequency *CV* curves measured at 1 MHz from samples with (a) Al_2O_3 and (b) HfO_2 dielectric having different thickness postannealed high-*k* layer. Inversion capacitance is seen to increase with thicker high-*k* layers. Inversion is on the negative bias, i.e., on the left side.

Samples with different high-*k* layer thicknesses were measured with XPS to gain information about the interface material structure. We have previously observed distinct core-level shifts on Si related to the negative charge formation using synchrotron high kinetic energy photoelectron spectroscopy [6]. Here, the aim was to investigate whether information about the material structure can be observed with a regular XPS instrument and to investigate the effect of high-*k* material thickness. Figure 4 shows XPS spectra of the oxide component of Si 2*p* spectra of a sample with 3-nm high-*k* thickness. The core-level shift toward higher binding energy is observed after annealing the sample at 500 °C, which is in agreement with the earlier observations [6]. However, a similar core-level shift was not observed from samples with thinner or thicker high-*k* layers. Especially with thicker high-*k* layers, the signal-to-noise ratio reduces too much to allow accurate analysis. This is also in agreement with our previous observation in which we observed that the photon energy significantly affects the ability to observe the core-level shift. Furthermore, by combining the result with the results from electrical measurement, we conclude that only a small amount of negative charge is generated in the interface with sub-3-nm films, as we observe small inversion capacitance and no negative fixed charge related core-level shift. Over 3-nm-thick films generate even more charge which is observed as higher inversion capacitance and also as a larger amount of core-level shift as observed in our previous study [6].

The interface material structure was investigated with DFT calculations to understand the effects of the structural modifications to the electronic properties of the interface. Based on the experimental evidence that the negative charge formation is caused by a structural rearrangement in the interface, the structural modification was modeled by alloying the interfacial Si oxide and the high-*k* material. Additionally,

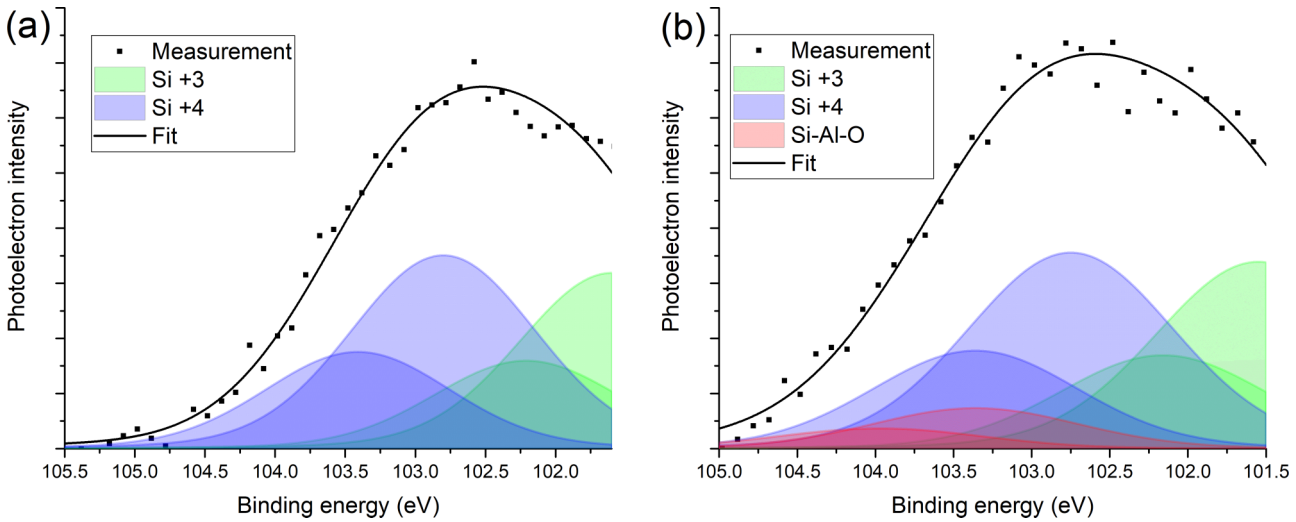

FIG. 4. XPS spectra of Si 2*p* oxide component measured from (a) before and (b) after annealing from a sample with a 3-nm Al_2O_3 insulator layer. The double component arising from the interfacial modification is seen in (b) in red.

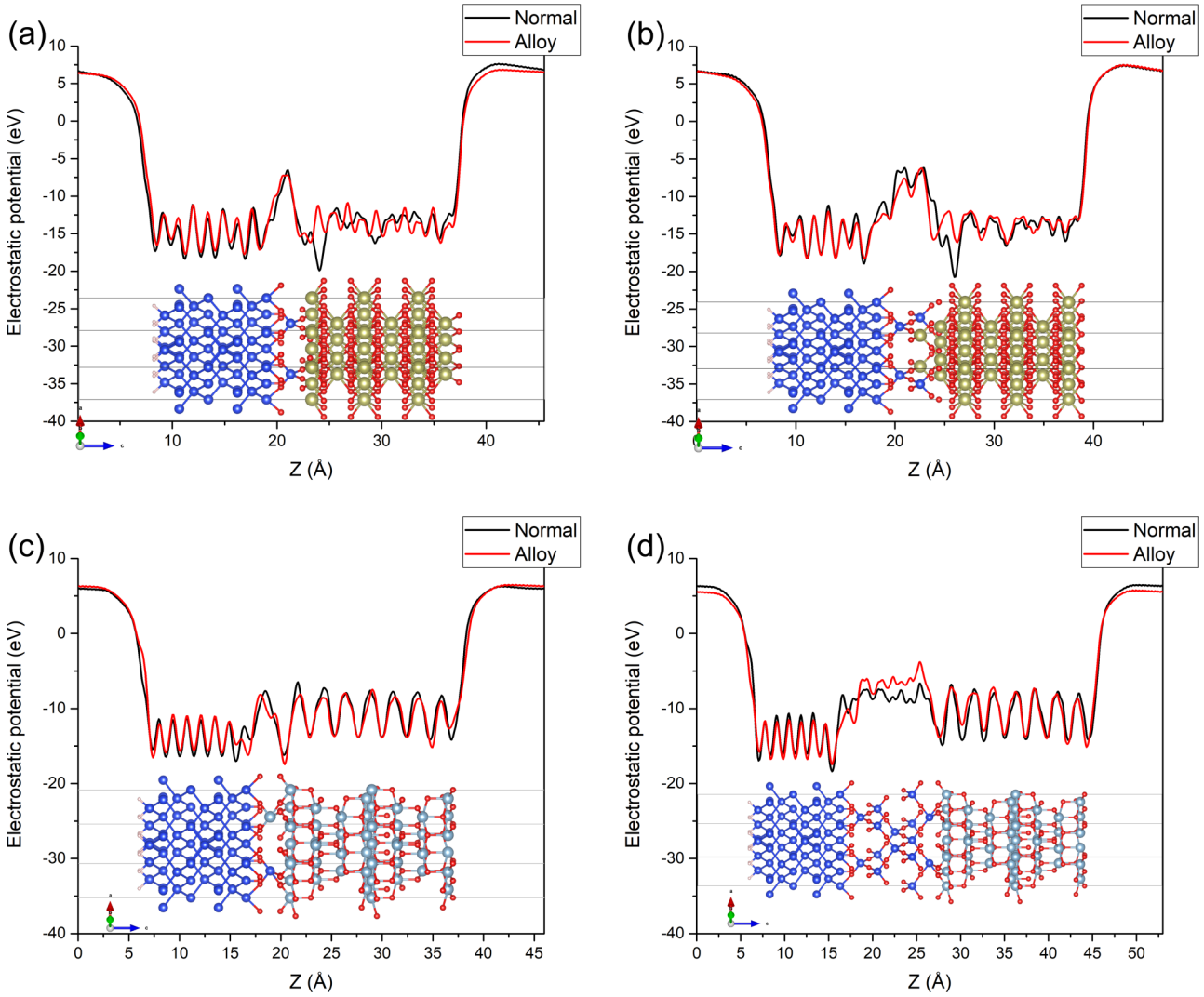

FIG. 5. Comparison of electrostatic potentials of alloyed and nonalloyed interfaces from slab models with (a), (b) HfO2 and (c), (d) Al2O3 dielectrics. Small local differences in the electrostatic potential are seen mostly on the Hf and Al side with thin interfacial SiO_2 in (a), (b), and (c). A larger difference in the potential is seen in (d) in the Al_2O_3 system with thicker interfacial Si. Atom colors in the figure are Si: blue; Al: light blue; Hf: yellow; O: red; and H: white. The alloyed interface with substitution is presented in (b) and (c) and the nonalloyed interface is presented in (a) and (d) for the HfO_2 and Al_2O_3 respectively.

previous studies have shown that the most likely position of the negative charge inducing defect is in the Si oxide and high-*k* interface [5,10,15]. The models were built for both $Si/SiO_2/Al_2O_3$ and $Si/SiO_2/HfO_2$ systems. The alloying was modeled as a substitution of one Al or Hf atom in the SiO_2. This assumption was justified by the previous experimental observation of the increase of interfacial Si oxide during the negative charge generating annealing, which was attributed to the interfacial Si reacting with the oxygen in high-*k* material to form more interfacial Si oxide and form Si-Al or Si-Hf bonds [6,13]. SiO_2 thickness was varied between one and five atomic layers in the models to investigate the effect of the amount of interfacial Si oxide and to understand the position and formation mechanism of the expected acceptor state in the interface. Such thickness covers the practical thickness range, which could form during the insulator deposition and during the subsequent negative charge generating annealing.

Figure 5 shows a comparison of electrostatic potential in the investigated interfaces. The calculations show an increase in the average electrostatic potential, which is in agreement with the core-level shift observed by XPS. The less negative electrostatic potential increases the binding force of electrons, which is observed as a core-level shift toward higher binding energy in the XPS measurement. In the calculations, the electrostatic potential shows differences even with very thin SiO_2 layers indicating that the substitutional alloying modifies the electrostatic potential effectively. However, the most significant differences are seen with the thicker SiO_2 layer, which is in agreement with the earlier XPS result showing increased SiO_2 after the negative charge generating annealing. Notably, the largest difference in the electrostatic potential is at the substitution in all models indicating that the alloying is a likely cause for the observed core-level shift.

To investigate the suggested acceptor state formation mechanism further, we calculated bulk models with an

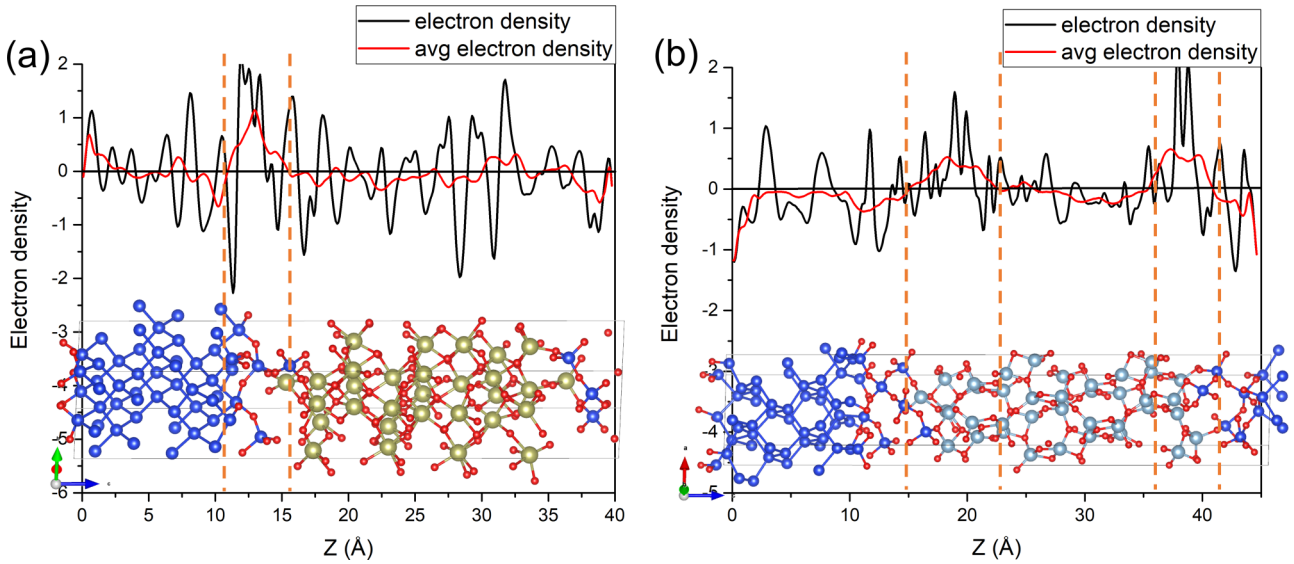

FIG. 6. Difference of electron density with an additional free electron in alloyed and nonalloyed models having (a) HfO_2 (b) Al_2O_3 insulator. The figure shows increased electron density in the interface region suggesting acceptor state presence in the interface. The area with increased electron density is highlighted with orange dashed lines. Atom colors in the figure are Si: blue; Al: light blue; Hf: yellow; O: red; and H: white. Both structures are alloyed structures with the Al or Hf substitution in the SiO_2.

additional electron. Figure 6 shows a comparison of electron distribution in the interface with an additional free electron. The distribution shows the additional electron sticking to the alloyed part of the interface. The result indicates an acceptor state in the interface to which the free electron is attracted. The electron distribution also shows a small reduction in electron density near the topmost Si layer in the interface suggesting that a depletion region forms in the Si near the interface. Such depletion region would result in the field-effect passivation effect, which is observed from the interfaces with the negative charge present. Thus, the observation of higher electron density in the alloyed region links the acceptor state formation and the experimentally observed field-effect passivation together. Although the models have equivalent interfaces, differences in the electron density between the interfaces can be seen. Specifically, the free electron distributes evenly to both interfaces in the model with Al_2O_3 but binds to one of the interfaces in the model with HfO_2. We expect this to be caused by relaxation to a slightly different structure, thus making one of the interfaces more optimal to function as the acceptor state.

The local density of states (LDOS) of the computational models was studied to understand the effects of the substitution on the band structure. Figure 7 shows a comparison of the LDOS of the models presented in Fig. 6. The density of states shows the Si band bending toward lower energy as presented in Fig. 1(c) while the band gap of high-k insulator and SiO_2 remain constant. In the $Si/SiO_2/Al_2O_3$ model, the Si bands bend from the middle of the Al_2O_3 band gap toward the valence band maximum (VBM) of the Al_2O_3. In the $Si/SiO_2/HfO_2$ model, the Si bands bend from the vicinity of the HfO_2 conduction band minimum (CBM) toward the mid gap of the HfO_2. The observed band bending of bulk Si is 1.5 eV for the system with Al_2O_3 and 0.65 eV for the system with HfO_2, which would suggest higher charge formation in the system with Al_2O_3. This is in agreement with the experimental observation in Figs. 2 and 3 in which higher inversion capacitance, i.e., higher charge, is observed. Notably, the band offset is seen throughout the bulk Si suggesting it to be a long-range effect in the Si bulk. In the Al_2O_3 LDOS, gap states can be seen in the SiO_2 band gap below the Si valence. These states could be evidence of the proposed acceptor state in the SiO_2 gap, and their location at 0.5 eV below the Si valence band maximum matches closely the acceptor state proposed in previous research [15]. However, the LDOS from the HfO_2 model does not show a similar clear gap state although the band bending is present.

Our results attribute the origin of the negative charge to an acceptor state which originates from a specific material structure in the Si/high-k interface [10,15]. On the other hand, many studies attribute the charge to a dipole that forms in the material interface [11,12,32,33]. The dipole is often discussed with the flat-band voltage of the MOS structure. However, the interface dipole and the acceptor state mechanism are essentially separate from each other, and in an ideal interface, the interface dipole cannot produce the long-range effect which we observe extending from the interface into the Si bulk. A dipole naturally occurs in an interface between two materials with different amounts of electrons. However, such dipole is well defined between the bonding atoms, for example, Si-O-Al. A dipole that forms between, e.g., positive and negative ions at the interface has a well-defined point like beginning and end and the field decays rapidly outside of the line between the ions. Thus, the electric field from such dipole cannot reach other parts of the materials outside the interface, and thus such dipole cannot generate the inversion layer that we observe on the Si side. On the other hand, an electron trapped in an acceptor state does not form a well-defined dipole as the electron originates from the Si and thus the compensating charge lies in the bulk Si. Thus, the electric field from the trapped electrons can have a broader long-range effect toward the compensating charge at Si bulk. Notably, some papers name a defect state induced electric field as a

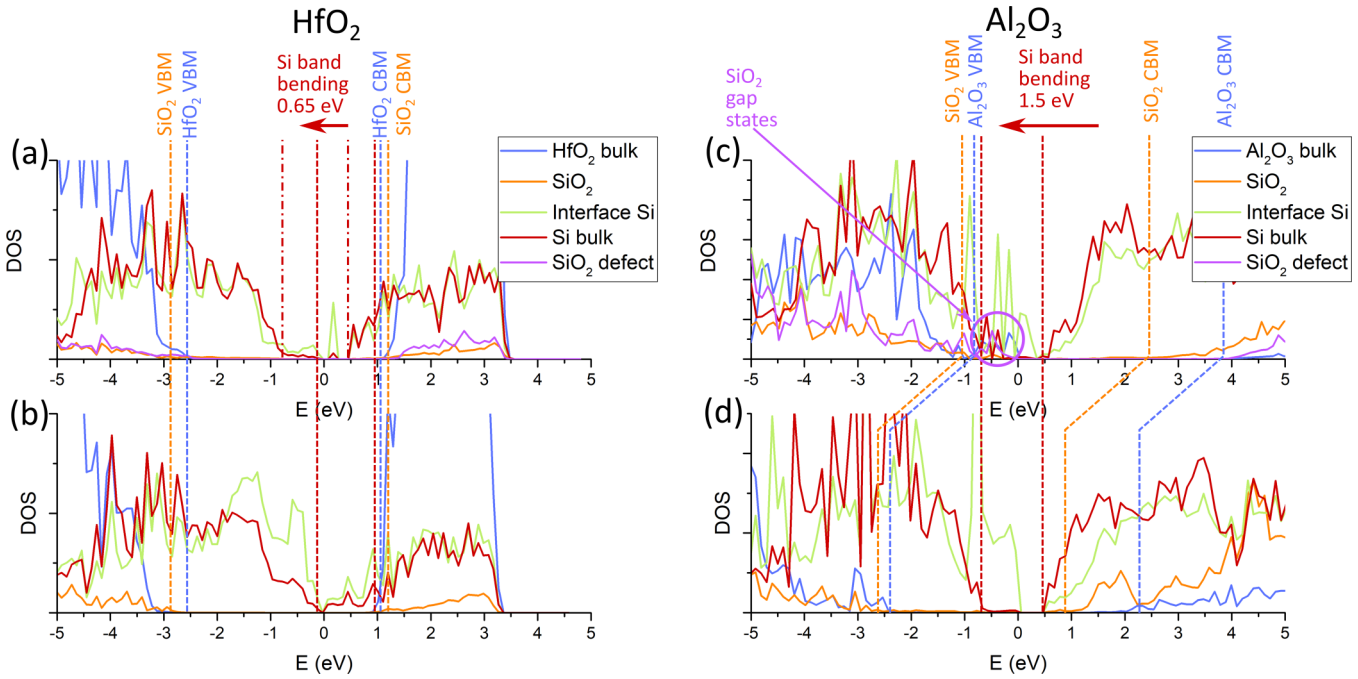

FIG. 7. LDOS calculated from different parts of the models from Fig. 5 (a), (c) with and (b),(d) without the substitution. The LDOS shows band bending of the Si bands in both models as the band gap of the Si is shifted to lower energy compared to the insulator band gaps in the models with the substitution. The individual LDOS has been calculated for HfO_2 and Si bulk from the most distant atoms away from the interface, for Si from the first Si-Si bonded layer from the interface, for SiO_2 from Si atom with Si-O-Si bond, and for SiO_2 defect from the substitution atom location. Zero energy is selected as the highest occupied state energy in the calculation.

dipole [10]. However, such a naming convention can be seen as misleading, because the defect state induced field does not have a well-defined beginning in the Si bulk, thus it is not a well-defined dipole. Finally, it is worth noting that an interface may include a dipole, which may cause a change in the observed flat-band voltage of a MOS capacitor. However, such dipole cannot cause a long-range electric field and thus cannot generate a depletion region outside the interface. On the other hand, the inversion capacitance increases and saturation to a constant value at high frequencies are key fingerprints of the long-range effect in the MOS capacitor characteristics [5].

V. CONCLUSION

In this study, we have investigated parameters controlling the negative charge formation in Si/HfO_2 and Si/Al_2O_3 interfaces during postannealing. A significant negative charge is generated to the interface at relatively low temperatures below 400 °C, which are used in processing steps after the high-k material deposition in many applications. A more negative charge can be obtained with higher postannealing temperatures up to 500 °C. The thickness of the annealed high-k layer also significantly affects the amount of charge generated. The high-k layer with thickness below 3 nm generates significantly less charge than thicker films. The results are in agreement with earlier observations attributing the negative charge to an intermediate material structure that forms to the interface during the postannealing. The modified interface material can be observed in XPS measurement exclusively from a sample with a 3-nm insulator layer. Acceptor state formation to the interface has been previously described to be the origin of the negative charge. The results in this study are in agreement with the acceptor state model suggesting the acceptor state formation being linked to the material modification of the interface. The results from the calculations indicate that such structural modification of the interface would be observed in the XPS as a core-level shift. Furthermore, the calculations show that such structural modification would create an electron state in the vicinity of the interface to which electron trapping is energetically favored, i.e., an acceptor state in the modified interface. The acceptor state causes the expected band bending in the top Si layers creating the experimentally observed inversion layer.

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