Doubling the mobility of InAs/InGaAs selective area grown nanowires

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Selective area growth (SAG) of nanowires and networks promise a route toward scalable electronics, photonics, and quantum devices based on III-V semiconductor materials. The potential of high-mobility SAG nanowires however is not yet fully realised, since interfacial roughness, misfit dislocations at the nanowire/substrate interface and nonuniform composition due to material intermixing all scatter electrons. Here, we explore SAG of highly lattice-mismatched InAs nanowires on insulating GaAs(001) substrates and address these key challenges. Atomically smooth nanowire/substrate interfaces are achieved with the use of atomic hydrogen (a-H) as an alternative to conventional thermal annealing for the native oxide removal. The problem of high lattice mismatch is addressed through an $In_xGa_{1-x}As$ buffer layer introduced between the InAs transport channel and the GaAs substrate. The Ga-In material intermixing observed in both the buffer layer and the channel is inhibited via careful tuning of the growth temperature. Performing scanning transmission electron microscopy and x-ray diffraction analysis along with low-temperature transport measurements we show that optimized In-rich buffer layers promote high-quality InAs transport channels with the field-effect electron mobility over 10 000 cm^2 V^{-1} s^{-1}. This is twice as high as for nonoptimized samples and among the highest reported for InAs selective area grown nanostructures.

I. INTRODUCTION

For the past decades semiconductor nanostructures have been an important materials platform for nanoelectronics and mesoscopic quantum transport [1–3]. The nanoscale confinement can be realized following various routes: by local electrostatic gating of two-dimensional heterostructures, using top-down processing, or by vapor-liquid-solid growth, where nanostructures grow out of plane of a substrate and the confinement is achieved by a nanoscale catalyst particle. Recently, selective area growth (SAG) of semiconductor structures and heterostructures has emerged as an appealing platform for the realization of electronic, optoelectronic, and photonic devices [4–9]. In the SAG approach, the material growth occurs in lithographically predefined openings formed in a layer of amorphous mask on a semiconductor substrate. The advantages of SAG include control over shapes, dimensions, positions, and faceting of the final structures [10,11]. Moreover, improved crystal quality of SAG materials as compared to their planar counterparts has been demonstrated [8,12].

The SAG approach has been used to successfully grow out-of-plane nanowires and nanofins as well as in-plane nanowires, nanomembranes, nanoprisms, nanorings, and quantum dots combining low-band-gap III-V and more exotic II-V materials with high-band-gap semiconductor substrates [9,10,13,14]. In-plane SAG of InAs and InSb nanowires attracts special attention for applications in quantum transport as controllable and scalable nanowire networks can be readily achieved [5,15–24]. Since structures are already grown horizontally in plane of the substrate, it also simplifies their device processing.

However, while the growth of continuous SAG nanowires and networks hosting ballistic transport thought the junctions has recently been demonstrated [16], issues related to surface/interface quality and material intermixing limit the electron mobility.

For example, the substrate fabrication process combined with the native oxide removal in the mask windows by thermal annealing prior nanowire growth also provoke interfacial roughness and voids in the substrate [5,6,25]. Although surface relaxation allows for the growth of highly lattice-mismatched materials, networks of misfit dislocations may still occur for certain materials combinations, dimensions, and growth conditions [5,21,26]. A way to address this issue is to use buffer layers to accommodate the mismatch,
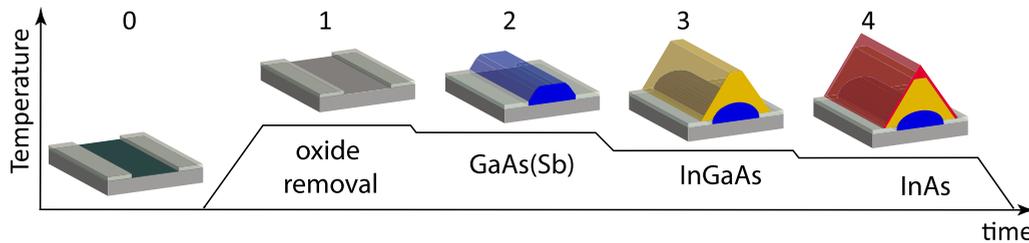
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FIG. 1. Schematics of growth steps of InAs/InGaAs/GaAs(Sb) SAG nanowires on GaAs(001) substrates covered with a 10-nm thick SiO_2 mask. 0. Substrate fabrication; 1. Native oxide removal; 2. GaAs(Sb), 3. InGaAs and 4. InAs layer growth. Note that the originally faceted GaAs(Sb) buffer becomes rounded after the growth of InGaAs and InAs layers on top.

as recently demonstrated for GaSb buffer layers between InAs SAG nanowires on GaAs substrates [4,15]. However, the GaSb buffer is electrically conducting and it complicates applications in transport devices. Finally, material intermixing between layers is inherent to heteroepitaxial systems and it leads to degrading mobility [27–33]. Recent reports on SAG of InAs/GaAs nanowires showed dramatic 50-80% Ga in nominally pure InAs active regions [18,24].

In this paper, we focus on SAG of highly lattice-mismatched InAs nanowires grown by means of molecular beam epitaxy (MBE) on GaAs(001) substrates and address the challenges stated above. We introduce an $In_xGa_{1-x}As$ buffer between conducting InAs and insulating GaAs and improve substrate cleaning prior to growth. Owing to material intermixing, $In_xGa_{1-x}As$ buffers are highly diluted with Ga, and nominally pure InAs channels consist of ternary In(Ga)As alloys prior to the optimization. By reducing the growth temperature, we suppress the Ga-In material intermixing achieving $In_xGa_{1-x}As$ buffer layers with high In content and pure InAs channels. In-rich buffers promote InAs/$In_xGa_{1-x}As$ interfaces with high crystal quality. This is directly reflected through measured electron mobility, which is doubled as compared to the nonoptimized samples, reaching record high values of 12 550 cm^2 V^{-1} s^{-1} for selective area grown InAs nanostructures [5,14,34].

II. RESULTS AND DISCUSSION

The sequence of growth steps leading to high-quality InAs SAG nanowires is shown in Fig. 1. We use undoped GaAs(001) substrates. The nanowire geometry is controlled by defining windows in a 10-nm silicon dioxide (SiO_2) mask layer. The substrate fabrication (step 0) follows the Ref. [5] except for the etching process. We use inductively coupled plasma with a mixture of tetrafluoromethane (CF_4) and hydrogen (H_2) gases to reveal the pattern instead of hydrofluoric acid for better controllability of the process. See Sec. S1 in the Supplemental Material (SM) [35] for the growth details of each step.

A. Oxide removal and GaAs(Sb) buffer growth

We first started by optimizing the procedure of removing the native oxide from the bottom of GaAs windows prior nanowire growth (step 1, Fig. 1). The standard approach for the oxide removal is thermal annealing, which degrades the surface due to the temperature activated transformation of

the stable Ga_2O_3 into the volatile Ga_2O by consumption of GaAs [36–40]. The results are 15–30 nm deep pits as seen in Figs. 2(a) and 2(b) ("step 1:T") (see Sec. S2 in SE [35]). The root-mean-square (rms) roughness of the GaAs surface in the growth windows increases from 0.31 ± 0.11 nm after etching to 3.18 ± 0.35 nm after annealing. In conventional thin film epitaxy, the surface topography after thermal annealing can be improved by growing thick buffer layers. In the SAG samples, however, we find that the pits underneath the oxide mask often do not get filled during growth leaving voids easily distinguished in scanning electron microscopy (SEM) [black stripes in Fig. 2(c)] [5,6,21,24]. These voids can potentially degrade SAG-based device performances and thus are unacceptable for many device applications.

There are several alternative ways of removing the native oxide from GaAs including group-III assisted annealing [41,42] or atomic hydrogen (a-H) [43]. Here, we investigated the use of a-H, which is known to produce atomically smooth GaAs surfaces in thin film epitaxy owing to significantly reduced temperatures required for the Ga_2O_3 to Ga_2O transformation and at the same time it also facilitates the reduction of the carbon contamination [25,44] (see Sec. S2 in SM [35]). As shown in Figs. 2(a) and 2(b) ("step 1:a-H"), exposing GaAs growth windows to 3.0×10^{-5} mbar a-H at 350 °C for 15 min results in atomically smooth GaAs surfaces with 0.37 ± 0.14 nm rms roughness without affecting the surrounding oxide mask. Our findings show that a-H is an ideal approach to smoothly remove the native oxide from substrates partially covered by an oxide mask used in SAG.

The second step in the process is the growth of a GaAs(Sb) buffer layer where Sb is used as surfactant. It was found that this step is essential for improving electronic transport properties of InAs/GaAs SAG nanowire devices [5]. GaAs(Sb) nanowires grown on substrates prepared with a-H are shown in Fig. 2(d). The nanowires grow continuously indicating that the native oxide was removed successfully. Figure 2(e) shows the topography across a typical GaAs(Sb) nanowire grown in a 220-nm-wide [1$\bar{1}$0]-oriented growth window measured with atomic force microscopy (AFM). The nanowire has a height of 30 nm above the trench and exhibits a flat top (001) facet with the rms roughness of 0.275 ± 0.015 nm. The side facets were assigned to {113}A and {112}A crystal planes based on the slope (see Sec. S3 in SM [35]). We note that {112}A facets are not expected from the equilibrium crystal shape (ECS) model for GaAs grown without any surfactants [45–47]. Instead, low-energy {111}A facets are predicted and observed experimentally [Fig. 2(e)] [48]. One
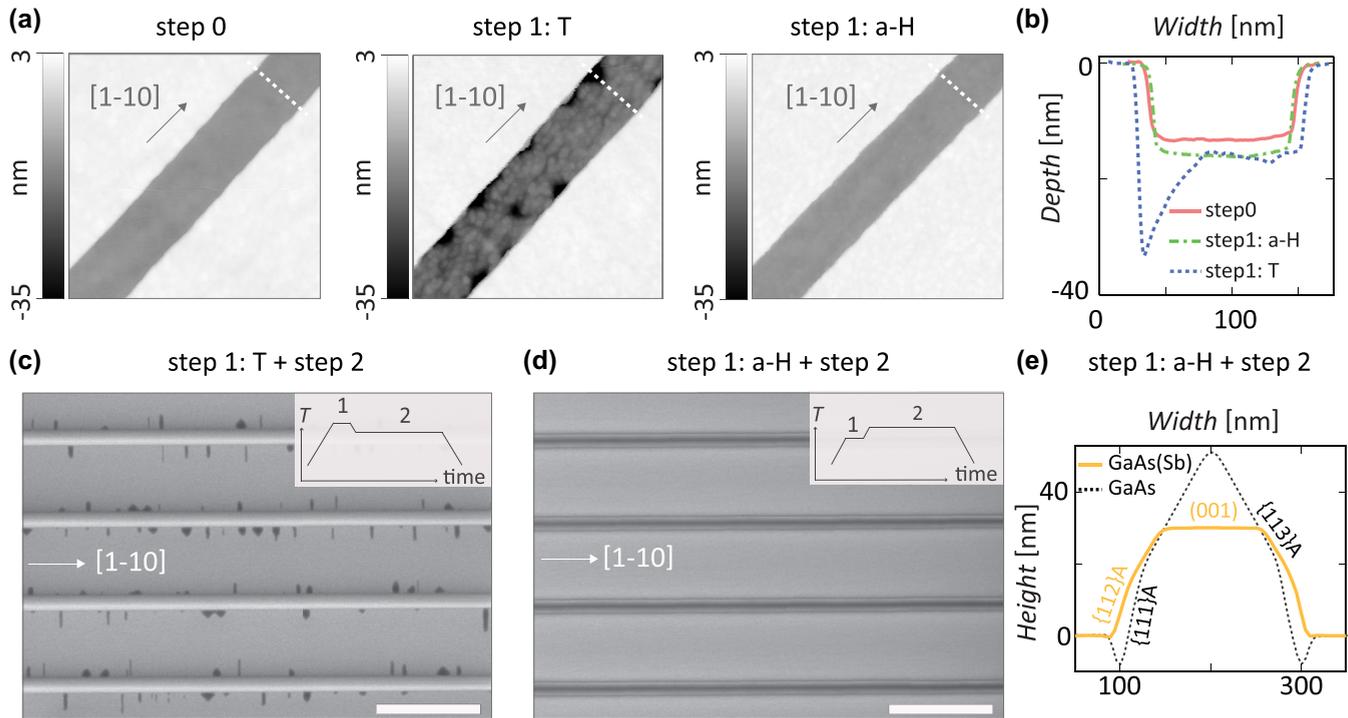
FIG. 2. (a) A set of AFM images (0.5×0.5 μm^2 image size) demonstrating a [1$\bar{1}$0]-oriented GaAs growth window (trench) with a native oxide (step 0), after thermal oxide desorption (step 1: T), after atomic hydrogen oxide removal (step 1: a-H). White dashed lines indicate the position of AFM profiles shown in (b) and averaged over 15 nm. Top-view SEM images (1 μm scale bar) of GaAs(Sb) SAG nanowires grown on a GaAs(001) substrate from which the native oxide was removed either thermally (c) or with a-H (d). The insets show relative temperature T of oxide removal with respect to the GaAs(Sb) growth step with the latter being fixed at 600 °C. (e) AFM profile across a typical GaAs(Sb) SAG nanowire with step 1: a-H showing a faceted structure. AFM profile across a GaAs SAG nanowire grown without Sb surfactant but otherwise identical growth parameters is shown for comparison.

possible explanation is that the facet angle is underestimated in our experiment owing to only a small fraction of the side facet being available. On the other hand, it is likely that the presence of Sb surfactant changes both thermodynamics (reducing the surface energy) and kinetics (increasing the surface diffusion of Ga adatoms on the facets) of the growing nanowires [49–54].

B. In$_x$Ga$_{1-x}$As buffer growth

To accommodate the lattice mismatch between the GaAs substrate and the InAs active region and to trap misfit dislocations away from InAs, we introduce an In$_x$Ga$_{1-x}$As buffer layer sandwiched between GaAs and InAs (step 3, Fig. 1). Such approach is extensively used in planar semiconductor structures [55,56], but it has not yet been adopted for SAG nanowires. A high In content x is required for the lattice matching. At the same time, the buffer must be electrically insulating, which favours lower x, leading to the need for a compromise. A set of InAs/In$_x$Ga$_{1-x}$As/GaAs(Sb) samples were grown in a temperature range from 520 °C to 540 °C to investigate the Ga-In material intermixing and in the following $x = 0.9$ was kept fixed. The bounds of the temperature range were dictated by the selectivity window [21]. The growth parameters of GaAs(Sb) and InAs layers were kept identical for all the samples (see Sec. S1 in the the SM [35]).

Figure 3(a) shows an STEM micrograph using the high-angle annular dark-field imaging mode (HAADF) taken across four [1$\bar{1}$0]-oriented InAs/InGaAs/GaAs(Sb) nanowires grown at 522 °C. The nanowires protrude out of the growth window with a slight lateral overgrowth on the SiO$_2$ mask (the layer with the darkest contrast in this imaging mode). The cross section is symmetrically formed by the (001) top facet, {111}A (and small inclusions of {111}B), {113}A, and {110} side facets as can be seen in STEM images and supported by simulated atomic model in Sec. S4 in SM [35] [57] and the ECS model [47]. Note that the InGaAs layer is grown without any surfactants and the {111} family of facets is observed in place of the {112} family seen for the first buffer layer. The EELS analysis in Fig. 3(b) reveals the presence of the GaAs(Sb) buffer layer, followed by an In$_x$Ga$_{1-x}$As region and a ~15–20-nm-thick InAs layer. Generally, the GaAs(Sb) layer has a rounded shape without the clear side facets observed earlier in the reference GaAs(Sb) nanowires [Fig. 2(e)]. Moreover, its surface in the vicinity of the substrate as well as the substrate are eroded [black arrows in Fig. 3(b)]. The In$_x$Ga$_{1-x}$As buffer layer has two regions with a distinct composition: the bottom Ga-rich part with x ~ 0.5 at the InGaAs/GaAs(Sb) interface [visible as cyan flames in Fig. 3(b)] and the upper In-rich part with x ~ 0.8. Additional EELS maps are shown in Sec. S4 in SM [35]. Finally, Fig. 3(c) shows the In composition profile extracted along the ($\bar{1}\bar{1}$1)A nanowire facet [white arrow in
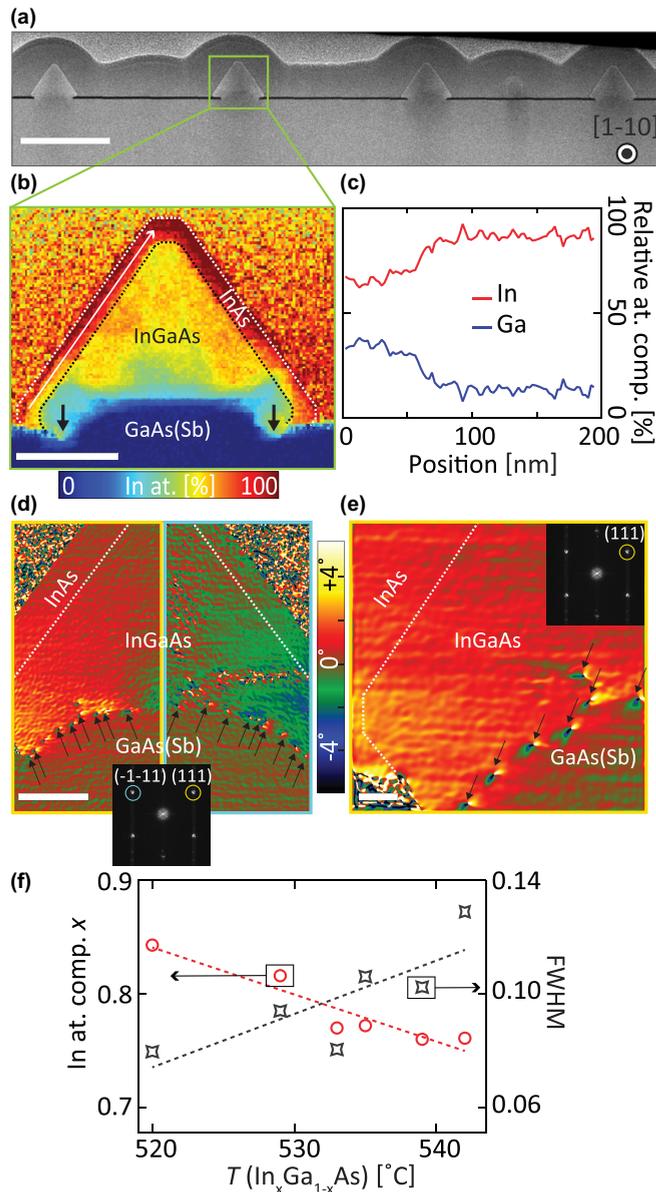
FIG. 3. The role of InGaAs growth temperature on the composition and crystal properties of the InAs/InGaAs/GaAs(Sb) SAG nanowires. (a) Low magnification HAADF-STEM image (scale bar, 500 nm) of a lamella taken across [1$\bar{1}$0]-oriented field-effect nanowires grown at 522 °C. (b) In atomic distribution EELS map (relative to Ga, in atomic percentage; scale bar, 100 nm) of the nanowire from (a). Arrows indicate the place of erosion of GaAs(Sb) and GaAs. (c) Relative Ga and In atomic composition profile along the ($\bar{1}\bar{1}1$) facet in the InAs channel from (b). [(d),(e)] GPA rotational maps of the nanowire from (b) representing its central part (50 nm scale bar) and the left corner (10 nm scale bar). Misfit dislocations at the InGaAs/GaAs(Sb) buffers are highlighted with black arrows. The insets show the corresponding fast Fourier transform (FFT) with the analysed planes: (111) planes correspond to the left half and ($\bar{1}\bar{1}1$) planes to the right half of the image in (d). (f) x in the buffer as a function of the buffer growth temperature T extracted from XRD reciprocal space maps. The peak broadening representative of the compositional variations in the buffer measured as FWHM is plotted as well. The dashed lines are linear fits and are guides to the eye.

Fig. 3(b)] inside the nominally pure InAs channel. x drops from ∼0.9 at the top of the nanowire to x ∼ 0.65 on its sides at the interface with the Ga-rich buffer region. This suggests that there is a constant flow of Ga, which diffuses towards areas with abrupt change in composition, and thus highly strained, creating diluted InGaAs alloys. As shown later, the InAs/InGaAs interface is mainly dislocation free suggesting that the intermixing provides efficient strain relief for the system.

Similar phenomena of diffusion and material intermixing activated at high-growth temperatures in strained epitaxial systems have earlier been reported in quantum dots [31–33], free-standing axial nanowires, and in-plane nanowires grown on nanomembranes [18,24,58,59]. Among possible mechanisms, bulk diffusion and surface diffusion have been suggested. In the case of Ge/Si quantum dots, it has been shown by both experiment and simulations that at standard growth temperatures the material for intermixing is provided by surface erosion of the Si substrate creating depressions around the growing system [32,33,60]. As the bulk diffusion of Ga is negligible at the growth temperatures used in the current work [61], we conclude that Ga is supplied from the surface of the GaAs(Sb) buffer and/or the underlying GaAs substrate, consistent with the observed surface erosion, similar to the Si/Ge case.

Overall, from EELS analysis we find that the sample grown at the highest growth temperature has on average the lowest In concentration in the InGaAs buffer for both [1$\bar{1}$0]- and [100]-oriented nanowires, indicating that the strain-driven Ga-In material intermixing is promoted by elevated temperatures.

To investigate the crystal quality of the samples, we employ Geometric Phase Analysis (GPA) on high-resolution HAADF-STEM images. Figures 3(d) and 3(e) show GPA rotational maps (planes bending with respect to the substrate). An array of misfit dislocations is seen at the InGaAs/GaAs(Sb) interface. We also find 1–2 stacking faults per nanowire cross section. They originate at the dislocated interface on the sides of the nanowire. Some part of the mismatch strain is released elastically via a ∼2° bending of planes close to the nanowire corners. The latter is possible owing to free side walls of SAG nanowires similar to free-standing nanowires [62]. On the other hand, the InAs/InGaAs interface, highlighted with dashed lines exhibits a high crystalline quality. Over four analyzed samples, we find only 1–2 misfit dislocations over the entire InAs/InGaAs interface. These are always found at the corners of the nanowires, between the Ga-rich flames and the InAs channel.

Our findings highlight the importance of the In-rich InGaAs buffer layer introduced between the InAs channel and the GaAs substrate. With the composition range obtained in this work, we estimate that the lattice mismatch between the InAs channel (containing on average 10% Ga as extracted with EELS) and the In$_x$Ga$_{1-x}$As buffer reduces from 1% to 0.47% by reducing the buffer growth temperature. The latter allows to extend the critical thickness from only a few monolayers for InAs/GaAs interfaces to ∼18 nm for InAs/InGaAs interfaces before misfit dislocations are introduced (for pure edge dislocations [63]). This is an important step forward toward high-quality InAs SAG nanowires [5,21].
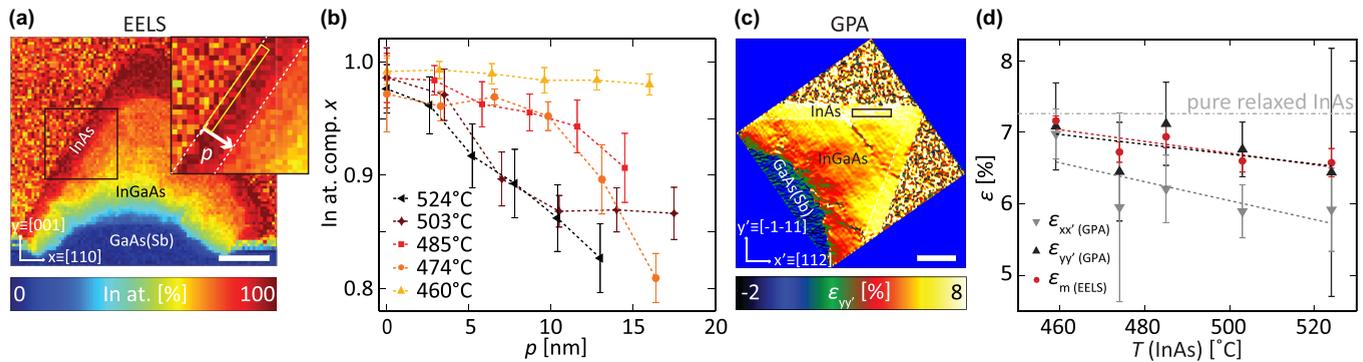
FIG. 4. Influence of the growth temperature on the InAs channel composition. (a) In atomic composition EELS map (relative to Ga; scale bar, 50 nm) of the sample with InAs channel grown at 485 °C. Inset: zoomed area of the channel indicating the procedure to obtain data points in (b). (b) In atomic composition x extracted at position p across the InAs channel grown at five different temperatures. For each growth temperature six data points are extracted. Each data point is taken at the position p and averaged over 100 nm [see inset in (a)]. The averaging gives the standard deviation as error bars. (c) An example of the out-of-plane lattice mismatch map ($\varepsilon_{yy'} = \Delta d_{(\bar{1}\bar{1}1)}/d_{(\bar{1}\bar{1}1)}$) obtained with GPA (scale bar, 50 nm; GaAs is the reference) for the nanowire from (a). x axis is rotated 54.75° with respect to the original direction: $x' = x + 54.75°$ (x' is parallel to the InAs/InGaAs interface, and thus to the [112] crystallographic orientation, y' is parallel to the [$\bar{1}\bar{1}1$] crystallographic orientation). (d) $\varepsilon_{yy'}$ and $\varepsilon_{xx'}$ as a function of the InAs growth temperature extracted from GPA. Each data point is averaged over a 50×10 nm^2 box and presented with standard deviations as error bars. We also plot ε_m calculated from the EELS composition assuming Vegard's law. In both cases, ε increases with decreasing InAs growth temperature. The dashed lines are a liner fit to the experimental data and are guides to the eye.

To corroborate on the composition differences between the samples, we use XRD. In contrast to EELS, where only local nanowire composition is measured through a transversal cut of 50–100 nm thickness, XRD allows to access an average In composition x of an entire layer in an array of nanowires (Sec. S4 in SM [35]). Figure 3(f) shows x in the buffer as a function of the InGaAs buffer growth temperature for the [1$\bar{1}$0]-oriented nanowires. The maximum value of $x = 0.84$ is reached at 520 °C and it gradually decreases to $x = 0.76$ at 541 °C. A similar trend is observed for the [100]-oriented nanowires. We also plot full width at half-maximum (FWHM) from XRD peaks. The broadening of the peaks can be caused by several reasons including the strain and the distribution in the chemical composition. In our experiment the InGaAs buffers are mainly plastically relaxed and the changes in the FWHM reflect the distribution in the chemical composition within the buffer [compositional variations visible in Fig 3(b)]. (See Sec. S4 in SM [35] for more images.) There is a clear tendency toward increased FWHM of x at higher growth temperatures. This shows that lower growth temperatures are beneficial for both higher In concentrations and compositional uniformity of the InGaAs buffer.

We then used XRD to extract an In composition from the InAs channels. We find $x \sim 0.89$ for all the samples in a good agreement with EELS results.

C. InAs growth optimization

As we saw before, the Ga-In material intermixing takes place not only in the bulk of the InGaAs buffer layer but also in the InAs channel [Figs. 3(b) and 3(c)]. To improve the composition homogeneity of the channel, we now optimize the growth temperature of the InAs layer. For this, five samples are grown in the temperature range between 460 and 524 °C (see Sec. S5 in SM [35] for SEM images). The InGaAs growth

temperature is fixed at 520 °C for all samples as it is found from the previous section to be the optimum.

We first begin by analyzing the compositional differences between the InAs nanowire channels by using EELS [Fig. 4(a)] (Sec. S5 in SM [35]). The In composition x (with respect to Ga) is extracted as a function of position p across the channel as shown in Fig. 4(b) [see inset to Fig. 4(a) for definition of p]. We note that for all samples the outermost layer ($p = 0$) is pure InAs owing to surface segregation [60,65]. However, the composition of the inner layer is significantly different. High-growth temperatures result in highly nonuniform compositions with x decreasing down to $\sim$83% across the channel. The relatively large error bars (up to 3%) are a consequence of composition broadening along the channel as well. On the contrary, when the temperature is as low as 460 °C, the In composition remains above 97% across the entire channel and error bars decrease to $\sim$1% demonstrating high composition homogeneity along the channel.

Based on the values of x extracted with EELS we obtain the lattice mismatch between the InAs channel and the GaAs buffer: $\varepsilon_m = (a_{In_xGa_{1-x}As} - a_{GaAs})/a_{GaAs}$ extrapolating the $In_xGa_{1-x}As$ lattice parameter $a_{In_xGa_{1-x}As}$ assuming Vegard's law [Fig. 4(d)] [66]. ε_m reaches its maximum value of 7.14 ± 0.07% at 460 °C corresponding to the pure InAs material ($x = 1$). To validate our measurements, we extract the lattice mismatch between InAs and the GaAs(Sb) buffer layer using GPA applied on atomic resolution HAADF STEM images. The in-plane ($\varepsilon_{xx'}$) and out-of-plane ($\varepsilon_{yy'}$) lattice deformations are plotted in Fig. 4(d). An identical trend can be seen: $\varepsilon_{xx'}$ and $\varepsilon_{yy'}$ increase with the decrease in growth temperature. Note, that $\varepsilon_{xx'}$ is smaller than $\varepsilon_{yy'}$ suggesting that the InAs layer remains compressively strained in the plane of the interface. The latter causes the expansion of the out-of-plane lattice constant owing to the Poisson effect [67].
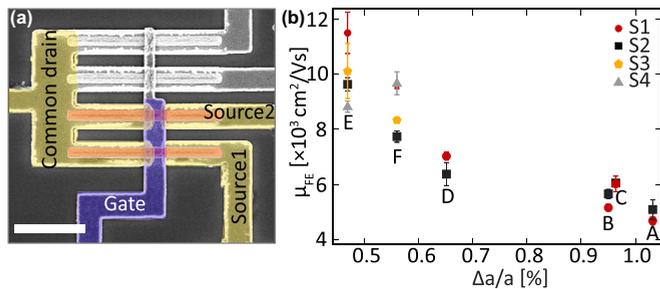
FIG. 5. The role of the InAs/InGaAs interface quality on the electrical properties of InAs/InGaAs/GaAs(Sb) nanowires. (a) False-colored SEM image of field-effect devices (2 μm scale bar). Measured nanowires appear in red, Au/Ti contacts (in yellow), the top Au/Ti gate (in violet). (b) Electron mobility μ_{FE} as a function of the InAs/InGaAs lattice mismatch, $\Delta a/a$, for six samples collected in Table I: A–F. Two nanowires per sample for samples A–D are measured: S1 and S2 both having 500-nm channel length [corresponding to Source 1 and Source 2 in (a)] and four nanowires per sample for samples E and F are measured: S1, S2, S3, S4, all having 500-nm channel length.

We then analyzed the crystal quality of InAs/InGaAs interfaces with GPA. Overall, 1–2 misfit dislocation(s) per nanowire at the InAs/InGaAs interface along the [1$\bar{1}$0] direction are observed, except for the sample grown at 474 °C. It shows a more defective interface with 4 misfit dislocation(s). By decreasing the InAs growth temperature, the Ga content in the channel is reduced increasing the InAs/InGaAs lattice mismatch. However, based on only one cross section per sample it is impossible to draw conclusions whether nanowires from the lowest temperature samples are more defective as compared to the high-temperature samples.

D. Electrical transport properties

Having shown that the In content in the InGaAs buffer and the InAs active region increases by decreasing the growth temperature, we examine if it also affects the electrical properties. Devices are fabricated directly on the growth substrates. Prior to depositing Ti 5 nm/Au 250 nm ohmic contacts, we remove the native oxide from the nanowires by Argon ion milling at 15 W for 150 s. The time of the milling is carefully adjusted to make sure that the InAs is not etched away. We then deposit

10 nm of HfO$_2$ at 90 °C by means of atomic layer deposition to separate the top gate from the contacts. Finally, Ti 5 nm/Au 250 nm top gates are deposited. The patterning of contacts and top gates is done with electron beam lithography. Fabricated devices are then cooled down in a cryogen-free DynaCool physical property measurement system (PPMS) with a base temperature of 1.7 K.

We measure single [1$\bar{1}$0]-oriented InAs/InGaAs/ GaAs(Sb) nanowires [Fig. 5(a)] with 500-nm channel length L and 250–290-nm channel width W, depending on the sample (Table I). The field-effect mobility μ_{FE} is extracted by fitting measured conductance G versus applied top gate voltage V_g as described in Refs. [68,69] (Sec. S6 in the SM [35]). Figure 5(b) shows μ_{FE} as a function of the InAs/InGaAs lattice mismatch, $\Delta a/a$, calculated assuming Vegard's law and using x extracted with XRD for both channel and buffer. For the nanowire samples grown each at a different buffer growth temperature (samples A–E, Table I), μ_{FE} increases from 4700 $\pm$ 100 cm^2 V^{-1} s^{-1} for $\Delta a/a$ = 1.03% (T$_{InGaAs}$ = 540°C, sample A) to 11 500 $\pm$ 700 cm^2 V^{-1} s^{-1} for $\Delta a/a$ = 0.47% (T$_{InGaAs}$ = 520°C, sample E). The carrier concentration n_{2D} ranges from 4.05 to 9.5 $\times 10^{12}$ cm^{-2} as estimated at V_g = 0.

From previous reports considering 15–20-nm wide InAs quantum wells at high carrier densities, it is known that there are primarily two scattering mechanisms affecting the mobility at low temperature: the interface roughness and the alloy disorder [70]. Samples A–E have the same composition of the InAs channel as accessed with EELS and XRD resulting in the same order of alloy disorder in the channel. We therefore attribute the mobility dependence in Fig. 5(b) to an effect of surface roughness and our results suggest that the quality of the InAs/InGaAs interface is significantly improved by growing InGaAs buffer layers at low growth temperatures. Indeed, the lattice mismatch reduces from 1% to 0.47% for the high-temperature and low-temperature sample, respectively. Given that the critical thickness below which dislocations-free interfaces are achieved for 1% lattice mismatch is only ~6 nm, the 15–20-nm InAs layer along the nanowire is expected to be defective for the samples grown with high buffer temperature. On the contrary, for the low buffer temperature sample with 0.47% lattice mismatch the critical thickness is ~18 nm and interfaces without dislocations are expected. The interface improvement directly translates to improvement in the electrical

TABLE I. List of growth parameters and transport data. W, V_{th}, μ, n_{2D}, S_1, and S_2 denote nanowire width, threshold voltage, maximum electron mobility, carrier concentration, outer and inner nanowire, respectively. n is estimated at zero gate voltage V_g=0 via the formula $n_{2D} = C\Delta V/Ae$ [64], where C is the capacitance found with the finite element simulations as described in [5], e is the elementary charge, $A = LW$ is the surface area, and $\Delta V = V_g$-V_{th}. See Sec. S9 in SM [35] for data on two more nanowires from samples E and F.

Sample	T_{InGaAs} °C	T_{InAs} °C	W (nm)		V_{th} V		μ (cm^2 V^{-1} s^{-1})		n_{2D} 10^{12} (cm^{-2})	
			S_1	S_2	S_1	S_2	S_1	S_2	S_1	S_2
A	539	520	270	270	−1.61	−0.84	4859	5541	7.76	4.05
B	535	520	280	290	−1.23	−1.12	5271	5881	5.69	5.02
C	533	520	270	270	−1.09	−1.49	6283	6165	5.23	7.42
D	529	520	250	250	−1.72	−1.11	7095	6360	8.93	5.74
E	520	520	290	290	−2.00	−2.00	12550	9949	8.95	8.95
F	520	474	250	250	−1.83	−1.65	8412	10064	9.48	8.57

properties of the InAs layer in agreement with previously reported results for InAs/AlGaSb heterostructures [71].

An alternative interpretation of the trend observed in Fig. 5(b) could be that a proportion of the conduction takes place in the InGaAs layer, where the reduction of alloy disorder and increased In concentrations at lower temperatures could potentially explain the observed mobility dependence. However, this situation is highly unlikely, since electron transport in InAs occurs in a surface accumulation layer with a depth on the order of 15–20 nm [72,73], less or equal to the InAs channel thickness. To confirm this, we performed simulations of the band structure using a 2D Schrödinger-Poisson model (Sec. S7 in the SM [35], [74]). The FWHM of the wave function is 11 nm at zero gate voltage suggesting that the bulk of conduction is confined to the InAs layer, with only a small part of the wave function tail overlapping into the In-GaAs buffer. To support this conclusion, we measured devices *without* an InAs layer (Sec. S8 in SM [35]). We found that inducing carriers in InGaAs/GaAs(Sb) devices required higher V_g than for InAs/InGaAs/GaAs(Sb) devices, consistent with the notion that at the gate voltages used to calculate mobility in Fig. 5(b) electrons were not occupying the InGaAs. In all, the mobility gains are attributable to reduced InAs/InGaAs interface roughness and reduced InAs dislocation density.

Finally, to check if improvement in the composition purity of the InAs channel affects the mobility, we measure sample F from the InAs sample series ($T_{InAs} = 474°C$) and compare it with sample E ($T_{InAs} = 520°C$). The sample grown at the lowest temperature ($T_{InAs} = 460$ °C) was not chosen for transport measurements because of a high density of parasitic clusters on the oxide mask. These are often merged with nanowires affecting their morphology. Having measured 4 nanowires per sample, we find that μ_{FE} remains in the range 8000–10000 cm^2 V^{-1} s^{-1} [Fig. 5(b)] comparable to the high-temperature sample E. These results support the conclusion that μ_{FE} is mainly limited by the InAs/InGaAs interface quality. Sample F has on average higher In content in the channel than sample E resulting in slightly increased lattice mismatch with the underlying buffer layer. Our data favorably agree with existing literature on InGaAs/GaAs bulk materials [28].

III. CONCLUSIONS

In conclusion, we have successfully optimized InAs/InGaAs SAG nanowires on GaAs(001) substrates doubling their electron mobility. The carrier mobility obtained in this work is higher than state-of-the-art values for SAG of InAs/GaAs and In$_{0.5}$Ga$_{0.5}$As/GaAs nanowires and nanofins [5,14,18,24] demonstrating an advancement toward realizing high-quality gatable InAs quantum channels based on the SAG approach. We improved the nanowire/substrate interface quality by substituting conventional thermal annealing for atomic hydrogen for the native oxide removal and by introducing a metamorphic In$_x$Ga$_{1-x}$As buffer layer between the InAs channel and the GaAs substrate. The Ga-In material intermixing was inhibited by reducing the growth temperature of InGaAs and InAs. We observed that In-rich InGaAs buffer layers grown at reduced temperatures result in improved InAs/InGaAs interfaces owing to the reduced lattice mismatch. The latter is found to be a crucial factor for enhancing the electron mobility of InAs/InGaAs SAG nanowires.

All data needed to evaluate the conclusions in the paper are present in the paper and in the Supplemental Material [35].

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