# Local defect-enhanced anodic oxidation of reformed GaN nanowires

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Understanding formation and distribution of defects in GaN substrates and device layers is needed to improve device performance in rf and power electronics. Here we utilize conductive atomic force microscopy (c-AFM) for studying defect-related leakage paths in an unintentionally doped GaN film formed by nanowire reformation. A nanoscopic Schottky contact is formed between the c-AFM probe and the GaN surface, which, under reverse-bias conditions, reveals local leakage currents at the positions of the nanowires. Cathodoluminescence shows these areas to be dominated by yellow-band luminescence, in contrast to the surrounding GaN matrix, which mainly shows near-band-gap luminescence. These results are attributed to a high density of native and residual defects, confined to the nanowires. In addition, we use anodic oxidation to map defect-related conductive paths through locally induced growth of gallium oxide. The oxide yield, which is known to depend on the local electric field strength between the AFM tip and the sample, correlates well with the level of reverse-bias leakage current. Local irregularities in oxide height reveal extended oxidation attributed to defect-related deep-level states. This is confirmed by controlled dissolution of the oxide in NaOH, showing that a deeper oxide film is grown over areas where defect-related conductive paths are formed. Finally, we demonstrate how this approach can be used as a quick and easy diagnostic tool for evaluating the influence of specific growth conditions and process steps on defect-induced leakage current levels and defect distribution in GaN structures, demonstrating its potential for accelerated test of leakage degradation at critical positions in GaN-based devices.

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## I. INTRODUCTION

GaN combines several distinct semiconductor properties, such as wide band gap, high charge density, high electron mobility, and appreciable temperature tolerance, making it a prominent candidate for next-generation rf and high-power electronics. One major limitation for large-scale implementation of GaN electronics is the current status of GaN material quality. Commercial GaN wafers, with a size of 2 and above, are typically grown by metal-organic vapor phase epitaxy (MOVPE) on foreign substrates (viz. sapphire, silicon carbide, and silicon), making them prone to large amounts of dislocations due to mismatch in crystal lattice constants and thermal coefficients. For this reason, technologies for suppressing dislocations have been investigated, the most well-known approach being epitaxial lateral overgrowth [1–3]. Another potential alternative, still in its infancy, is based on reformation of nanowire (NW) arrays [4]. This method comprises a sequence of epitaxial growth steps: nanowire growth, shell growth, and planarization. It has the potential to significantly reduce the amount of dislocations [4], but possibly at the cost of introducing local areas of an increased density of point defects, due to specific growth conditions.

The influence of defects in GaN can be directly seen and investigated through metal-semiconductor junction Schottky barriers. The effect of dislocations on Schottky barrier height and reverse-bias leakage current [5,6] can be influenced by their surface termination [7,8], and their ability to attract contaminants, especially carbon [9]. Point defects are known to lead to trap-assisted tunneling, resulting in an increased reverse-bias leakage current [6,10–12]. Surface donor states have been shown to reduce the Schottky barrier height [13]. Access to bulk GaN with very low dislocation densities has enabled investigation of leakage currents associated with point defects. An intriguing correlation has been seen between an increased V/III ratio and a decrease of both yellow-band luminescence [14] and carbon impurity levels, as well as an improvement of reverse-bias characteristics and on-resistance [15].

Identification and characterization of point defects is challenging, requiring a set of complementary techniques. Secondary ion mass spectrometry is a well-suited macroscopic tool for determining impurity concentrations and elements [16], and positron annihilation spectroscopy [17] can identify vacancy defects. Defect states in the band gap can be characterized with deep-level transient spectroscopy and capacitance-voltage profiling [18,19], as well as temperature-dependant Schottky measurements [6,13]. Cathodoluminescence (CL) is an excellent tool to reveal the energy level and spatial position of both extrinsic and intrinsic point defects by

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measuring optical properties. Anodic oxidation by conductive atomic force microscopy (c-AFM) has been used previously to identify and modify dislocations [20], but according to our knowledge it has not yet been used for the characterization of point defects.

Anodic oxidation is enabled by the generation of a strong electric field developed between the metallic c-AFM tip and the sample surface. Under ambient conditions, a water bridge forms between the surface and the tip. The electric field accelerates anions from the water bridge towards the sample surface, and, at a certain threshold voltage, electrochemical reactions result in local oxide growth [21,22]. Anodic oxidation thus generally requires a positive sample bias (the sample acting as anode). Field strengths on the order of $10^8$ V cm$^{-1}$ were modeled by Cabrera and Mott [23], who have shown that the role of the electric field is to lower the barrier for transport of ions across an already existing oxide. The oxide height will be a function of the electric field strength, as shown by Avouris *et al.* [24].

Here, the anodic oxidation by c-AFM is used for visualization and passivation of defect-related leakage current paths on a GaN semiconductor surface. A Schottky junction formed at the tip-surface interface allows trap-assisted tunneling to be locally revealed by the reverse-bias leakage current and onset of anodic oxidation. AFM-induced oxide films are self-selectively growing only on areas which show local leakage current in the reverse-biased Schottky barrier configuration, which can be correlated with electrically active dislocations and point defects. The dependence of the oxide film thickness on applied bias as well as trap-assisted tunneling is explored. The anodic oxidation process highlights local variations in oxide formation, which we relate to deep-level traps, as confirmed by subsequent oxide removal through etching in NaOH solution. We suggest applying anodic oxidation by c-AFM as a comparatively fast and easy diagnostic tool for investigating hidden electrically active defects in GaN.

The investigated GaN surfaces, obtained by reformation of NW arrays, comprise a pattern of different areas, originating from different epitaxial growth steps, where both the NW growth and the reformation utilize conditions that are radically different from conventional growth by MOVPE. As such, they enable a very efficient suppression of dislocations [4], but they also provide conditions for incorporation of significantly different levels of point defects. Therefore a tool for fast characterization and improved understanding of point defects and their local distribution in the reformed GaN surfaces, as demonstrated here, is an essential step towards the development of affordable high-quality GaN substrates.

## II. EXPERIMENTAL DETAILS

The experiments were performed in a Schottky barrier configuration formed by the metal AFM tip and the semiconducting GaN surface, see Fig. 1(a). All measurements were carried out at +10 V sample bias at room temperature and ambient humidity of 30%−40%, unless otherwise stated. A good electrical back contact with the substrate and the GaN buffer layer is assured by the addition of silver paste to the bottom and the sides of the sample. For surface characterization and local oxide formation, a JPK Nanowizard II AFM, operated in

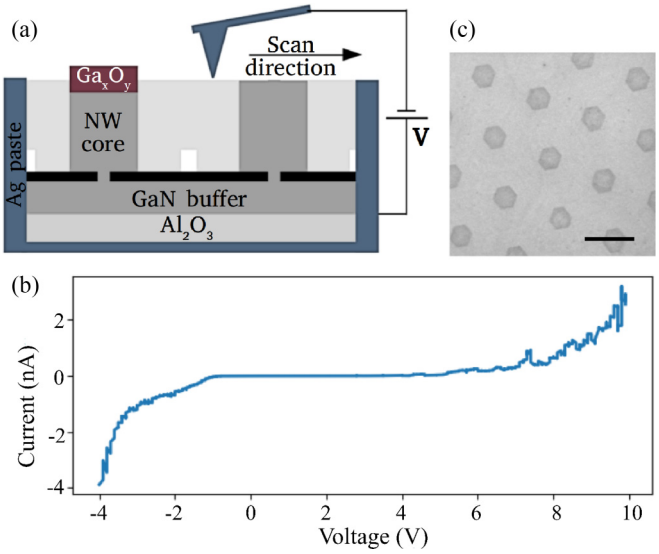


FIG. 1. (a) Schematics of the measurement setup and (b) typical *I-V* curve acquired over a GaN nanowire core. Note that the bias is applied to the sample. (c) SEM top-view image of the coalesced GaN.

contact mode, and a Bruker Dimension Icon AFM, operated in Peak Force Tapping™mode, were used. Conductive modules were utilized in order to induce surface oxide growth and measure local electrical properties. The Nanowizard instrument was operated with the feedback loop maintaining a constant cantilever deflection using Pt-coated cantilevers (PtSi-CONT from Nanosensors) with nominal force constant of 0.2 Nm$^{-1}$ and resonance frequency of 13 kHz. The local current was measured with a low current amplifier with a gain of $10^8$ VA$^{-1}$ and a noise limit of 0.5 pA rms. For the Dimension Icon AFM, the PF-TUNA module was used, providing high sensitivity and being capable of detecting currents in the sub-pA range, together with PtIr-coated cantilevers (SCM-PIT-V2 from Bruker) with nominal force constant of 2.8 Nm$^{-1}$ and resonance frequency of 75 kHz. Although the Peak Force Tapping mode was implemented, where the tip is oscillated between attractive and repulsive force regimes with a maximum repulsive peak force controlled by the feedback loop, we only show the contact current channel recorded during the tip-surface contact period of the repulsive regime. In addition to current mapping, individual current-voltage (*I-V*) curves were obtained at specific positions on the sample, as shown in Fig. 1(b). Note that the bias is applied to the sample, meaning that negative voltage corresponds to a forward-biased Schottky barrier and vice versa. Cathodoluminescence measurements were performed in a conventional scanning electron microscope (SEM, Zeiss MA 15) at room temperature. Monochromatic and hyperspectral images were recorded in top view using a Delmic Sparc setup. The data presented here is from hyperspectral maps, which were recorded using an acceleration voltage of 5 kV and a probe current of 50 pA.

The reformed GaN samples were coalesced by recrystallization of a periodic array of GaN NWs which were grown by MOVPE on a commercial *n*-type GaN buffer layer grown on a sapphire substrate. The growth mask for the NW growth consists of a 70-nm-thick $Si_3N_4$ layer deposited on the GaN

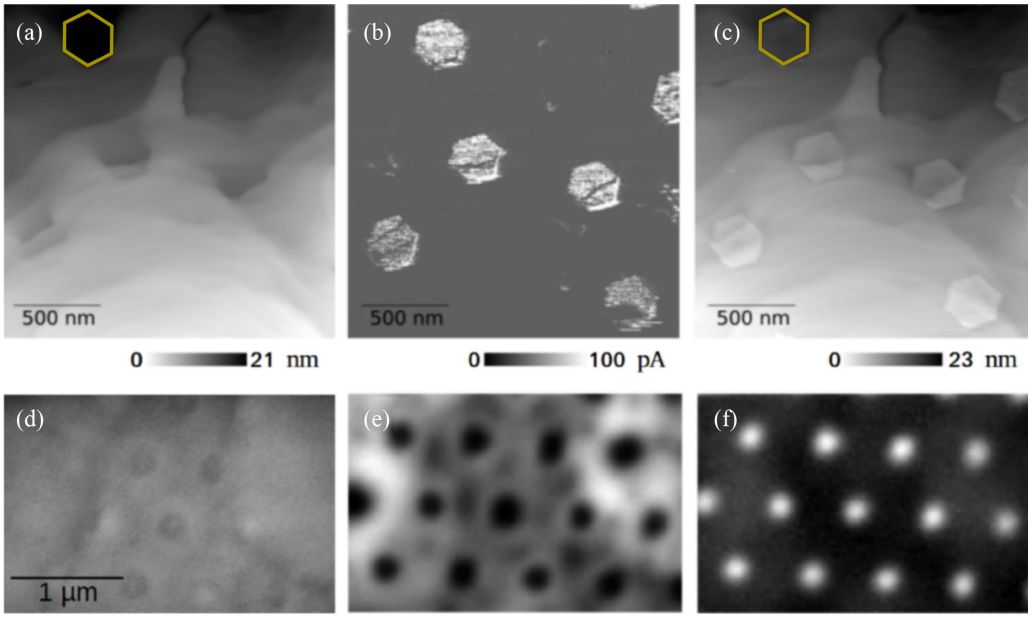


FIG. 2. (a)–(c) c-AFM and (d)–(f) CL images of the coalesced GaN NW sample. (a) AFM topography image before anodic oxidation. Simultaneously acquired (b) current map and (c) topography image of the same area during local anodic oxidation at 10-V sample bias and 30% relative humidity using the JPK AFM in contact mode. The oxide formed on the hexagonal cores (c) increases their height, revealing their position and shape much clearer than in (a). (d) SEM image together with hyperspectral CL maps showing (e) near-band-gap emission using an energy window of 150 meV centered at 3.4 eV and (f) yellow-band emission, from the same position, in an energy window of 500 meV centered at 2.2 eV.

buffer layer. The mask pattern was fabricated by nanoimprint lithography and reactive ion etching and comprises a hexagonal array of 160 nm wide openings spaced 700 nm apart. After cleaning, the sample was loaded into the MOVPE reactor and baked at around 400 °C, followed by an anneal step to ensure removal of the native oxide in the openings. The nanowire nucleation was initiated at an elevated temperature of 1010 °C, using triethylgallium and ammonia as precursors with a low V/III ratio of 7:1, and nanowires were grown at a sample temperature of 980 °C, resulting in the growth of NW cores with about 250 nm width, facet to facet. This was followed by radial growth on the NWs at 880 °C and a V/III ratio of 7000:1. Finally, these core-shell NW structures were coalesced by a passive reformation step at 980 °C with the Ga precursor turned off, resulting in a planar GaN film. In the scanning electron microscopy (SEM) image of Fig. 1(c) the areas corresponding to the NW core, shell, and the reformed surface are visible. A second sample was grown at appreciably higher preanneal and NW nucleation temperature (1054 °C instead of 1010 °C). Other growth conditions were kept constant between samples. More details of sample growth and morphology are found elsewhere [4].

## III. RESULTS AND DISCUSSION

Figure 2 shows the reformed GaN sample characterized by c-AFM and CL. A hexagonal pattern, corresponding to the NW cores, can be seen in the AFM topography image of Fig. 2(a). Some NW cores are less apparent due to a redistribution of GaN material over the NWs during reformation. A current map, Fig. 2(b), shows reverse-bias leakage current of the same area, acquired after the initial scan at +10 V sample bias. Conductivity is mostly restricted to the NW cores, showing current levels of ∼100 pA. Some additional conductive points at current levels of 10–60 pA are observed at the interfaces between coalesced NWs. The average CL emission from the coalesced layers shows two features, a peak at 3.4 eV corresponding to near-band-gap emission (NBE) from GaN and a broader band centered at 2.2 eV, referred to as the yellow-band (YB), generally associated with point defects. Figure 2(d) shows an SEM image of a random area of the sample. Some of the cores appear dark surrounded by bright rings. Figures 2(e) and 2(f) show monochromatic images of the same area, extracted from a hyperspectral image. Images highlighting the NBE, like the one in Fig. 2(e) centered at 3.4 eV, show the same pattern over the entire sample of dark spots corresponding to the position of the cores and a bright ring corresponding to the shell. The coalesced areas between the shells show reduced emission intensity and a pattern of dark spots and lines, corresponding to defects, probably dislocations. When the energy window is centered at 2.2 eV, as in Fig. 2(f), the contrast is reversed, where the cores appear bright. The fact that no NBE is observed from the cores, which however show strong YB emission, indicates the presence of point defects in the NW cores.

In a previous investigation [4] we reported on properties and localization of dislocations in similarly coalesced planar GaN. We found conductive dislocations at the interfaces between coalesced NWs, which coincides with the position of small bright points in Fig. 2(b) showing current values in the 10–60 pA range and the position of reduced NBE in Fig. 2(e). The only other position where dislocations were observed was in the center of few NW cores, as also confirmed

by transmission electron microscopy. However, those were nonconductive edge dislocations. In the same work, scanning capacitance microscopy was used to identify the NW cores to be *n* type, while the NW shells showed weak *p*-type behavior. We want to point out especially that no dislocations were found at the interface between the NW cores and shells.

Here the focus is placed on the NW cores, which show appreciable leakage current levels (∼100 pA). The interface between the unintentionally doped *n*-type core and unintentionally doped *p*-type shell often shows higher current. It has been reported that a potential barrier may form at this interface [25]. It is also possible that unintentional impurity incorporation along this interface creates parasitic conductive channels, contributing to a higher leakage current. By combining our current results with our previous measurements, we find that although the NW cores potentially provide dislocation-free templates for planar GaN, their growth conditions may strongly encourage incorporation of point defects, leading to unintentional *n*-doping, defect-related yellow-band luminescence, and trap-assisted leakage. This is not too surprising, since the selective formation of GaN NWs requires off-equilibrium conditions in order to achieve highly anisotropic growth, enhancing the influence of parameters such as surface diffusion and surface reconstruction. Plausible impurity sources related to the selective NW growth process include carbon from the alkyl Ga source triethylgallium and Si from etch damage of the $Si_3N_4$ mask.

Several point defects have been reported to act as shallow donors and result in background electron concentration in unintentionally doped GaN. The most common donor impurities in general are silicon at Ga sites ($Si_{Ga}$), oxygen at N sites ($O_N$), and carbon at Ga sites ($C_{Ga}$). However, the Ga-rich conditions applied here during NW core growth energetically favor the incorporation of carbon at N sites ($C_N$), and $C_N$ acts as a very deep acceptor [26]. Furthermore, $C_N$ point defects have been identified before, together with $C_NO_N$ complexes, to be the origin of a 2.2 eV peak in the broad YB emission [27], which corresponds to the luminescence observed here from the NW cores. Ga vacancies ($V_{Ga}$), which also are known to be a deep-level acceptor [28], are further attributed to the YB emission [29]. According to literature and our specific growth conditions, we tentatively correlate the increased current levels of the NW cores together with the increased YB luminescence to $C_N$ impurities. $Si_{Ga}$ or $O_N$ impurities, acting as shallow donors, might further contribute to the increased conductivity and explain the intrinsically *n*-type behavior of the NW cores.

We now focus on anodic oxidation and how this process can further visualize local defects. An AFM topography image was acquired simultaneously with the current map, i.e., with applied sample bias of 10 V, shown in Fig. 2(c). Compared with the topography image shown in Fig. 2(a), the NW cores are more pronounced due to a 4–6 nm height increase. This has to be interpreted as the result of anodic oxidation of the GaN surface forming gallium oxide ($Ga_xO_y$) exclusively at those areas where current was measured, see Fig. 2(b). We note that the oxide is 1 nm higher at the core/shell interface where a higher current was previously observed. The surface roughness of the $Ga_xO_y$ is about 0.8 nm rms, an increase from 0.2 nm rms before oxidation, measured over the area of a NW core with a homogeneous oxide layer, as indicated in Fig. 2(c). Note, though, that features with larger surface corrugation, such as step bunching, as seen on the original NW *c* planes, are retained after oxidation. The tip loading force required to induce oxidation is 30 nN, much lower than reported previously [30]. Furthermore, the anodic oxide suppresses conductivity at bias voltages equal to or lower than the one used for oxidation: *I*-*V* spectra taken at the NW core after local anodic oxidation show a higher onset voltage at forward bias, as compared to Fig. 1(b), and no current at reverse bias up to 10 V. This is in agreement with a previous report regarding anodic oxidation of dislocations [20], while in our study local anodic oxidation is enabled by point-defect-assisted leakage current.

In order to investigate the leakage current variation throughout a NW core and better understand its influence on oxide formation, a series of topography measurements at increasing bias voltages was performed. A small area, including a single NW core, was chosen, which was imaged subsequently at sample bias voltages increasing from 0 to 10 V, as shown by the AFM images in Fig. 3. Height profiles across the edge of the NW core, taken from the topography images with increasing bias, are overlaid in Fig. 3, demonstrating how the thickness of the anodic oxide over the NW core evolves. A measurable onset of oxide formation, as well as current detection, occurred at a threshold bias of 6 V at 30% relative humidity, resulting in an approximately 0.5 nm high anodic oxide on top of the NW core. The oxide layer continues to grow with increasing bias, reaching a height of around 5 nm at 10 V over the NW core. The increasing thickness of the oxide film results in a decrease of the electric field strength over the tip/surface interface. We expect that this will finally lead to an electric field that is insufficient to overcome the threshold voltage of the oxidation process and thus to a saturation of the oxide thickness. We further observe that the oxide growth is enhanced at the core/shell interface, here reaching a height of around 6 nm at 10 V. It has been reported that a potential barrier may form at this interface [25]. It is also possible that unintentional impurity incorporation along this interface creates parasitic conductive channels, contributing to a higher leakage current and thereby anodic oxidation. Moreover, we note the fast growth of a local $Ga_xO_y$ hill at the lower corner of the NW core, which will be discussed later.

We propose that during oxide growth, the Ga atoms from the GaN material are used to form $Ga_xO_y$ while the N atoms are released into the gas phase. The current-dependent variation in $Ga_xO_y$ height should thus accordingly correspond to a variation in consumption of GaN. In order to verify this expected behavior, we removed the oxide by NaOH wet etch using a 2 M solution at 70 °C in darkness for 30 min. The results are presented in Fig. 4, showing AFM topography images of the same area (a) prior to surface modification, (b) after anodic oxidation, and (c) after etching. It can be seen that the surface of the GaN NW cores after etching is lowered by 2–3 nm, corresponding to those areas of the surface that had been oxidized, while the unoxidized material is stable against NaOH etching, as individual surface steps along the coalesced regions are preserved. The surface roughness at the NW cores remains unchanged upon oxide removal at around 0.8 nm rms.

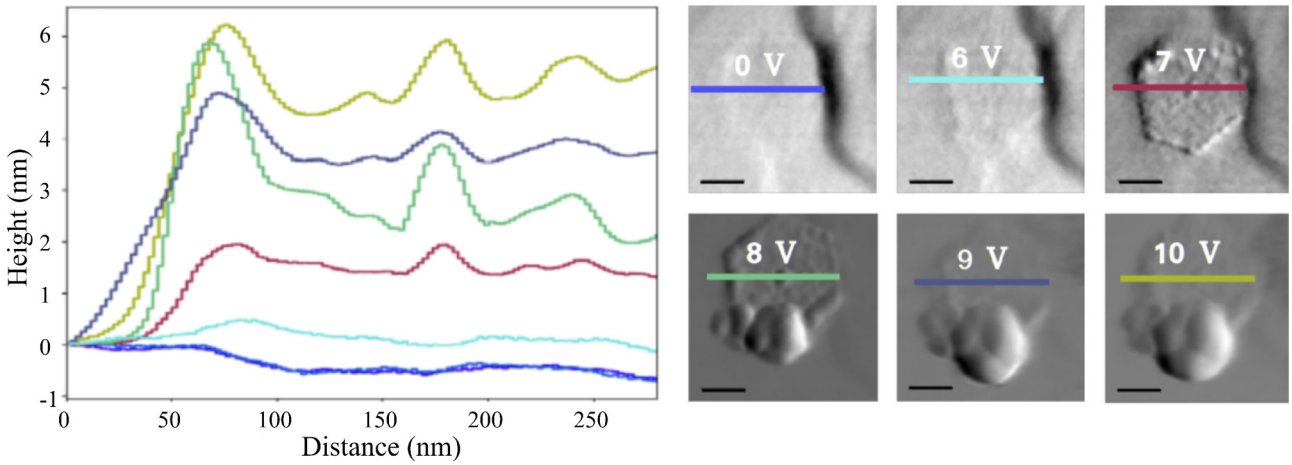


FIG. 3. Series of successive topography measurements at different sample bias, recorded with the JPK AFM in contact mode at 30% relative humidity. Height profiles are overlaid, taken at the same position from images obtained at increasing sample bias, as indicated in the AFM images (derivative of height) to the right. The scale bar corresponds to 100 nm. Before oxidation, the surface of the imaged NW core is 0.5 nm below that of the surrounding shell. Anodic oxidation starts at a threshold bias of 5 V, with increasing oxide thickness for increasing bias.

Furthermore, small cavities can be found locally in those areas where etching resulted in the removal of material [Fig. 4(c)], representing irregularities in oxide thickness underneath the original surface. Irregularities in oxide thickness had also been found above the surface, such as the previously noted fast-growing $Ga_xO_y$ hill at the lower corner of the NW core in Fig. 3 and the locally inhomogeneous oxide thickness on some NW cores seen in Fig. 4(b). We therefore interpret the cavities as counterparts of those small structure with increased oxide height. Such locally increased oxide thickness has to be related to local incidents of higher conductivity in the semiconductor, as a higher fraction of the applied bias voltage will drop across the tip/sample junction, enabling the growth of a thicker oxide. We attribute this to the onset of trap-assisted tunneling through deep-level states, which would not only explain the increased conductivity but also its localized nature. Indeed, the presence of deep-level impurities throughout the NW cores was already indicated by the YB emission. The local distribution of these defects can be obtained from the sample conductivity, showing moderate levels over the entire NW core with locally enhanced values due to local high defect densities. This local distribution is revealed by the anodic oxide through the formation of cavities upon etching but also through the irregularities in the oxide above the surface. Accordingly, it has to be noted that NaOH etching is not even needed, but a thorough investigation of the oxidized surface is sufficient to indicate the location of the underlying, hidden defects.

Finally, we present an example where we use the anodic oxidation as a diagnostic tool to investigate the influence of NW growth conditions. A second sample was grown at appreciably higher preanneal and NW nucleation temperature in order to reduce impurity incorporation in the base of the NWs. Figure 5 shows simultaneously acquired (a) topography and (b) current map images of this sample with 10 V bias voltage. The nanowire cores exhibit significantly reduced current levels as compared to the previous sample, Fig. 2(c). In general, no measurable levels of current or oxide are seen in the NW core center. At the core/shell interface, typically very low currents (1–2 pA) are measured, as seen in Fig. 5(b), with no discernible oxide formation [see Fig. 5(a)]. We have also found groups of NWs with interface currents of 5–20 pA and a very limited oxide growth of a few nanometers height, as shown in the insets in Fig. 5. The elimination of reverse-bias

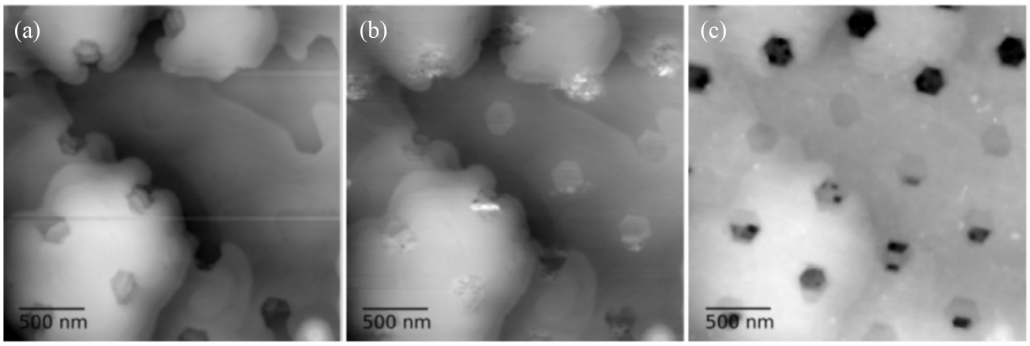


FIG. 4. AFM topography depicting the same area (a) prior to surface modification, (b) after oxidation, and (c) following NaOH etching treatment, recorded with the JPK AFM in contact mode. The grayscale corresponds to a height range of 30 nm (a), 34 nm (b), and 66 nm (c).

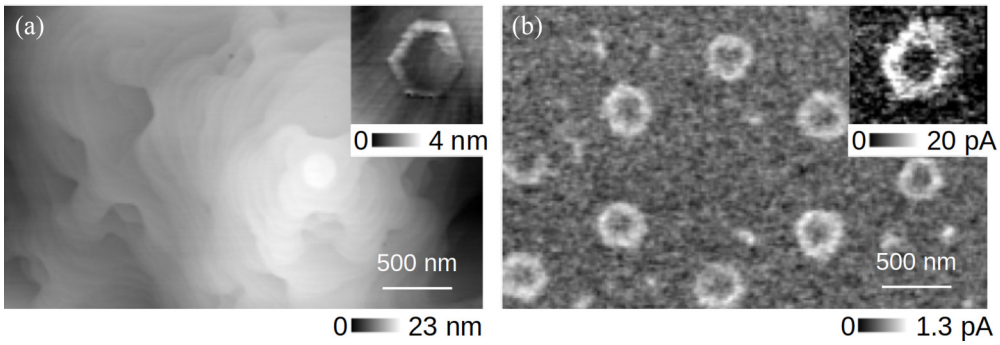


FIG. 5. AFM topography image (a) and current map (b) of a coalesced GaN NW sample nucleated at 1145 °C, acquired with the Bruker AFM in PeakForce mode at 40% relative humidity and 10-V sample bias. Note the much smaller current values as compared to Fig. 2. The insets show one of a few examples of a NW core with slightly higher current values of 20 pA at the core/shell interface (b) leading to the local formation of a thin oxide (a).

leakage current within the NW cores, as compared to typically 100 pA in the previous sample, was accompanied by higher onset voltage at forward bias, indicating an increased series resistance in the AFM tip/sample circuit. The location of the added resistance in the circuit was pinpointed by control measurements of the electrically active dislocations of the coalesced interface, which showed a corresponding decrease in reverse leakage current, from about 10–60 pA in the first sample to below 0.5 pA at 10 V in the second sample, due to an added series resistance.

In perspective, the trap-assisted leakage current and anodic oxidation are essentially diminished on the NW core surface but not eliminated. They still occur occasionally at NW core/shell interfaces, although with appreciably lower current levels and oxidation rate. We interpret these results to show that trap-assisted tunneling is still viable at the NW cores, but the tip/surface junction threshold voltage for onset of anodic oxidation is rarely met due to an added series resistance resulting from a preanneal and nucleation at increased temperature.

Interestingly, with the trap-assisted tunneling mechanism still prevalent, we have no clear indication of decreased carbon incorporation. The CL spectra of the samples, see Fig. S1 of the Supplemental Material in Ref. [31] and Fig. 2(f), both show the carbon-related 2.2 eV YB peak, while an appreciable decrease in NW conductivity was found. The low current levels observed in the second sample therefore may not be related to a change in carbon incorporation but rather a decrease in residual silicon, due to the high initial growth temperature and henceforth reduced unintentional doping.

## IV. CONCLUSIONS

In conclusion, anodic oxidation enabled by c-AFM was used as a surface diagnostic tool for visualization and analysis of defect-assisted local leakage current in a GaN surface, formed by growth and reformation of GaN NW arrays. YB luminescence, measured by CL, shows a 2.2 eV peak, most commonly attributed to deep-level $C_N$ impurities, which here are assumed to be the origin of reverse leakage current by localized trap-assisted tunneling. There were no signs of reduction of carbon incorporation by increased temperature at preanneal NW nucleation, although *n*-type conductivity of the NW fell sharply. The anodic oxide effectively suppresses reverse-bias leakage currents below sub-pA level, at the supplied bias. The topography of gallium oxide has been confirmed to be correlated to reverse current levels with discernible local conductive paths. The specific and immediate feedback that the method provides was illustrated by a comparison between samples with different anneal and NW nucleation temperature. The simplicity of this approach, only requiring a c-AFM operating at ambient conditions, without extensive sample preparation or processing, offers a comparably straightforward method for local visualization and analysis of impurity-related leakage paths inside epitaxial layers, heterostructures, and critical positions in devices, potentially simplifying reliability and stress test analysis.

## ACKNOWLEDGMENTS

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[31] See Supplemental Material at http://link.aps.org/supplemental/10.1103/PhysRevMaterials.4.074603 for CL spectrum of the sample with low nucleation temperature highlighting the 2.2-eV peak.