Editors' Suggestion

Two-dimensional defect mapping of the $SiO_2/4H$-SiC interface

Judith Woerle,[1,2,*] Brett C. Johnson,[3] Corrado Bongiorno,[4] Kohei Yamasue,[5] Gabriel Ferro,[6] Dipanwita Dutta,[1] Thomas A. Jung,[1] Hans Sigg,[1] Yasuo Cho,[5] Ulrike Grossner,[2] and Massimo Camarda[1,2]

[1]*Paul Scherrer Institute, Forschungsstrasse 111, 5232 Villigen, Switzerland*

[2]*Advanced Power Semiconductor Laboratory, ETH Zurich, Physikstrasse 3, 8092 Zurich, Switzerland*

[3]*Centre for Quantum Computing and Communication Technology, School of Physics, University of Melbourne, Victoria 3010, Australia*

[4]*Consiglio Nazionale delle Ricerche–Istituto per la Microelettronica e Microsistemi (CNR-IMM), Strada VIII 5, Zona Industriale, 95121 Catania, Italy*

[5]*Research Institute of Electrical Communication, Tohoku University, 2-1-1 Katahira, Aoba, Sendai 980-8577, Japan*

[6]*Laboratoire des Multimatériaux et Interfaces (UMR 5615), Université de Lyon, Université Claude Bernard Lyon 1, CNRS, 43 boulevard du 11 Novembre 1918, 69622 Villeurbanne, France*

(Received 22 March 2019; revised manuscript received 14 June 2019; published 15 August 2019)

Current generations of 4*H*-SiC metal-oxide-semiconductor field-effect transistors are still challenged by the high number of defects at the SiO_2/SiC interface that limit both the performance and gate reliability of these devices. One potential source of the high density of interface defect states (D_{it}) is the stepped morphology on commonly used off-axially grown epitaxial surfaces, favoring incomplete oxidation and the formation of defective transition layers. Here we report measurements on intentionally modified 4*H*-SiC surfaces exhibiting both atomically flat and stepped regions where the generation of interface defects can be directly linked to differences in surface roughness. By combining spatially resolving structural, chemical, optical, and electrical analysis techniques, a strong increase of D_{it} for stepped surfaces was revealed while regions with an atomically flat SiC surface exhibited close-to-ideal interface properties.

DOI: 10.1103/PhysRevMaterials.3.084602

I. INTRODUCTION

Silicon carbide (SiC), with its beneficial electrical and thermal properties such as a wide band gap, high breakdown field, high electron saturation velocity, and high thermal conductivity, is a very attractive material for a wide range of high-power, high-voltage, and high-temperature applications. Recently, SiC has also proved to be a promising quantum technology platform and the first successful demonstrations of it as a solid-state host material for single-photon sources or quantum sensors have been reported [1–4].

Most of these applications require substrates with homoepitaxial layers with a well-defined doping profile and thickness to act as an active layer. In order to maintain the polytype of the substrate during epitaxial growth, substrates are cut a few degrees off-axis from the (0001) basal plane (most common today are off-angles of 4° toward the [11$\bar{2}$0] direction), promoting a lateral epitaxial growth at the surface steps [5,6].

While this step-controlled growth results in electronic-grade single-polytype epilayers, it also leads to the creation of atomic steps on the surface, commonly referred to as microsteps [7], together with the formation of so-called isolated macrosteps, consisting of bunched microsteps of several nanometers in height [8].

Since the thermal oxidation process is strongly orientation-dependent, the described surface morphology of 4*H*-SiC is expected to significantly influence the formation of the SiO_2/SiC interface. Apart from variations in the oxide growth rate for different surface facets [9,10], a stepped surface may lead to an increased number of interface defects as incomplete crystal planes may favor nonideal oxidation with a larger number of dangling bonds and the formation of a nonstoichiometric near-interface region [11,12]. This will not only affect surface regions with a large number of isolated macrosteps, but could also explain the high density of interface defect states (D_{it}) for all epitaxies grown under a small off-angle which exhibit a continuous microstep pattern. The question of whether macrosteps lead to performance limitations of metal-oxide-semiconductor field-effect transistors (MOSFETs) due to electric field crowding and higher surface roughness in particular has been addressed previously but experimental results are not conclusive [13–15]. While Liu *et al.* reported that neither the channel mobility nor the density of interface defects depended on the presence or absence of macrosteps, Frazzetto *et al.* observed an improvement of channel mobility and D_{it} for samples with large macrosteps formed during postimplantation annealing without a protective carbon cap. Cabello *et al.* showed that the impact of surface roughness scattering—the deflection of electrons by structural defects—only starts to play a role for devices where the Coulomb scattering due to interface defects in the channel region is low enough and the quality of the interface is sufficiently high.

One reason for this wide spread of experimental results may be related to the fact that all these studies use electrical analysis methods such as capacitance-voltage (CV) or conductance measurements which require large probing pads and

*woerle@aps.ee.ethz.ch

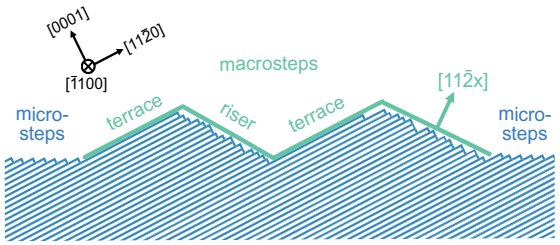

FIG. 1. Schematic of an off-axis surface showing both micro- and macrosteps as observed on commercial 4*H*-C epitaxial surfaces. The subnanofacets at the riser exhibit different orientations commonly described with a Miller index of (11$\bar{2}x$). The terrace along the (0001) basal plane is atomically flat with only some sparsely distributed single steps as indicated on the terrace on the right. Note that the off-axis angle (the most common of these are 4°) is exaggerated in this sketch.

result in an averaged signal over a large number of micro- or macrosteps. Hence, local variations in surface roughness cannot be addressed with these techniques. In order to separate the contributions from different morphological features to the formation of defects at the SiO_2/SiC interface, spatially resolving analysis techniques are required. Apart from their small dimensions, isolated macrosteps present an ideal system to explore the SiO_2/SiC interface formed on SiC surfaces with varying surface roughnesses as they are composed of two different types of facets: atomically flat terraces [parallel to the (0001) plane] and stepped risers [parallel to a (11$\bar{2}x$) plane with $x = 25$–30] [16–18]. A schematic plot of the faceted morphology of an off-axis surface is depicted in Fig. 1.

In order increase the size and density of the macrosteps and thus allow for the analysis of individual macrostep facets, a high-temperature process can be employed, leading to a surface reconstruction with an amplification of the macrosteps. Here we use a so-called Si-melt process where the SiC surface is capped with a Si piece during the high-temperature annealing [19,20]. While a noncapped annealing step often leads to a carbon-rich surface, chemical analysis of Si-capped samples confirmed a Si-rich surface reconstruction [21]. Using this approach, macrosteps with heights of up to 200 nm and terrace widths of several micrometers have been reported [20], an order of magnitude larger than what is commonly observed for surface reconstruction processes without any capping [22,23].

In this study, a variety of spatially resolved analysis techniques are combined to form a comprehensive picture of the morphology-dependent defect distribution at the SiO_2/SiC interface. For this purpose, the previously described Si-melt process is performed prior to oxidation and the targeted, strongly macrostepped surface with both atomically flat and stepped facets is monitored by atomic-force microscopy (AFM). After the thermal oxidation process, scanning transmission electron microscopy (STEM) and electron energy loss spectroscopy (EELS) provide structural and chemical information on the transition region between the SiC bulk and the SiO_2 layer on top. Finally, photoluminescence (PL) confocal microscopy and local deep-level transient spectroscopy (local-DLTS) are used to investigate the optical and electronic properties of interface defects in a spatially resolved manner.

II. EXPERIMENTAL DETAILS

A. Sample preparation

For this study, 10 mm × 10 mm samples of a Wolfspeed (0001) 4*H*-C wafer with a 4° off-axis orientation towards the ⟨11$\bar{2}$0⟩ direction were used. The 15 μm thick *n*-type epitaxial layers had a nitrogen doping concentration of $N_d = 4 \times 10^{15}$ cm^{-3}. The samples exhibited a few isolated macrosteps nonuniformly distributed along the [11$\bar{2}$0] direction with step heights between 2 and 8 nm [10].

A strong and continuous macrostep formation was obtained by a Si-melt process where a piece of Si was melted on top of the 4*H*-C wafer [20]. After this process, the solidified silicon was removed by etching the samples for several hours in a solution of $HF + HNO_3$. Subsequently, samples with and without the described Si-melt process were thoroughly cleaned and then thermally oxidized at 1050°C for up to 24h in an O_2 ambient, resulting in SiO_2 layers with thicknesses up to 30 nm. No further postoxidation annealing steps were applied.

TEM samples of the SiO_2/SiC interface were prepared by capping the oxide with a 500 nm thick Al layer before milling the lamellas with a focused-ion beam first at 30 keV and 98 pA and finally at 5 keV and 47 pA [24]. Subsequently, the samples were cleaned and thinned further to around 80 nm using the Fischione 1040 Nanomill TEM specimen preparation system. The orientation of the lamellas was chosen to be orthogonal to the surface steps.

For the local-DLTS measurements, a 100 nm thick Ni layer was deposited on the back of the sample to provide good Ohmic contact. For electrical analysis via capacitance-voltage measurements (see the Supplemental Material [46]), circular Al contacts ($r = 300$ μm) were deposited on top of the SiO_2 and Ni was used for the Ohmic backside contact.

B. Sample characterization

AFM analysis was conducted with either a Bruker MultiMode 8 AFM or a Bruker Dimension 3100 AFM in tapping mode with a tapping frequency of 150 kHz. The probe tips had radii down to 2 nm to enhance the lateral resolution. All AFM maps shown here were performed prior to thermal oxidation.

The STEM analysis was performed with a JEOL ARM200CF using an accelerating voltage of 60 keV and a spot size of 0.13 nm. EELS spectra were collected with a Gatan quantum spectrometer equipped with dual EELS acquisition and fast shutter capabilities. Pixel sizes spanned from 0.1 nm to 0.05 nm and the energy dispersion was fixed at 0.25 eV/pixel in order to have the silicon, carbon, and oxygen signals in the same spectrum.

For optical characterization, a custom-built confocal microscope was used. It was equipped with a 532 nm continuous wave laser, a dichroic mirror, a high-NA (0.95) 100× air objective, a 560 nm long pass filter, and a fiber-coupled single-photon counting module [see also Fig. 4(a)]. The theoretical diffraction-limited spatial resolution was 280 nm for emission wavelengths of 600 nm. The samples were mounted onto a piezoelectric *XYZ* scanning stage allowing for 100 μm × 100 μm scans. All confocal images presented here were collected at room temperature. For the ensemble PL

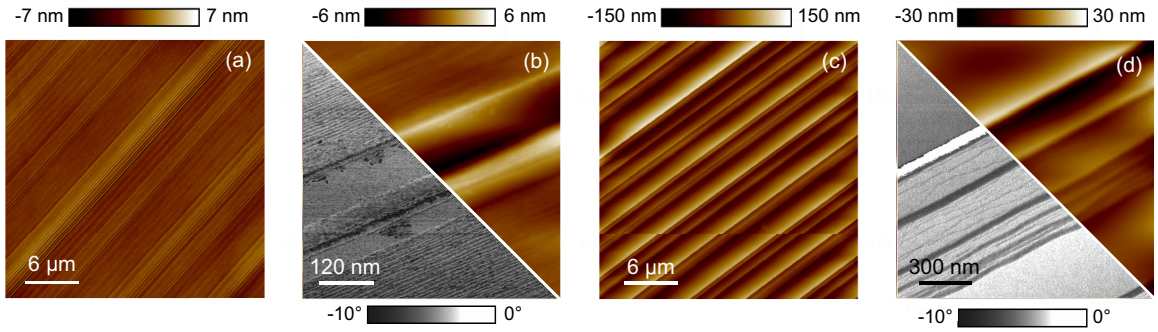

FIG. 2. (a) AFM images of an unprocessed (0001) 4*H*-C epitaxial surface showing a random distribution of isolated macrosteps. (b) Isolated macrostep consisting of a double-peak with atomically flat terraces and a faceted riser in between. The phase image (bottom left) also shows the microstepping of the surface away from the macrostep. (c) Surface morphology after the Si-melt process and subsequent Si removal. (d) A zoom-in view of a macrostep in (c) showing two wide terraces separated by a riser facet composed of several smaller steps. The white stripe in the phase map is a measurement artifact. Note that the scan sizes of (b) and (d) are different.

measurements, a micro-Raman Renishaw InVia spectrometer equipped with a 532 nm laser with 1mW power was used. The exposure time for all PL spectra was 50 s.

Local-DLTS measurements were performed using a commercial contact-mode AFM (Bruker Icon) with a home-built scanning nonlinear dielectric microscopy (SNDM) probe oscillating at a frequency of 1 GHz [see Fig. 6(a)] [25,26]. The radius of the Pt-coated probing tip forming a capacitor with the SiO_2/SiC stack was 150 nm and the scan size was 1 μm × 1 μm. For the measurements, voltage pulses with amplitudes between 0 and −5V and with a pulse width of $t_{pw} = 0.5\,\mu$s were applied to the samples. The repetition frequency of the pulses was 10 kHz. Assuming a capture cross section of the interface traps of $\sigma_S = 4 \times 10^{-16}\,cm^2$ (obtained from standard-DLTS measurements), an energy depth of 0.38 eV below the conduction band was probed.

III. RESULTS

A. AFM analysis

Before thermal oxidation, the surface topography of the unannealed and annealed samples were studied by height and phase AFM. While height maps image the surface topography, phase maps are error images showing the phase difference between the oscillating cantilever and the drive signal. Although a quantitative interpretation of the phase maps is difficult, they often reveal additional properties of the sample material itself.

Figure 2 shows typical macrostep distributions for samples before and after the Si capping and high-temperature anneal. As-grown Si-face 4*H*-C epitaxial layers exhibit isolated macrosteps with heights of several nanometers which are nonuniformly distributed across the surface [10,27,28], as depicted in Fig. 2(a). Figure 2(b) shows a high-resolution height (top right) and phase (bottom left) image of such an isolated macrostep with its typical double-hill-valley structure composed of two types of facets: atomically flat terraces parallel to the (0001) plane and bunched risers parallel to a $(11\bar{2}x)$ plane. The phase image also resolves the continuously microstepped surface of standard epitaxial layers with step heights of 2 to 4 bilayers (2.5–5 Å).

The macrosteps of the Si-melted sample in Fig. 2(c) on the other hand have heights of up to a few hundred nanometers and terrace widths in the micrometer range. Similarly to the isolated macrosteps on the untreated surface, they are composed of two types of facets: step-free terraces and step-bunched risers, as depicted in Fig. 2(d). Here, the risers are composed of an accumulation of steps, each of them several nanometers high and exhibiting again a subnanometer faceting. Additional 1D line scans of macrosteps as shown in Figs. 2(b) and 2(d) are included in the Supplemental Material [46].

For all further analysis presented in the subsequent sections, three different types of surface morphologies are distinguished: surfaces with a continuous nanofaceting (microsteps) as observed on common, unmodified SiC epitaxial surfaces as well as atomically flat terraces and strongly bunched risers of macrostepped epitaxial surfaces after the Si-melt process.

B. STEM/EELS analysis

In EELS, a thin SiO_2/SiC cross-section specimen is exposed to an electron beam and the energy loss of the scattered electrons passing through the sample is detected, yielding information on the atoms the electrons interacted with. By scanning across a larger 2D window and collecting an EELS spectrum for each pixel, chemical composition maps across the SiO_2/SiC interface can be obtained.

For the EELS analysis, lamellas with all three distinct SiC surface morphologies were prepared. In the case of the macrostep terraces on the surface-modified sample [parallel to the (0001) basal plane], a distinction between completely step-free regions and regions with single steps, sporadically present at such terraces, was made. All samples used for the EELS analysis had the same oxide thickness of 30 nm.

Figure 3 shows the high-resolution dark-field (DF) cross-section STEM images and corresponding EELS profiles for different interface regions. For the EELS profiles, several rows of the 2D scans parallel to the interface were averaged to reduce the noise. For the interpretation of the profiles, an approach similar to that suggested in Ref. [12] was followed where the interface (at the origin of the x axis) is determined with the help of the dark-field image using the last atomic SiC crystal plane. Three chemical components are separately analyzed: apart from the carbon and oxygen maps,

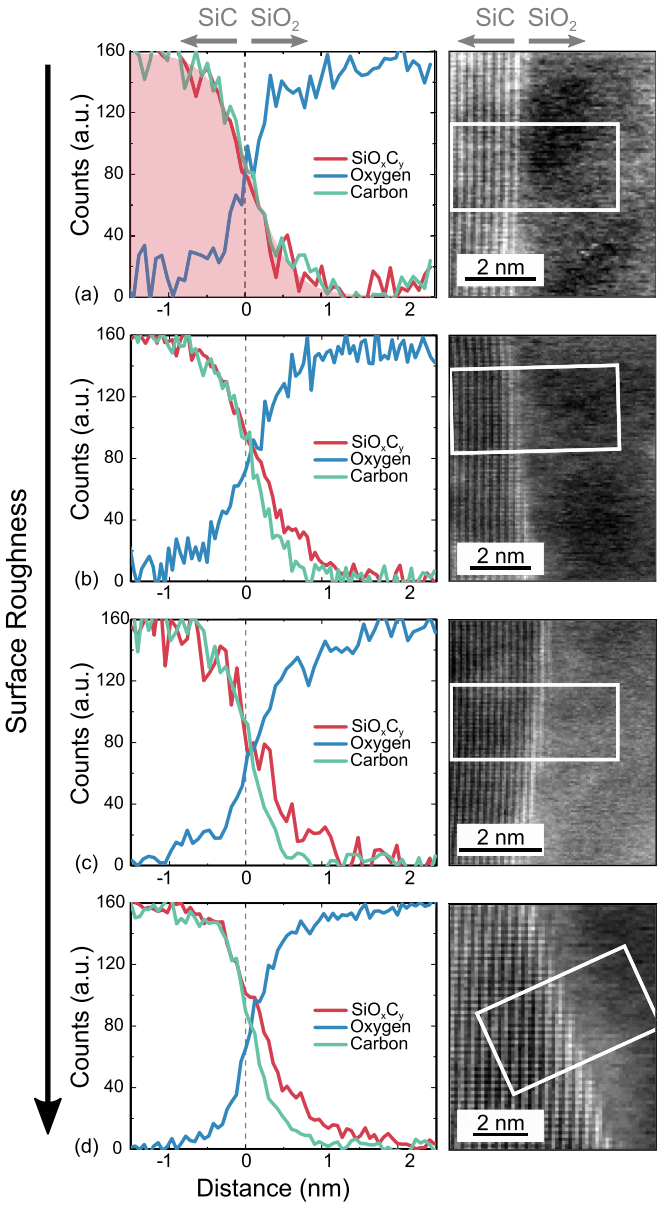

FIG. 3. EELS profiles (left) with traces of carbon, oxygen, and SiO_xC_y and corresponding dark-field STEM images (right) from (a) an atomically flat region of a terrace, (b) a single step of a terrace, (c) a nonmodified surface with microsteps, and (d) a step-bunched macrostep riser. For the EELS line profiles, EELS spectra were averaged over a 2 nm large area parallel to the interface. In (a), also a reference SiO_xC_y profile of a deposited SiO_2/SiC interface is shown (shaded area) where no transition region is expected. In the case of the atomically flat terrace, both the C signal and the SiO_xC_y spectrum overlap perfectly with the reference sample.

substoichiometric SiO_xC_y (also including suboxides without any C atoms, i.e., SiO_x) from an energy window between 99 eV and 103 eV is extracted. By choosing this energy range, fully oxidized Si^{+4} atoms at energies above 104 eV do not contribute to the EELS signal and the profile quickly decreases in the SiO_2 bulk where all Si atoms are surrounded by oxygen.

Flat terraces, depicted in Fig. 3(a), exhibit a complete last SiC bilayer stacking without any observable steps in the DF image and a very good overlap of the C and SiO_xC_y signals in the EELS spectrum. Given the narrow width of the transition region between SiC bulk and the SiO_2 of less than 2 nm which is close to the sensitivity limit of this technique [29], we consider this interface to be abrupt. Also shown in Fig. 3(a) is the smoothened substoichiometric SiO_xC_y EELS profile of a SiO_2/SiC interface with a low-temperature deposited SiO_2 which was analyzed in parallel to the macrostepped samples. The perfect overlap of the two SiO_xC_y spectra supports our interpretation of an ideal SiO_2/SiC interface on the atomically flat terrace.

For a flat SiC terrace where a few single steps are present [Fig. 3(b)], the drop of the SiO_xC_y signal moves away from the interface, which is interpreted as an increased contribution of an only partially oxidized SiC plane containing some residual Si, C, and O bonds.

An increased SiO_xC_y signal is also observed for the SiO_2/SiC sample which did not undergo the Si-melt process shown in Fig. 3(c). This trend is even more pronounced in the case of the strongly stepped riser facet as depicted in Fig. 3(d). Here, the SiO_xC_y signal extends more than 1 nm into the SiO_2 bulk, suggesting an increased thickness of the transition layer and a larger contribution of a substoichiometric SiO_xC_y region.

For some of the EELS profiles which were acquired either on micro- or macrostepped SiC surface regions, we did observe a slightly increased carbon signal, appearing as a small peak at 0.2 nm away from the interface in the SiO_2 bulk (not shown here; see the Supplemental Material [46]).

C. PL analysis

In order to correlate the observed thickness variations of the transition region with the density of interface defects, a mapping of the SiO_2/SiC interface was performed using confocal PL measurements. Figures 4(b) and 4(d) depict reflectivity measurements of the SiO_2/SiC interface on samples with and without a previously employed Si-melt process where the height profile of the inspected regions is clearly visible. Confocal images of the same regions [Figs. 4(d) and 4(e)] show the drastic difference in emission signal for the different surface morphologies: While the atomically flat terraces exhibit a defect density of approximately 0.62 emitters/μm^2 with an average defect emission count rate of 128 kilocounts per second at an excitation power of 1 mW, a much higher density of defects is observed as bright vertical lines along the $\langle 1\bar{1}00\rangle$ direction at the stepped risers. A slightly higher density of defects (1 emitter/μm^2) but an emission intensity similar to that for the terraces is found for nonmodified surface regions. An increased number of defect centers is also observed close to areas with crystal defects or damage (e.g., scratches) of the epitaxial layer (not shown here).

The corresponding room temperature ensemble PL spectra, measured with a laser spot size of 2 μm, are presented in Fig. 5. Single interface defects exhibit a noticeable spectral variability, leading to a broad peak centered around 750 nm. Compared to a nonmodified surface, the photoluminescence slightly decreases for areas on the macrosteps terrace, while it is considerably higher for the riser. This is in accordance with conductance measurements reported previously [21] and with

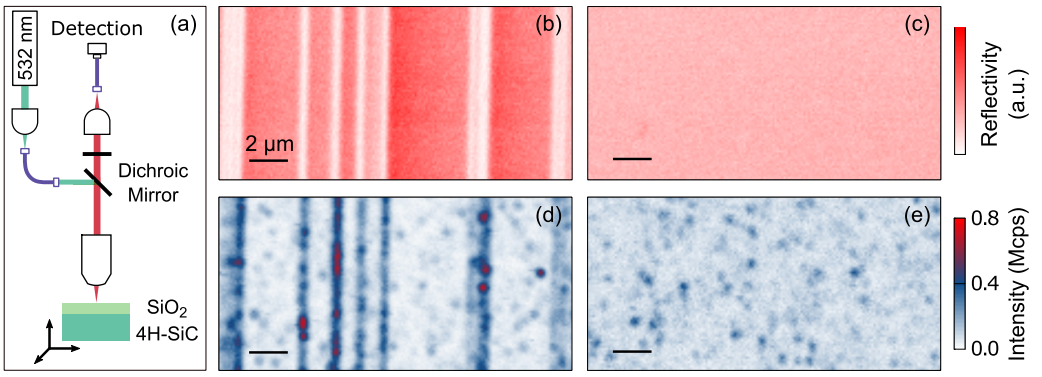

FIG. 4. (a) Schematic of the confocal microscope. A laser is directed onto a dichroic mirror via a fiber and directed on the sample which is mounted on an *xyz* stage. The PL emission is guided through another fiber and detected with a single-photon avalanche photodiode. (b)–(e) Reflectivity (top) and confocal PL maps (bottom) of (b), (d) a modified surface after the Si-meld process with flat terraces and stepped risers and (c), (e) a common microstepped surface. The reflectivity maps were measured without the 532 nm long pass filter and at a greatly reduced laser power. The bright vertical lines along the $\langle 1\bar{1}00\rangle$ axis in the confocal PL maps indicate a higher defect density for the riser facets.

a macroscopic capacitance-voltage analysis [30] performed on the same set of samples (see the Supplemental Material [46]). We attribute the decrease of D_{it} at the macrostepped regions to the enhanced interface quality at the atomically flat terraces where no microsteps are present. Even when averaging over a larger number of terraces and risers (as for the case of a standard CV measurement with large MOS contacts), the relatively low defect density of the terraces exceeds the influence of the high defect density at the risers and an overall improvement of the D_{it} value is observed.

D. Local-DLTS analysis

In order to obtain quantitative information on the defects related to the surface morphology of off-axially grown 4*H*-C, a newly developed modification of the conventional DLTS technique was employed which allows the spatial mapping of interface defect densities with a sub-μm resolution [25]. The working principle of local-DLTS is schematically depicted in Fig. 6(a). A conductive sharp tip contacts the surface of the SiO_2/SiC sample, forming a very small MOS capacitor. By applying a voltage pulse to the sample, the capacitance

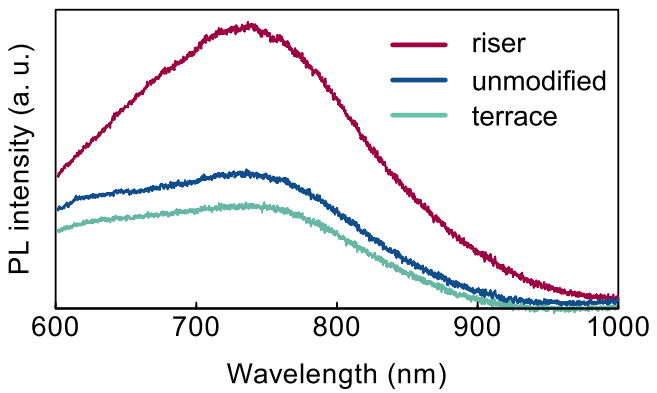

FIG. 5. PL spectra of the SiO_2/SiC interface with three different SiC surface morphologies. An increased density of defects is observed at the stepped risers, whereas the atomically flat terraces show lower intensities compared to the unmodified microstepped SiC surface.

deviation beneath the cantilever tip leads to a modulation of the oscillation frequency of the SNDM probe, and from the time evolution of the frequency shift, a transient capacitance, and with that a spatially resolved D_{it} value, is derived. A more detailed explanation of the measurement principle and D_{it} extraction is given in the Supplemental Material [46].

Figure 6 shows local-DLTS images (1 μm × 1 μm) of the SiO_2/SiC interface, acquired on a macrostep formed during the Si-melt process [Fig. 6(b)] and on an unmodified SiC surface [Fig. 6(c)] at 300 K. As is the case for the PL analysis presented in Fig. 4, a clear dependence of the defect distribution on the morphology of the SiC surface is observed. While the riser facets with strong step bunching exhibit D_{it} values up to $1 \times 10^{14}\,\mathrm{cm^{-2}eV^{-1}}$, the flat terrace regions in Fig. 6(b) have average defect densities of $4 \times 10^{13}\,\mathrm{cm^{-2}eV^{-1}}$. On the sample where no Si-melt process was performed, the average D_{it} value is $5 \times 10^{13}\,\mathrm{cm^{-2}eV^{-1}}$ which is slightly greater compared to the terrace regions.

Since the interface defect density is a function of the oxide thickness (t_{ox}) below the probing tip, local variations of t_{ox} on macrostepped SiC surfaces due to the orientation-dependent oxide growth rate have to be carefully considered [6,31,32]. For the calculation of D_{it}, experimentally determined t_{ox} values were therefore used. Cross-section TEM studies performed on samples with the same oxidation process (1050°C for 4h) showed that the oxide on the stepped risers of an isolated macrostep [parallel to the $(11\bar{2}x)$ plane] was around 11 nm thick while on the terraces [parallel to the (0001) plane], a thickness of only $t_{ox} = 7$ nm was measured [10]. For the microstepped regions [parallel to the 4° off-axis (0001) plane], an oxide thickness of 8 nm was extracted.

IV. DISCUSSION

The origin of the high density of interface defect states at the SiO_2/SiC interface has been the scope of a large number of dedicated studies, both theoretically and experimentally. Here we interpret our results in the context of well-established interpretations, starting with the concept of dangling bonds at the oxide/semiconductor interface. As pointed out by

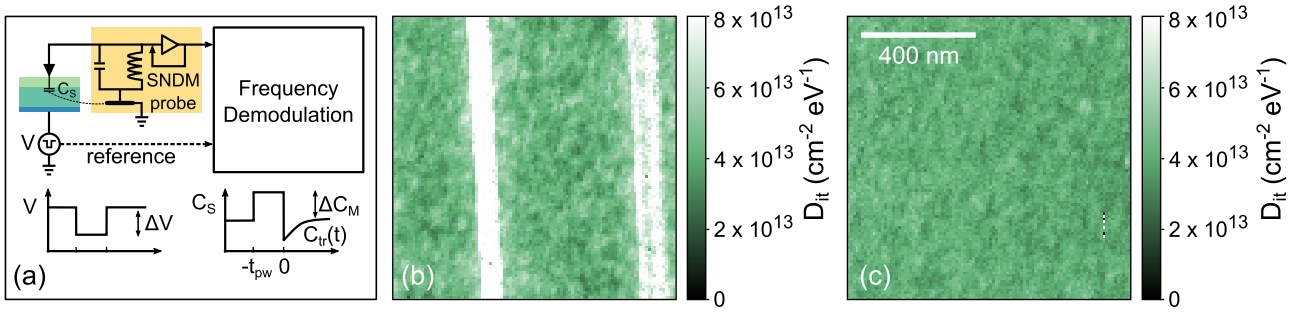

FIG. 6. (a) Schematic of the local-DLTS setup, adapted from [25]. (b) D_{it} map for a sample with enhanced macrosteps. The oxide thickness on terraces and risers was estimated to be 7 nm and 11 nm, respectively. (c) D_{it} map for an unmodified SiC surface with 8 nm thermally grown SiO_2 on top. For both D_{it} maps, $E_{it} = 0.38\,\mathrm{eV}$.

various groups [12,33,34] and in accordance with the presented STEM analysis, incomplete crystal planes at the interface favor the generation of a disordered atomic region, giving rise to an increased density of dangling bonds at the interface. Contradicting explanations of the nature of these dangling bonds can be found in the literature, suggesting either carbon [33–36] or silicon dangling bonds [37–39]. Considering the large number of zero-phonon lines observed in low and room temperature PL for similar oxidation processes on 4*H*-C [40,41], correlated C dangling bonds with large varieties of possible geometries and backbone structures as proposed in Ref. [33] might be likely candidates.

Another explanation for oxidation-related interface defects is bigger carbon accumulations at the interface ("carbon-cluster model") [13,42,43]. Despite the large number of samples studied with STEM, we did not observe pronounced C clustering. However, this might also be a limitation of the method itself: first of all, a considerable number of such clusters would be needed to increase the likelihood of capturing one of them in the very small area of a typical TEM lamella. In addition, it would be difficult to distinguish such clusters from carbon contaminants of a similar size (about 3 nm) introduced during lamella fabrication. Nevertheless, for some of the EELS profiles of stepped regions we did observe a slightly increased carbon signal, appearing as a small peak at 0.2 nm away from the interface in the SiO_2. An example of such a profile is given in the Supplemental Material [46]. Since the signal is almost at noise level, more statistics are needed to clarify whether this can be interpreted as C excess at the interface.

From the PL analysis, a close confinement of the defects to the SiO_2/SiC interface can be deduced: polarization measurements of the samples (see the Supplemental Material [46]) have established that the optical dipoles are aligned along the major axes of the SiC crystal, suggesting that they are formed in the oxide in close proximity to the SiO_2/SiC interface. An observed variability of the dipole orientation is attributed to local strain or a distorted crystal environment. Furthermore, a recent study of the oxidation-induced strain at the SiO_2/SiC interface characterized by in-plane x-ray diffractometry reported indeed an extended region of lattice distortion [44].

Finally, point defects such as carbon or silicon vacancies are unlikely to strongly contribute to the D_{it} values obtained in the local-DLTS measurements: similarly to previously reported PL studies of the SiO_2/SiC interface both at low and at room temperature [41,45], the position of the zero-phonon line for different defect centers varied considerably in our measurements, which is normally not the case for point defects.

V. CONCLUSION

In this study, structural, optical, and electronic properties of various stepped surface morphologies of 4*H*-C were investigated and differences in the SiO_2/SiC interface quality due to surface stepping were observed. The comprehensive analysis suggests that the surface faceting which is always present at off-axially grown 4*H*-C epitaxial layers promotes the formation of an extended oxycarbide interface region and hence the generation of interface defect states.

STEM/EELS revealed an abrupt interface in the case of the macrostep terraces, similar to a low-temperature deposited SiO_2 where no transition region is expected. The strongly faceted riser with $(11\bar{2}x)$ orientation, on the other hand, exhibited a broadened interface region with incomplete crystal planes leading to an increased signal of partially oxidized Si. A nonmodified reference sample with the commonly observed microfaceting of the surface showed properties similar to those of the stepped risers.

For a qualitative analysis of the interface defect densities, PL ensemble measurements at room temperature were conducted and an increased emitter density for the $(11\bar{2}x)$ plane was observed. Local-DLTS measurements were in accordance with the optical analysis and showed higher D_{it} values at an energy of $E_{it} = E_C - 0.38\,\mathrm{eV}$ ($D_{it} = 1 \times 10^{14}\,\mathrm{cm^{-2}eV^{-1}}$) for the stepped riser surface and the lowest interface defect density for the flat terrace regions.

Our results provide evidence that an atomically flat SiC surface enables the formation of an abrupt SiO_2/SiC interface with reduced interface defect densities. Apart from the technical implications of our results for the development of high-quality oxide/semiconductor interfaces, this work also highlights the great potential of spatially resolving analysis techniques for a fast and nondestructive interface characterization: extracting the local defectivity can already give a first indication on the quality of the SiO_2/SiC interface without the need of fabricating dedicated test devices.

ACKNOWLEDGMENTS

This research project is part of the National Research Programme "Energy Turnaround" (NRP 70) of the Swiss National Science Foundation (SNSF). Further information on the National Research Programme can be found at www.nrp70.ch. This work was supported by the Australian Research Council Centre of Excellence for Quantum Computation and Communication Technology (Grant No. CE110001027).

[1] S. Castelletto, B. C. Johnson, V. Ivády, N. Stavrias, T. Umeda, A. Gali, and T. Ohshima, A silicon carbide room-temperature single-photon source, Nat. Mater. **13**, 151 (2013).

[2] M. Widmann, S.-Y. Lee, T. Rendler, N. T. Son, H. Fedder, S. Paik, L.-P. Yang, N. Zhao, S. Yang, I. Booker, A. Denisenko, M. Jamali, S. A. Momenzadeh, I. Gerhardt, T. Ohshima, A. Gali, E. Janzén, and J. Wrachtrup, Coherent control of single spins in silicon carbide at room temperature, Nat. Mater. **14**, 164 (2014).

[3] W. F. Koehl, B. B. Buckley, F. J. Heremans, G. Calusine, and D. D. Awschalom, Room temperature coherent control of defect spin qubits in silicon carbide, Nature (London) **479**, 84 (2011).

[4] H. Kraus, V. A. Soltamov, F. Fuchs, D. Simin, A. Sperlich, P. G. Baranov, G. V. Astakhov, and V. Dyakonov, Magnetic field and temperature sensing with atomic-scale spin defects in silicon carbide, Sci. Rep. **4**, 5303 (2014).

[5] T. Ueda, H. Nishino, and H. Matsunami, Crystal growth of SiC by step-controlled epitaxy, J. Cryst. Growth **104**, 695 (1990).

[6] T. Kimoto and J. A. Cooper, *Fundamentals of Silicon Carbide Technology* (John Wiley & Sons Singapore Pt. Ltd., 2014).

[7] T. Kimoto, Z. Y. Chen, T. Satoshi, S.-i. Nakmura, N. Onojima, and H. Matsunami, Surface morphological structures of 4H-, 6H-, and 15R-SiC (0001) epitaxial layers grown by chemical vapor deposition, Jpn. J. Appl. Phys. **40**, 3315 (2001).

[8] G. Pennington, S. Potbhare, J. M. McGarrity, A. Lelis, and N. Goldsman, Electron transport at technologically significant stepped 4H-SiC/SiO_2 interfaces, in *SISPAD 2006* (IEEE, 2006).

[9] H. Watanabe and T. Hosoi, Fundamental aspects of silicon carbide oxidation, in *Physics and Technology of Silicon Carbide Devices* (InTech, 2012).

[10] J. Woerle, V. Šimonka, E. Müller, A. Hössinger, H. Sigg, S. Selberherr, J. Weinbub, M. Camarda, and U. Grossner, Surface morphology of 4H-SiC after thermal oxidation, Mater. Sci. Forum **963**, 180 (2019).

[11] G. Gruber, J. Cottom, R. Meszaros, M. Koch, G. Pobegen, T. Aichinger, D. Peters, and P. Hadley, Electrically detected magnetic resonance of carbon dangling bonds at the Si-face 4H-SiC/SiO_2 interface, J. Appl. Phys. **123**, 161514 (2018).

[12] P. Fiorenza, F. Iucolano, G. Nicotra, C. Bongiorno, I. Deretzis, A. L. Magna, F. Giannazzo, M. Saggio, C. Spinella, and F. Roccaforte, Electron trapping at SiO_2/4H-SiC interface probed by transient capacitance measurements and atomic resolution chemical analysis, Nanotechnology **29**, 395702 (2018).

[13] L. Liu, C. Jiao, L. C. Feldman, and S. Dhar, The influence of SiC/SiO_2 interface morphology on the electrical characteristics of SiC MOS structures, in *2014 IEEE Workshop on Wide Bandgap Power Devices and Applications* (IEEE, 2014), pp. 103-106.

[14] A. Frazzetto, F. Giannazzo, P. Fiorenza, V. Raineri, and F. Roccaforte, Limiting mechanism of inversion channel mobility in Al-implanted lateral 4H-SiC metal-oxide semiconductor field-effect transistors, Appl. Phys. Lett. **99**, 072117 (2011).

[15] M. Cabello, V. Soler, D. Haasmann, J. Montserrat, J. Rebollo, and P. Godignon, Evidence of channel mobility anisotropy on 4H-SiC MOSFETs with low interface trap density, Mater. Sci. Forum **963**, 473 (2019).

[16] M. Fujii and S. Tanaka, Ordering Distance of Surface Nanofacets on Vicinal 4*H*-SiC (0001), Phys. Rev. Lett. **99**, 016102 (2007).

[17] M. Camarda, A. Severino, P. Fiorenza, V. Raineri, S. Scalese, C. Bongiorno, A. L. Magna, F. L. Via, M. Mauceri, and D. Crippa, On the "step bunching" phenomena observed on etched and homoepitaxially grown 4H silicon carbide, Mater. Sci. Forum **679–680**, 358 (2011).

[18] L. Dong, G. Sun, L. Zheng, X. Liu, F. Zhang, G. Yan, L. Tian, X. Li, and Z. Wang, Analysis and modeling of localized faceting on 4H-SiC epilayer surfaces, Phys. Status Solidi A **210**, 2503 (2013).

[19] T. Masuda, S. Harada, T. Tsuno, Y. Namikawa, and T. Kimoto, High channel mobility of 4H-SiC MOSFET fabricated on macro-stepped surface, Mater. Sci. Forum **600–603**, 695 (2008).

[20] V. Soulière, D. Carole, M. Camarda, J. Woerle, U. Grossner, O. Dezellus, and G. Ferro, 4H-SiC(0001) surface faceting during interaction with liquid Si, Mater. Sci. Forum **858**, 163 (2016).

[21] M. Camarda, J. Woerle, V. Soulière, G. Ferro, H. Sigg, U. Grossner, and J. Gobrecht, Analysis of 4H-SiC MOS capacitors on macro-stepped surfaces, Mater. Sci. Forum **897**, 107 (2017).

[22] M. A. Capano, S.-H. Ryu, J. A. Cooper, and M. R. Buss, Dopant activation and surface morphology of ion implanted 4H and 6H silicon carbide, J. Electron. Mater. **27**, 370 (1998).

[23] Y. Negoro, K. Katsumoto, T. Kimoto, and H. Matsunami, Electronic behaviors of high-dose phosphorus-ion implanted 4H-SiC (0001), J. Appl. Phys. **96**, 224 (2004).

[24] D. Meertens, M. Kruth, and K. Tillmann, FEI Helios NanoLab 400S FIB-SEM, J. Large-Scale Research Facilities **2**, 1 (2016).

[25] N. Chinone and Y. Cho, Local deep level transient spectroscopy using super-higher-order scanning nonlinear dielectric microscopy and its application to imaging two-dimensional distribution of SiO_2/SiC interface traps, J. Appl. Phys. **122**, 105701 (2017).

[26] Y. Yamagishi and Y. Cho, Nanosecond microscopy of capacitance at SiO_2/4H-SiC interfaces by time-resolved scanning nonlinear dielectric microscopy, Appl. Phys. Lett. **111**, 163103 (2017).

[27] W. Chen and M. A. Capano, Growth and characterization of 4H-SiC epilayers on substrates with different off-cut angles, J. Appl. Phys. **98**, 114907 (2005).

[28] K. Wada, T. Kimoto, K. Nishikawa, and H. Matsunami, Epitaxial growth of 4H-SiC on 5 degree off-axis (0001) and (000$\bar{1}$) substrates by hot-wall chemical vapor deposition, J. Cryst. Growth **291**, 370 (2006).

[29] R. F. Egerton, Scattering delocalization and radiation damage in STEM-EELS, Ultramicroscopy **180**, 115 (2017).

[30] H. Yoshioka, T. Nakamura, and T. Kimoto, Accurate evaluation of interface state density in SiC metal-oxide-semiconductor structures using surface potential based on depletion capacitance, J. Appl. Phys. **111**, 014502 (2012).

[31] K. Ueno, Orientation dependence of the oxidation of SiC surfaces, Phys. Status Solidi A **162**, 299 (1997).

[32] M. Schürmann, S. Dreiner, U. Berges, and C. Westphal, Structure of the interface between ultrathin SiO_2 films and 4*H*-SiC(0001), Phys. Rev. B **74**, 035309 (2006).

[33] S. Wang, S. Dhar, S.-r. Wang, A. C. Ahyi, A. Franceschetti, J. R. Williams, L. C. Feldman, and S. T. Pantelides, Bonding at the SiC-SiO_2 Interface and the Effects of Nitrogen and Hydrogen, Phys. Rev. Lett. **98**, 026101 (2007).

[34] J. Cottom, G. Gruber, G. Pobegen, T. Aichinger, and A. L. Shluger, Recombination defects at the 4H-SiC/SiO_2 interface investigated with electrically detected magnetic resonance and ab initio calculations, J. Appl. Phys. **124**, 045302 (2018).

[35] J. L. Cantin, H. J. von Bardeleben, Y. Ke, R. P. Devaty, and W. J. Choyke, Hydrogen passivation of carbon Pb like centers at the 3C- and 4H-SiC/SiO_2 interfaces in oxidized porous 4H-SiC, Appl. Phys. Lett. **88**, 092108 (2006).

[36] T. Umeda, G.-W. Kim, T. Okuda, M. Sometani, T. Kimoto, and S. Harada, Interface carbon defects at 4H-SiC(0001)/SiO_2 interfaces studied by electron-spin-resonance spectroscopy, Appl. Phys. Lett. **113**, 061605 (2018).

[37] C. J. Cochrane, P. M. Lenahan, and A. J. Lelis, An electrically detected magnetic resonance study of performance limiting defects in SiC metal oxide semiconductor field effect transistors, J. Appl. Phys. **109**, 014506 (2011).

[38] C. J. Cochrane, P. M. Lenahan, and A. J. Lelis, Identification of a silicon vacancy as an important defect in 4H SiC metal oxide semiconducting field effect transistor using spin dependent recombination, Appl. Phys. Lett. **100**, 023509 (2012).

[39] M. A. Anders, P. M. Lenahan, and A. J. Lelis, Are dangling bond centers important interface traps in 4H-SiC metal oxide semiconductor field effect transistors? Appl. Phys. Lett. **109**, 142106 (2016).

[40] B. C. Johnson, J. Woerle, R. A. Parker, C. T. K. Lew, D. Haasmann, H. Knowles, B. Pingault, M. Atature, A. Gali, S. Dimitrijev, M. Camarda, and J. C. McCallum, Optically active defects at the SiC/SiO_2 interface (unpublished).

[41] Y. Abe, T. Umeda, M. Okamoto, R. Kosugi, S. Harada, M. Haruyama, W. Kada, O. Hanaizumi, S. Onoda, and T. Ohshima, Single photon sources in 4H-SiC metal-oxide-semiconductor field-effect transistors, Appl. Phys. Lett. **112**, 031105 (2018).

[42] J. A. Taillon, J. H. Yang, C. A. Ahyi, J. Rozen, J. R. Williams, L. C. Feldman, T. S. Zheleva, A. J. Lelis, and L. G. Salamanca-Riba, Systematic structural and chemical characterization of the transition layer at the interface of NO-annealed 4H-SiC/SiO_2 metal-oxide-semiconductor field-effect transistors, J. Appl. Phys. **113**, 044517 (2013).

[43] T. Hatakeyama, H. Matsuhata, T. Suzuki, T. Shinohe, and H. Okumura, Microscopic examination of SiO_2/4H-SiC interfaces, Mater. Sci. Forum **679–680**, 330 (2011).

[44] A. D. Hatmanto and K. Kita, Thermal-oxidation-induced local lattice distortion at surface of 4H-SiC(0001) characterized by in-plane x-ray diffractometry, Appl. Phys. Express **11**, 011201 (2018).

[45] S. Castelletto, B. C. Johnson, C. Zachreson, D. Beke, I. Balogh, T. Ohshima, I. Aharonovich, and A. Gali, Room temperature quantum emission from cubic silicon carbide nanoparticles, ACS Nano **8**, 7938 (2014).

[46] See Supplemental Material at http://link.aps.org/supplemental/10.1103/PhysRevMaterials.3.084602 for additional AFM and EELS profiles as well as further details on the capacitance-voltage and DLTS analysis. Also presented are PL polarization measurements of the SiO_2/SiC interface formed on different SiC surface morphologies.