

Atomic-layer doping of SiGe heterostructures for atomic-precision donor devices

E. Bussmann,^{1,*} John King Gamble,^{2,†} J. C. Koepke,³ D. Laroche,³ S. H. Huang,^{4,5} Y. Chuang,^{4,5} J.-Y. Li,^{4,5} C. W. Liu,^{4,5} B. S. Swartzentruber,¹ M. P. Lilly,¹ M. S. Carroll,³ and T.-M. Lu³¹Center for Integrated Nanotechnologies, Sandia National Laboratories, Albuquerque, New Mexico 87185, USA²Center for Computing Research, Sandia National Laboratories, Albuquerque, New Mexico 87185, USA³Sandia National Laboratories, Albuquerque, New Mexico 87185, USA⁴Department of Electrical Engineering and Graduate Institute of Electronic Engineering, National Taiwan University, Taipei 10617, Taiwan, R.O.C.⁵National Nano Device Laboratories, Hsinchu 30077, Taiwan, R.O.C.

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As a first step to porting scanning tunneling microscopy methods of atomic-precision fabrication to a strained-Si/SiGe platform, we demonstrate post-growth P atomic-layer doping of SiGe heterostructures. To preserve the substrate structure and elastic state, we use a $T \leq 800^\circ\text{C}$ process to prepare clean $\text{Si}_{0.86}\text{Ge}_{0.14}$ surfaces suitable for atomic-precision fabrication. P-saturated atomic-layer doping is incorporated and capped with epitaxial Si under a thermal budget compatible with atomic-precision fabrication. Hall measurements at $T = 0.3\text{ K}$ show that the doped heterostructure has $R_{\square} = 570 \pm 30\ \Omega$, yielding an electron density $n_e = 2.1 \pm 0.1 \times 10^{14}\text{ cm}^{-2}$ and mobility $\mu_e = 52 \pm 3\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$, similar to saturated atomic-layer doping in pure Si and Ge. The magnitude of μ_e and the complete absence of Shubnikov–de Haas oscillations in magnetotransport measurements indicate that electrons are overwhelmingly localized in the donor layer, and not within a nearby buried Si well. This conclusion is supported by self-consistent Schrödinger-Poisson calculations that predict electron occupation primarily in the donor layer.

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I. INTRODUCTION

Atomic-precision fabrication via scanning tunneling microscopy (STM) hydrogen depassivation lithography has blossomed as a unique route to form doped-Si and Ge nanoelectronics with single-atom selectivity and feature sizes [1–7]. Atomic precision is enabling for Si quantum computing research [8–15] with potential utility in other fields such as limit testing in scaling and quantum confined geometries in conventional microelectronics [16–20].

A step to facilitate broader electronic device applications is to integrate atomic-precision doping into vertically gated configurations incorporating metal-insulator-semiconductor (MIS) capacitors [21–23]. For example, the archetypal Kane proposal utilizes single donors placed in MIS stacks [9–12]. To protect atomic-precision donors from disordering via diffusion, the thermal budget to integrate a gate stack is constrained to temperatures too low for ideal SiO_2 growth by furnace oxidation [24–26]. This has inspired attempts to integrate gate stacks using insulators grown by lower-temperature methods. Unfortunately, these yield more defective films and disorder with measurable effects on donor device performance [22,23].

Strained-layer band-offset engineering via thin-film heteroepitaxy is a mature technique to form an interfacial barrier at a relatively low growth thermal budget [10,27]. Layered

strained-Si (s-Si) and SiGe heterostructures have the benefit of pristine all-epitaxial interfaces with disorder that compares well with the highest-quality Si/SiO₂ interfaces [27,28]. As a measure of disorder, exceptional Si/SiO₂ field-effect devices undergo a $T < 1\text{ K}$ metal-insulator transition at critical electron densities $n_c = 0.6\text{--}0.8 \times 10^{11}\text{ cm}^{-2}$ with peak mobilities $\mu_e \sim 2\text{--}5 \times 10^4\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ [29,30]. By comparison, good SiGe field-effect devices turn on at $n_c = 0.3\text{--}0.6 \times 10^{11}\text{ cm}^{-2}$ achieving peak $\mu_e \sim 10^5\text{--}10^6\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ [31–35]. In our SiGe substrate, we find $n_c = 0.6 \times 10^{11}\text{ cm}^{-2}$ and peak $\mu_e = 7 \times 10^5\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ at $T = 0.3\text{ K}$ prior to adding atomic-layer doping [33]. Figure 1(a) shows a schematic of the field-effect device used to characterize transport in the s-Si well (see Ref. [33]). Figure 1(b) shows our device to test transport after atomic-layer doping.

Integrating atomic-precision doping with SiGe heterostructures leverages advantages of all-epitaxial order inherent in both platforms. A few works have proposed donor spin qubits in s-Si/SiGe [10,11]. Figure 1(c) shows a simplified sketch for a two-qubit interaction. Qubit control would be via MIS gating to move electrons on and off the nucleus, or into SiGe layers, to tune spin precession. Spins would couple by drawing electrons to heterointerfaces, e.g., to form two-electron quantum dots. Spin initialization and readout would be by established methods using single-electron transistors formed by MIS accumulation in the well [10,11]. Another potential application is two-dimensional (2D) atomic-precision modulation doping to investigate effects of carefully tuned ordered potentials on 2D electron transport at heterostructure interfaces, which may permit tailor-made electronic band structures enforced by

*ebussma@sandia.gov

†Current address: Microsoft Quantum – Redmond (QuArC), 1 Microsoft Way, Redmond, WA 98052, USA; john.gamble@microsoft.com

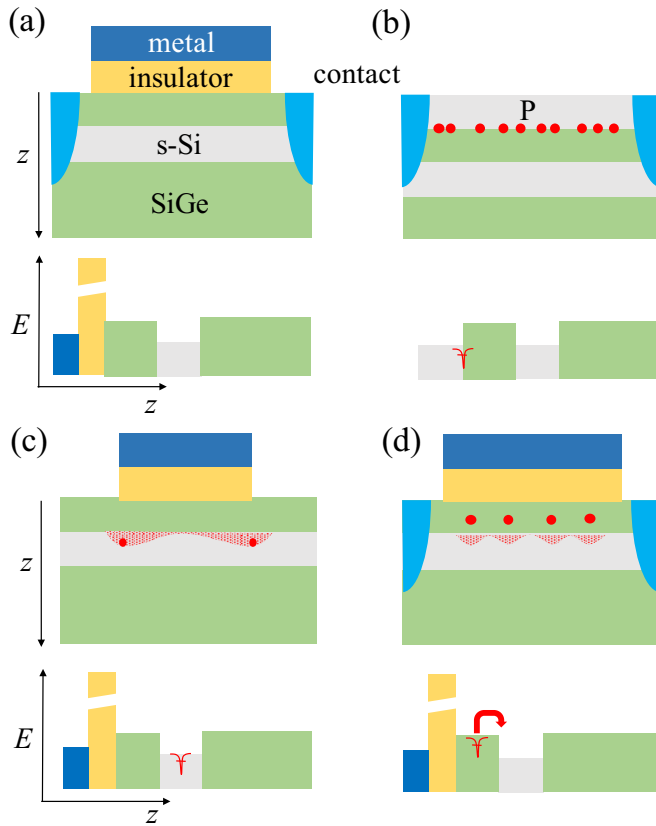


FIG. 1. Schematic cross sections of heterostructure test devices and proposed device concepts. The lower panels show schematics of relative conduction band position in each layer. (a) An undoped field-effect transistor for characterizing transport of gate-accumulated two-dimensional electrons in the s-Si well prior to our atomic-layer doping process. (b) A schematic of the atomic-layer-doped transport device produced in this work. The doping is a two-dimensional (2D) random substitutional Si:P alloy. Electron transfer from the donor layer to the s-Si well is blocked by the band alignments. (c) Gate-stack isolation for donor spin qubits via band offsets in an all-epitaxial Si environment away from Si-insulator interfaces. Spin initialization and readout would be enabled by gate-defined accumulation-mode single-electron transistors (not shown). (d) Concept for a high electron mobility transistor where STM-defined atomic-precision modulation doping creates a periodic potential in the s-Si transport channel.

donor periodicity [16]. Figure 1(d) shows a schematic of a field-effect device with ordered modulation doping in the channel. Ordered doping potentials promote channel mobility, with anticipated applications in high-electron mobility transistors [27].

Here, we demonstrate atomic-layer doping of a s-Si/SiGe heterostructure via a thermal process entirely compatible with STM atomic-precision fabrication and our epitaxial SiGe heterostructure, which can withstand $T \lesssim 850^\circ\text{C}$ annealing [36]. We incorporate P atomic-layer doping into the heterostructure by a process thermally compatible with atomic-precision fabrication. Results of each process step are characterized and contrasted with outcomes on relaxed bulk Si. Post-growth secondary ion mass spectroscopy (SIMS) yields an integrated P density $N_D \sim 1.2 \times 10^{14} \text{ cm}^{-2}$ with a full width at half-maximum (FWHM) = 3 nm, similar to

results demonstrated for pure Si and Ge [5,37]. Hall effect measurements show that the doped heterostructure has an electron density $n_e = 2.1 \pm 0.1 \times 10^{14} \text{ cm}^{-2}$ and mobility $\mu_e = 52 \pm 3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. These numbers are consistent with electron transport predominantly in the atomic-layer doping. Magnetotransport measurements to $\pm 8 \text{ T}$ reveal only a small $B = 0 \text{ T}$ weak-localization bump, characteristic of transport via the atomic-layer doping, and no sign of Shubnikov-de Haas oscillations characteristic of transport via the high-mobility strained Si well [33]. Self-consistent Schrödinger-Poisson calculations confirm the intuitive picture that electrons primarily populate the donor layer.

II. DEVICE FABRICATION AND PHYSICAL CHARACTERIZATION

Atomic-precision fabrication has been demonstrated on (100)-oriented Si [1–4], Ge [5,6], strained-Si on insulator (s-SOI) [38,39], and Ge on insulator [40]. Needless to say, the recipes differ between each, owing to unique thermal and chemical considerations [cf. materials-specific growth recipes for molecular beam epitaxy (MBE) of Si vs Ge [41,42]]. In principle, s-SOI also provides a platform for strained-layer band engineering, but we consistently find that the s-SOI surface is rough on a nanometer scale owing to bulk-elasticity-driven step bunching [38,39,43]. Therefore, we have chosen to investigate donor placement on the relaxed SiGe surface, which as we will show, does not suffer from the inherent step-bunching problem.

We perform atomic-layer doping in an ultrahigh vacuum ($5 \times 10^{-10} \text{ Torr}$) scanning tunneling microscope (UHV STM) equipped with a phosphine (PH_3) gas source and a Si MBE source (joule heated solid Si, homebuilt). The substrates for our experiments are s-Si/Si_{0.86}Ge_{0.14} heterostructures grown by UHV chemical vapor deposition using SiH₄ and GeH₄ as precursors at $T = 550^\circ\text{C}$. The substrates have a 20-nm-thick s-Si well and a 50-nm-thick relaxed Si_{0.86}Ge_{0.14} cap. Further details about the substrate growth and characterization can be found in Ref. [33].

Prior to atomic-layer doping experiments, we perform an *ex situ* wet chemical cleaning procedure, and annealing in the UHV STM. The samples are cleaned by three cycles of chemical oxidation (3:1 H₂SO₄ : H₂O₂, 90 °C, 5 min) and reduction (6:1 NH₄F:HF, 10 s), followed by a rinse in deionized H₂O. Samples are exceptionally hydrophobic upon extraction (presumably hydrogen terminated). Two different chemical and annealing recipes yield suitably clean flat surfaces for atomic-layer doping: (1) the H-terminated samples can be loaded into the UHV system and annealed at a temperature sufficient to desorb the hydrogen (650 °C, 15 s), or (2) samples can be oxidized (5:1:1 H₂O:H₂O₂:HCl, 60 °C, 5 min), then annealed hotter ($T = 800^\circ\text{C}$, 20 min) to remove the chemical oxide. Both approaches yield suitable surfaces and there is not yet any evident advantage to either approach.

Figure 2(a) shows STM images of a SiGe(100) surface prepared by our *ex situ* chemical process followed by UHV annealing at $T = 650^\circ\text{C}$ for 15 s. For contrast, Fig. 2(b) shows images of pure Si(100) surfaces prepared by annealing at 1200 °C for 10 s, yielding a characteristic step-terrace structure with the $2 \times 1/1 \times 2$ reconstruction.

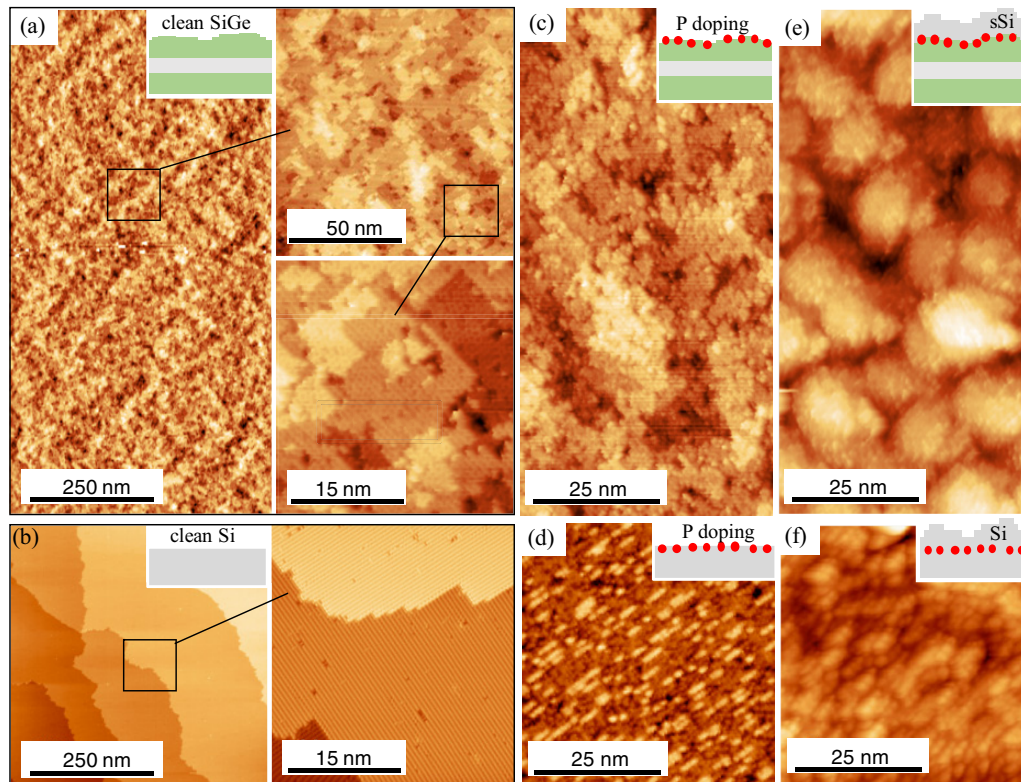


FIG. 2. STM images of the outcomes of the atomic-layer doping process on SiGe along with images of the process on the bulk Si(100) surface for comparison. (a) STM of $\text{Si}_{0.86}\text{Ge}_{0.14}$ surface following surface preparation by $650^\circ\text{C}/15$ s annealing in UHV. Smaller panels show details of the surface dimer-row reconstruction and monolayer-sized roughness. (b) A bulk Si surface prepared by a $1200^\circ\text{C}/10$ s anneal. (c) SiGe surface following P incorporation and (d) a bulk Si surface after P incorporation covered by monolayer-high islands of Si ejected by P incorporation into the surface. (e) SiGe:P after capping by 20-nm-thick epitaxial s-Si, and (f) the surface of a 20-nm-thick epitaxial Si cap on a Si:P structure. All images were acquired in filled states at -2 to -4 V bias and $I = 100$ pA.

Our lower-temperature process produces surfaces that show no definitive indication of any step-terrace order in larger areas [Fig. 2(a)], but higher magnification images (insets) reveal that the surface is simply rough at the atomic-layer scale with terraces only several nanometers wide. The terraces have mixed $p(2 \times 2)$ and $c(4 \times 2)$ reconstructions characteristic for SiGe and pure Ge [5]. The atomic-layer roughness is most likely caused by the chemical preparations, and the subsequent anneal is inadequate to activate surface smoothing. Roughness at the atomic-layer scale does not cause problems for atomically precise donor fabrication. Recently, McKibbin *et al.* have demonstrated entirely functional atomically precise donor devices on similarly rough epitaxial Si surfaces [44,45].

Atomic-layer doping is introduced by exposing the sample to PH_3 at 2×10^{-8} Torr for 5 min (6 Langmuir dose) at room temperature. A $T = 400^\circ\text{C}/30$ s anneal is used to incorporate P into lattice sites in the surface [1,2,32,38,40]. Figure 2(c) shows the surface after the incorporation anneal, which again is not hot enough to activate surface smoothing, leaving the characteristic atomic-layer roughness on the surface. For comparison, Fig. 2(d) shows an image of a relaxed bulk Si surface after a similar doping procedure. The surface is covered by ~ 0.25 monolayers of atomic-height islands formed by Si ejected onto the surface by P incorporation [1]. We do not observe similar islands on the SiGe surface most likely because

ejected Si or Ge is able to migrate to dense preexisting atomic steps, preventing island nucleation.

After P incorporation, samples are capped with (10–20)-nm-thick epitaxial s-Si grown at ~ 0.1 Å/s at $T = 250^\circ\text{C}$. Previous reports for Si and Ge structures indicate that this temperature is sufficiently low to inhibit P surface segregation, while yielding a crystalline capping layer [37]. Figure 2(e) shows an STM image of the surface of the capping layer, which is rough owing to the relatively low growth temperature. Under similar growth conditions, similarly rough surfaces are reported for both Si and Ge epitaxy [1,5,46]. Figure 2(f) shows an example of an STM image of the typical surface topography of a capping layer on pure bulk Si.

Although there is no clear indication of crystal order, e.g., the 2×1 reconstruction, in the STM images of the epitaxial s-Si cap, cross-sectional transmission electron microscopy (TEM) (Fig. 3) shows that the films are epitaxial. Figures 3(a) and 3(b) show that the SiGe layer structure is preserved with no evidence of threading dislocations in the field of view. Stacking faults are visible in the s-Si cap on the SiGe material. Figures 3(c) and 3(d) show cross-sectional TEM of the relaxed bulk Si:P structure for comparison. There are no stacking faults in the relaxed Si:P structure.

Secondary ion mass spectroscopy (SIMS) [Fig. 4(a)] shows that our recipe yields a sharply peaked $\text{FWHM} = 3$ nm,

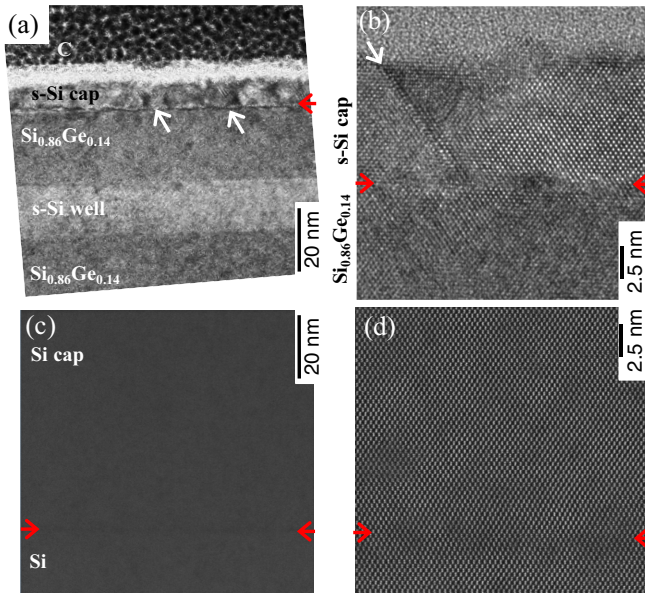


FIG. 3. Cross-sectional TEM of atomic-layer doped structures: (a) s-Si/P/Si_{0.86}Ge_{0.14}, (b) detail of the s-Si/P/Si_{0.86}Ge_{0.14} interfaces and crystal, (c) Si:P doped structure grown under similar conditions, and (d) interfacial and crystal detail of the Si:P structure. Red arrows point to the P layer and white arrows point to stacking faults in the epitaxial s-Si cap.

P sheet density $\sim 1.2 \times 10^{14} \text{ cm}^{-2}$. This is very similar to the FWHM = 3 nm peaked P sheet density $1.3 \times 10^{14} \text{ cm}^{-2}$, measured in our Si:P structure [Fig. 4(b)] and consistent with results reported previously [37]. It is likely that the difference between the P sheet density and the Hall e density is due to SIMS instrumental error. Quantifying the density of atomically thin doping layers is challenging owing to competing tradeoffs to attain adequate vertical spatial resolution and simultaneous quantitative accuracy. The apparent 3-nm-spread of the dopant peak is due to the limited SIMS depth resolution ($\sim 4 \text{ nm/decade}$ of P density). The SiGe epitaxial cap has substantial backgrounds of N, C, and O contamination, which are somewhat higher than in the bulk Si:P structure, indicating that the lower-temperature process leaves more

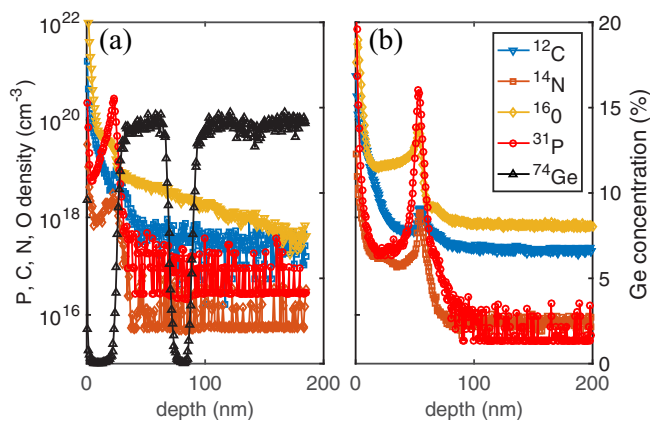


FIG. 4. (a) Post-growth SIMS of the complete s-Si/P/Si_{0.86}Ge_{0.14}. (b) SIMS of Si:P material grown under similar conditions.

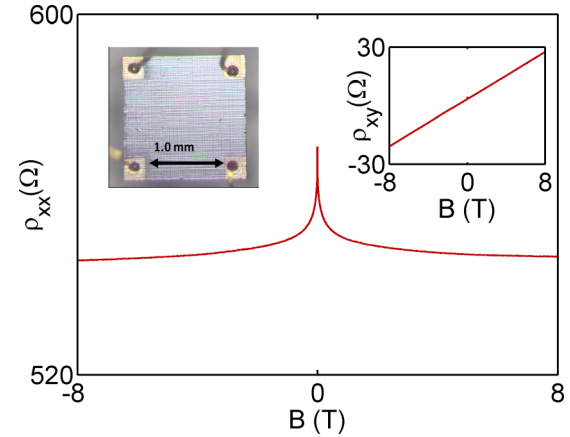


FIG. 5. Longitudinal magnetoresistance and Hall (inset) resistance at $T = 0.3 \text{ K}$ of the atomic-layer doped heterostructure along with a photo of the test device. The aluminum contact pads appear bright gold hue.

residual contamination, which may be the cause of the stacking faults in the s-Si capping layer [47].

III. ELECTRONIC DEVICE CHARACTERIZATION

Electronic figures of merit for the atomic-layer doping are the electron density and mobility. These are measured using a Hall effect device fabricated on a $\sim 1 \times 1 \text{ mm}^2$ die with Al contact pads. Figure 5 inset shows a photograph of the completed device.

Transport measurements are done in a ^3He system with a base temperature of 0.3 K. We use standard lock-in measurement techniques with an excitation current of 100 nA. Hall effect measurements (Fig. 5 inset) yield $R_{\square} = 570 \pm 30 \Omega$, and an electron density $n_e = 2.1 \pm 0.1 \times 10^{14} \text{ cm}^{-2}$ and mobility $\mu_e = 52 \pm 3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. These values are similar to those reported for atomic-layer doping in Si ($1.7\text{--}2.4 \times 10^{14} \text{ cm}^{-2}$ and $\mu_e = 30\text{--}120 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$), and Ge ($6 \times 10^{13} \text{ cm}^{-2}$, $30 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) [5,24,37]. These values of mobility also compare well with the calculations of Hwang and Das Sarma describing transport in the donor layers entirely in a semiclassical Drude model [48].

Magnetotransport measurements (Fig. 5) provide insight into the character of transport. The data are essentially featureless except for a 4% bump at $B = 0 \text{ T}$, indicative of weak localization which is typical of transport via atomic-layer doping in Si and Ge [24,37]. The values of n_e , μ_e , and the absence of any Shubnikov–de Haas oscillations indicate that electrons move via the atomic-layer doping, and do not significantly populate the nearby higher-mobility buried Si well (20–50 nm distant).

IV. SELF-CONSISTENT SIMULATIONS

To determine whether electron transport via the 2D phosphorus sheet is physically consistent with the device geometry, we performed self-consistent simulations of the one-dimensional semiconductor heterostructure (along the growth direction). We use the standard predictor-corrector approach to achieve rapidly convergent calculations [49], assuming

zero-field boundary condition at the bottom of the stack, corresponding to charge neutrality deep in the substrate. Since the conduction band is not pinned at the top of the stack (either by a top gate or a high density of surface traps), the appropriate boundary condition is ambiguous. Hence, in our simulations we checked a wide range of Dirichlet boundary conditions at the top to ensure that our conclusions do not rely on particular boundary conditions. Throughout, we work within the Hartree approximation at 4 K, and neglect exchange and correlation effects.

The nontrivial part of the calculation is the proper inclusion of the P-doped layer, which is sufficiently highly doped that typical models of donor neutralization [50] no longer directly apply. Instead, we explicitly include the Γ_1 , Γ_2 , and four degenerate Δ bands in the 2D density of states model introduced in Ref. [51], with the locations of the P-layer bands specified by Ref. [52]. As pointed out in Ref. [51], the simple density of states model alone introduces an inconsistency, in that the Fermi level required to impose charge neutrality is predicted to be (unphysically) above the conduction band edge for $\frac{1}{4}$ monolayer P doping. To achieve the Fermi level location of 130 meV below the conduction band edge, as reported from density functional theory (DFT) [51], we adopt a uniform multiplicative correction to the density of states of the three P-layer bands. We find they need to be suppressed by ~ 0.65 . The P layer is smeared out over a 2-nm vertical window, and its bands are included alongside conduction band accumulation in our self-consistent simulations.

In Fig. 6, we show results of our calculations. As can be anticipated from the experiment, the conduction band is effectively pinned by the P layer, which is incredibly metallic. Since the charge-neutrality condition imposes that the conduction band is 130 meV above the Fermi level at the P layer, essentially no accumulation occurs in the quantum well, which must dip below the Fermi level to form a channel. As we discussed above, the top interface is not directly controlled, so we confirm that a wide variety of boundary conditions do not change the core results. While certain plausible boundary conditions can achieve modest accumulation in the silicon cap, we cannot form a channel in the quantum well.

These results indicate that, given our device geometry, we would expect electron occupation in the 2D phosphorus sheet, but not in the quantum well. Hence, our device simulations provide a consistent picture with our electrical transport measurements.

V. SUMMARY

In summary, we have demonstrated a recipe for low-temperature surface preparation and atomic-layer doping of SiGe heterostructures that is compatible with atomic-precision donor nanofabrication, while preserving the strained-layer structure and elastic state. SIMS shows the atomic-layer doping has $N_D \sim 1.2 \times 10^{14} \text{ cm}^{-2}$ with a FWHM = 3 nm, while Hall effect measurements at $T = 0.3 \text{ K}$ show that the structure has a sheet resistance $R_{\square} = 570 \pm 30 \ \Omega$, electron density $n_e = 2.1 \pm 0.1 \times 10^{14} \text{ cm}^{-2}$, and mobility $\mu_e = 52 \pm 3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. These results indicate that electrons stay localized to the donors owing to the conduction band offset of the s-Si cap with respect to the SiGe. By contrast, to achieve

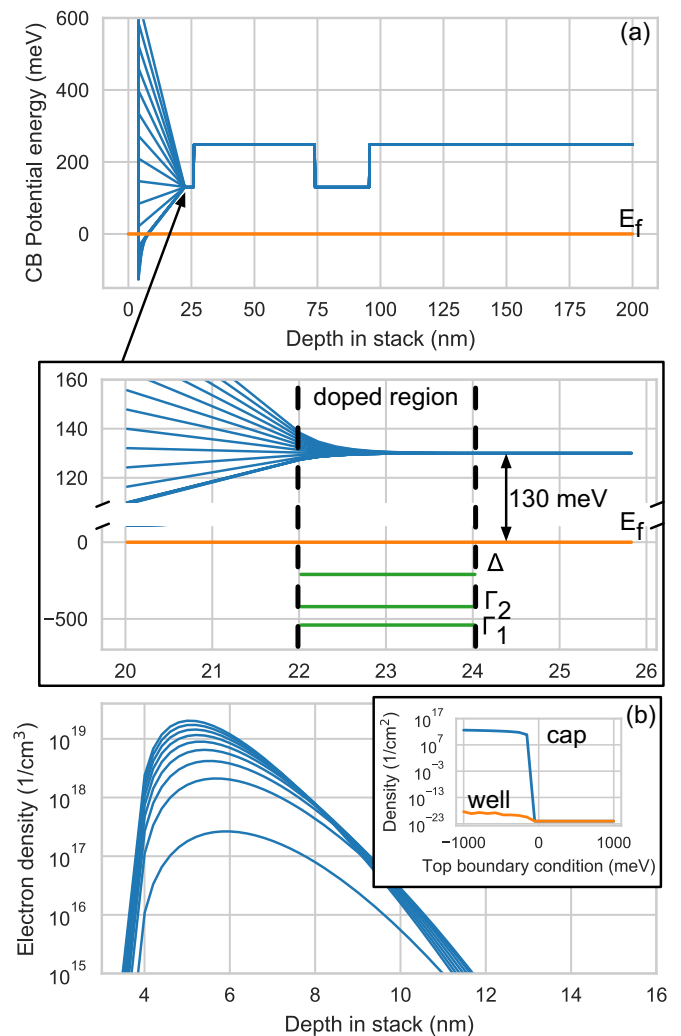


FIG. 6. Self-consistent simulations of the atomically doped structure. (a) Conduction band edge results from self-consistent Schrödinger-Poisson simulations. Since the boundary condition at the top of the stack is uncertain, we computed results for many values, ranging between $\pm 1 \text{ eV}$. We found that the pinning due to the P layer was sufficiently strong that surface effects (either via gating or oxide charge) would have a negligible effect on the quantum well below. The conduction band at the P layer is pinned 130 meV above the conduction band edge, which is the charge-neutrality condition established in Ref. [52]. (b) Excess electron density (electrons neutralizing the P layer are not shown) accumulation in the heterostructure stack for the various top boundary conditions used. The inset shows the integrated 2D sheet density of excess electrons in the cap layer and the quantum well, respectively, as a function of top boundary condition. This shows that, although we can accumulate electrons in the cap layer, we never expect accumulation within the quantum well. Zero density was set to $1 \times 10^{-23} \text{ cm}^{-2}$ for plotting on a semilog scale.

spontaneous electron transfer from the donors to the well would require capping the donor layer with SiGe, as in Fig. 1(d). Also, while we have demonstrated atomic-layer doping on the relaxed $\text{Si}_{0.86}\text{Ge}_{0.14}$ surface, the procedure will work equally well on s-Si surfaces formed by epitaxy on the relaxed SiGe structure [38,39]. This is an enabling step toward engineering structures that simultaneously utilize atomic-precision donor nanofabrication and SiGe strained-layer engineering. Our

proof of concept is on a complete heterostructure with a preprocess peak mobility $\mu_e = 7 \times 10^5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, although the procedure will work equally on a commercially available relaxed SiGe virtual substrate. The next step is to demonstrate a complete atomic-precision nanofabrication process using STM hydrogen depassivation lithography to template donor incorporation laterally in plane to form 3D atomically abrupt doped nanostructures [1–3].

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