Near-thermal limit gating in heavily doped III-V semiconductor nanowires using polymer electrolytes

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Doping is a common route to reducing nanowire transistor on-resistance but it has limits. A high doping level gives significant loss in gate performance and ultimately complete gate failure. We show that electrolyte gating remains effective even when the Be doping in our GaAs nanowires is so high that traditional metal-oxide gates fail. In this regime we obtain a combination of subthreshold swing and contact resistance that surpasses the best existing *p*-type nanowire metal-oxide semiconductor field-effect transistors (MOSFETs). Our subthreshold swing of 75 mV/dec is within 25% of the room-temperature thermal limit and comparable with *n*-InP and *n*-GaAs nanowire MOSFETs. Our results open a new path to extending the performance and application of nanowire transistors, and motivate further work on improved solid electrolytes for nanoscale device applications.

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I. INTRODUCTION

Complementary metal-oxide semiconductor (CMOS) technology is central to modern integrated circuits. The technology combines *p*-type and *n*-type metal-oxide semiconductor field-effect transistors (MOSFETs), exploiting the opposing charge carrier polarity and channel current versus gate voltage characteristics to achieve low power logic. Miniaturization drove the development of nanowire CMOS featuring III-V nanowires integrated on Si toward high performance at low cost [1–3]. This is underpinned by broader research aimed at improved gating in III-V Nanowire Field-Effect Transistors (NWFETs) seeking steeper subthreshold slope and lower parasitic resistance for reduced operating voltage and enhanced energy efficiency [4]. Progress has been strong for *n*-type III-V NWFETs with near-thermal limit subthreshold slopes obtained for InP [5], InGaAs [6], and AlGaAs/GaAs [7]. Integration of *n*-type III-V NWFETs on Si is well established [6,8] with GHz operation demonstrated [9]. Most of these devices achieve their excellent gate channel coupling by employing high-κ dielectrics such as HfO_2.

The development of *p*-type III-V NWFETs has lagged behind [1]. This is caused by several key challenges for *p*-type devices including lower intrinsic carrier mobility and difficulties in growth, doping, and fabrication of high-quality ohmic contacts and gates. Hence a III-V nanowire CMOS circuit typically features *p*-type transistors, which are far less ideal than their *n*-type counterparts [5,10,11]. Here we present polymer-electrolyte-gated Be-doped p^+-GaAs NWFETs with near-thermal limit gating that point out a path to filling this significant performance gap. Our p^+ doping ensures low contact resistance and high channel conductivity while the electrolyte gate provides subthreshold slope ~75 mV/dec, on-off ratio of order 10^4, and low hysteresis. This is despite the doping level being so high that traditional metal-oxide gate structures fail completely, i.e., they give no gate modulation or very poor on-off ratios (<3) [12]. In particular, even top gates with HfO_2 dielectric—similar to those that facilitate near thermal limit switching in, e.g., InP [5]—do not provide effective transistor action.

Our polymer-electrolyte (PE) gate consists of an electron-beam patterned polymer gel, e.g., polyethylene oxide, spanning the gap between a metal electrode and the nanowire [13]. The gel absorbs water providing an environment for mobile ions, either H^+/OH^- from dissociated H_2O, or added salt, e.g., $LiClO_4$ [14]. Gating occurs by electric field driven ion migration with gate charge forming a concentric ion layer within ~1 nm of the nanowire surface [15]. The resulting strong gating has seen electrolyte gating become a well-known approach to improved performance in materials ranging from organic semiconductors to chalcogenides [16]. Electrolyte gating also provides a simpler route to achieving concentric gating action for nanowire devices [13,17]. The key result of this work is a demonstration that electrolyte-gated nanowire transistors remain functional even in the limit where the doping density becomes sufficiently high that traditional gating approaches fail. This is useful because heavy doping provides a path to reduced contact and channel resistance. Additionally, PE gates are far simpler to produce than traditional metal-oxide wrap-gate structures [18–21] and utilize an intrinsically biocompatible material [22]. Nanopatterned PE gates have been used in applications from enacting external ionic doping of quantum devices [17,23] to ionic-to-electronic signal transduction [14]. Here we extend this to include improved *p*-type NWFETs for room-temperature nanowire complementary circuits.

II. METHODS

Our self-catalyzed [24] GaAs nanowires were grown by molecular beam epitaxy on (111)Si [25]. The undoped core

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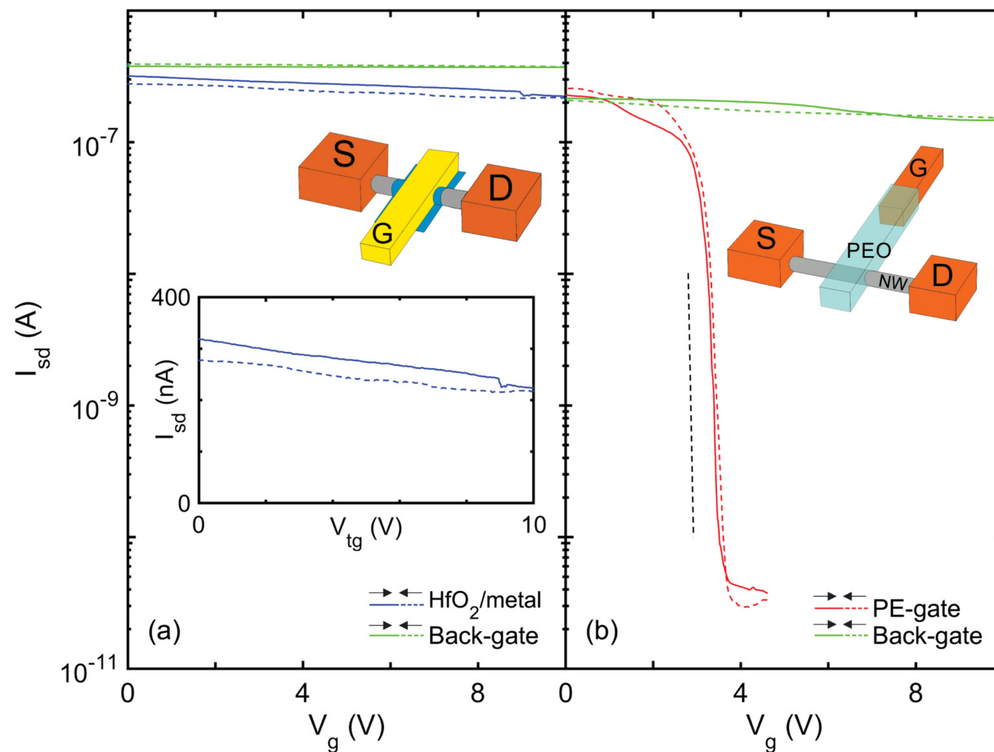

FIG. 1. Source-drain current I_{sd} vs gate voltage V_g for (a) metal-oxide top-gated and (b) PE-gated NWFETs. Both feature high Be acceptor concentration $N_A = 1.5 \times 10^{19}$ cm^{-3} p^+-GaAs. $V_{sd} = 100$ mV for all traces with solid (dashed) lines showing sweeps toward more positive (negative) V_g. The blue and green traces in (a) are the metal top gate and n^+-Si back-gates, respectively. The blue traces are offset downward by 100 nA for clarity. The green and red traces in (b) are for the n^+-Si back gate and PE gate respectively. The dashed black line in (b) indicates the thermal limit subthreshold swing 60 mV/dec. The inset to (a) shows the metal-oxide top-gated data from (a) on a linear scale to further demonstrate that weak gate modulation and no clear switching is observed. Corresponding device structures are inset to (a) and (b); S = source, D = drain, G = gate electrode, NW = nanowire, PEO = polyethylene oxide. The typical gate electrode G to nanowire gap is 2 μm for the device in (b). All data were obtained at room temperature.

was grown at 630°C using As_4 and a V/III flux ratio of 60 for 30–45 min. The Be-doped shell was grown at 465°C using As_2 and a V/III ratio of 150 for 30 min giving nanowires with typical diameters of 150–200 nm and length 5–7 μm. The nanowires should be pure zincblende crystal phase throughout. There will possibly be some short wurtzite segments at the ends [26]; these will be buried under the contacts. We focus here on nanowires with shell acceptor densities of $N_A = 1.5 \times 10^{19}$ cm^{-3}, the highest doping density from our earlier work on all-inorganic p-GaAs NWFETs [12]. Nanowires were transferred to a prepatterned HfO_2/SiO_2-coated n^+-Si substrate for device fabrication with two architectures used: (a) a traditional metal-oxide Ω-gate structure [Fig. 1(a) inset] and (b) a PE gate [Fig. 1(b) inset]. Fabrication for both began with the contacts. These were defined by electron-beam lithography (EBL) and thermal evaporation of 200 nm of 1% Be in Au alloy (ACI Alloys). GaAs native oxide at the contact interfaces was removed by a 30 s etch in 10% HCl solution. The metal-oxide gate was produced in two steps. First a patterned 10-nm layer of the high-κ insulator HfO_2 was defined by EBL and atomic layer deposition (ALD). An overlapping 20/180 nm Ti/Au gate electrode was then formed in a separate round of EBL and metal deposition.

For PE-gated devices, the Ti/Au gate electrode terminated 2 μm from the nanowire and was defined by EBL and thermal evaporation [13]. Patterning of the PE was the final step. Two hundred mg of polyethylene oxide (molecular weight 200k—Aldrich) was dissolved in 10 mL of methanol by sonication for 30 min. Addition of $LiClO_4$ is optional and provides no significant performance enhancement in our NWFETs [14]. For all of the PE gates used in this study, the polyethylene oxide is doped with $LiClO_4$ with a 1:10 $LiClO_4$:PEO ratio. The solution was left to stand overnight with the supernatant spin-coated onto the device at 3000 rpm for 60 s. The device was baked at 90°C for 30 min to remove residual methanol. Polyethylene oxide acts as a positive EBL resist [13] and was directly patterned by EBL with beam energy 7 keV and dose 300 μC/cm^2. Development in H_2O removed unexposed regions giving nanoscale PE strips between the gate electrode and nanowire [13]. Electrical measurements were performed at room temperature in ambient. Yokogawa GS200 voltage sources supplied the source-drain voltage V_{sd} and gate voltage V_g for both PE and metal-oxide gates. We measured the drain current I_d using a Keithley 6517A electrometer.

III. RESULTS

A key challenge for p-GaAs NWFETs is obtaining low contact resistance and strong gate performance simultaneously. Low-resistance contacts to GaAs nanowires are difficult because surface states pin the surface Fermi energy midgap,

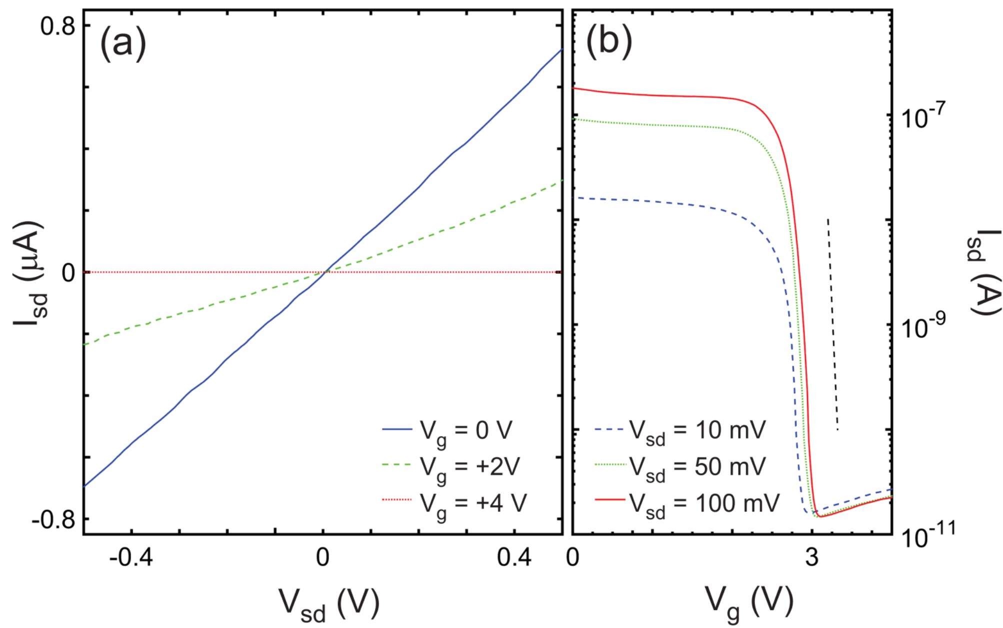

FIG. 2. (a) Source-drain current I_{sd} vs source-drain voltage V_{sd} for the PE-gated NWFET with $V_g = 0$ V (blue solid), +2 V (green dashed), and +4 V (red dotted) demonstrating the ohmic contact performance obtained via high acceptor density. (b) I_{sd} vs PE gate voltage V_g for $V_{sd} = 10$ mV (blue dashed), 50 mV (green dotted) and 100 mV (red solid) demonstrating slight dependence of threshold voltage on V_{sd}. Corresponding threshold voltage values are 2.75, 2.80, and 2.90 V, respectively. The dashed black line in (b) indicates the thermal limit subthreshold swing of 60 mV/dec.

unlike for InAs, where the surface Fermi energy is pinned at the conduction band edge. This leads to a significant Schottky barrier for metal-GaAs interfaces. Ohmic contacts to GaAs typically use an annealed alloy of a noble metal and a diffusive dopant [27], e.g., AuGe for n-type [7] and AuBe for p-type [12]. The idea is that the diffusive dopant causes the semiconductor local to the metal contact to become very highly doped. This makes the Schottky barrier depletion region very narrow, raising the electron tunneling probability and giving a linear I-V characteristic for the contact. This can be assisted by doping the semiconductor local to the contact by other means, e.g., by ion implantation [28] or during growth [25,29].

Our GaAs nanowires are readily doped p-type with Be, which incorporates preferentially via the nanowire side facets enabling structures with an undoped core and Be-doped shell [25]. A Be-doped shell provides an ideal interface for AuBe contacts with narrow Schottky barriers and thereby p-type NWFETs with low-resistance ohmic contacts. We recently showed that contact annealing is detrimental in this case likely because the Be diffusion rate within the nanowire exceeds the Be out-diffusion rate from the alloy, reducing the net doping level at the contact interface [12]. This provides a strong incentive to compensate by maximizing shell doping density to ensure the Schottky barrier depletion width remains minimized. However, this approach brings a second problem: severe loss in gate performance. Figure 1(a) shows I_{sd} versus V_g for a p-GaAs nanowire MOSFET with high shell acceptor density $N_A = 1.5 \times 10^{19}$ cm^{-3}. The metal-oxide Ω gate (blue trace) modulates the current by a factor of 2 at best despite the use of high-κ dielectric. The data are presented on a focused linear I_{sd} scale in the inset to Fig. 1(a) to conclusively demonstrate this. To prove that this is not due to a limited gate voltage range, we take a separate device to catastrophic gate dielectric breakdown without switching being observed. The data for this are shown in the Supplemental Material [30]. We obtain similar lack of gate efficacy from the n^+-Si back gate (green trace). Poor gating at the high free carrier density arising from degenerate doping is expected; it is exactly why FETs do not have metal channels. An obvious potential solution is to keep the shell doping density high near the contacts yet lower near the gate. Unfortunately, it is not clear how to achieve nanowire shell growth with controlled axial doping variation. Ion implantation is an alternative but one that causes significant damage to the nanowire [28]. Thus for our p-GaAs nanowire MOSFETs we are trapped in an unfortunate trade-off between contact resistance and gate performance governed by shell doping density. Our key finding in this paper is that electrolyte gating offers a path to obtaining low contact resistance and good gate performance simultaneously.

Figure 1(b) shows the performance of the PE gate (red trace) for a p-GaAs nanowire with $N_A = 1.5 \times 10^{19}$ cm^{-3} from the same growth. The green trace shows the performance for the n^+-Si back gate to confirm that conventional gating still fails and there is no unanticipated difference between the nanowires in Figs. 1(a) and 1(b). The PE gate gives very strong gating with subthreshold swing $S \sim 75 \pm 15$ mV/dec and on-off ratio near 10^4. The subthreshold swing is comparable to the best obtained for n-InP (68 mV/dec) [5] and n-GaAs (70 mV/dec) [7] nanowire MOSFETs and within 25% of the room-temperature thermal limit (60 mV/dec). We obtain on-current $I_{on} \sim 0.25\mu$A at $V_{sd} = 100$ mV corresponding to 400 kΩ channel resistance, with contact resistance $R_{on} \sim$ 30 kΩ previously measured for this doping level [12]. Similar performance is obtained from separate nominally identical devices as demonstrated by the data in Fig. 2. Figure 2(a) shows I_{sd} versus V_{sd} for a PE-gated device at several V_g

demonstrating good linear contact performance throughout the entire PE-gate range. Saturation is not observed for $V_{sd} <$ 2.5 V in these high N_A nanowires, as expected given their high doping density. A significant aspect of Fig. 1(b) is the low hysteresis, particularly in the subthreshold regime, which we attribute to three factors. First, growth on (111)Si gives {110} side facets for which surface states largely reside outside the band gap [31,32]. Second, there is no added oxide beyond the thin GaAs native oxide that grows upon air exposure. Third, the high density of free carriers in the shell and mobile ions in the PE strongly screen the residual surface state/oxide trapping effects. As with the p-GaAs nanowire MOSFETs, the precise performance is tunable via N_A; for example, at lower $N_A = 1 \times 10^{18}$ cm^{-3} we see slightly poorer subthreshold swing (95 mV/dec) and higher $R_{on} \sim 1.4$ MΩ but improved on-off ratio $\sim 10^6$, lower threshold voltage ($\sim + 2$V), and no appreciable worsening in hysteresis. We also find that the threshold voltage is slightly influenced by V_{sd} as shown in Fig. 2(b). We do not expect significant short-channel effects in our devices, and accordingly, the threshold shift direction is opposite that expected for drain-induced barrier lowering (DIBL). The threshold shift direction is instead indicative of the increased I_{sd} that naturally follows increased V_{sd} at fixed V_g, consistent with other nanowire transistors [5,10]. Finally, we comment briefly on the field-effect mobility for our device. We can obtain the field-effect mobility $\mu_{FE} = g_m L^2/C V_{ds}$ with transconductance $g_m = \partial I_{ds}/\partial V_g$, channel length L, and gate capacitance C. The latter is difficult to accurately estimate for an electrolyte gate and should be considered an order of magnitude estimate at best. Here we estimate the capacitance of the electrical double layer at the PE/NW interface using a concentric cylinder formula $C = \frac{2\pi\epsilon_r\epsilon_0 L}{\ln(1+t/r)}$ where ϵ_0 is the permittivity of free space, t is the electrical double layer thickness, and r is the nanowire radius. We measured $r = 72.5$ nm by scanning electron microscopy, and $L = 1.5$ μm, which is the length of nanowire covered by the PE gate, by optical microscopy. We take typical values of $\epsilon_r = 20$ and $t = 1$ nm for a polyethylene oxide formulation similar to ours from Takeya *et al.* [33] and thereby obtain $C \approx 0.12$ pF. This gives a capacitance per area of 17 μF/cm^2, which is consistent with the 10 μF/cm^2 typical of polyethylene oxide-based polymer electrolytes [15]. With a measured transconductance $g_m = 175$ nS at $V_{sd} = 100$ mV for the data in Fig. 1(b), we obtain $\mu_{FE} \approx$ 0.3 cm^2/Vs. The field-effect mobility is low compared to, e.g., InAs nanowire transistors, but this is not unexpected given the much higher effective mass $m^* \sim 0.35 m_0$ for one-dimensional confined holes in GaAs [34] (cf. $m^* \sim 0.023 m_0$ for electrons in InAs nanowires [35]) and the fact that conduction occurs largely via a thin, heavily doped shell in our devices.

IV. DISCUSSION

We now put our results into context with other p-type III-V NWFETs. The most promising alternate III-V is GaSb, which is intrinsically p-type even when undoped due to native antisite defects [36,37]. Dey *et al.* [10] recently reported on single InAs/GaSb nanowire CMOS inverters with a GaSb p-MOSFET subthreshold swing $S = 400$ mV/dec, on-off ratio $\sim 10^{1.8}$, and on-resistance $R_{on} > 1.2$ MΩ. Our device in Fig. 1(b) surpasses all three performance metrics. The on-resistance for GaSb NWFETs can be improved by Zn doping [38] but this compromises on subthreshold swing, as for GaAs p-MOSFETs [12]. Babadi *et al.* [38] obtain $R_{on} \sim$ 26 kΩ with $S \sim 820$ mV/dec for moderate Zn doping and short channel length $L = 200$ nm but lose pinch-off for longer channels and/or higher doping levels. The one aspect where our PE-gated GaAs NWFETs fall behind is ac response. The InAs/GaSb CMOS inverter of Dey *et al.* shows square-wave fidelity loss at $\sim$10 kHz [10]. We currently experience fidelity loss at $\sim$10 Hz due to the limited ionic conductivity of our PE, but our estimates suggest $\sim$1 kHz is possible with some engineering of the PE and device design [14], while MHz operation of other PE-gated devices is well established [15]. A key limitation of polyethylene oxide-based electrolyte gates is their strong affinity for water and their hygroscopic nature, which makes their performance sensitive to ambient humidity and hydration accumulated during processing [14]. We expect improved performance to be obtained by a shift to other electrolyte-gate materials (see, e.g., discussion in Kim *et al.* [15]), as well as through further engineering of N_A and the device architecture; this will be the subject of future work.

Briefly considering other p-type III-Vs, p-InAs gives ambipolar behavior because conduction via the subsurface electron layer from surface Fermi-level pinning competes with hole conduction in the core [39]. This competition leads to poor off-current and subthreshold slope performance albeit with low contact resistance at room temperature [39]. p-InP is likewise ambipolar. The higher band gap of InP aids with off-current suppression giving on-off ratio $>10^2$ with $S \sim 220$ mV/dec but low $I_{on} < 10$ pA [5]. In contrast, InSb has the smallest band gap and gives the poorest performance in the role of room-temperature p-NWFET [40].

V. CONCLUSION

We have shown that electrolyte gating remains effective in nanowire transistors where the doping level is sufficiently high that traditional metal-oxide gate formulations fail completely. We exploit this to obtain p-GaAs nanowire transistors that surpass other III-V p-type nanowire MOSFETs on a combination of three performance metrics: subthreshold swing, on-off ratio, and on-resistance. The latter is achieved via the high doping density which necessitates electrolyte gating for functional gating. We obtain a subthreshold swing of 75 ± 15 mV/dec, within 25% of the room-temperature thermal limit, and comparable with the best n-type nanowire MOSFETs. Additionally, our gate structures show low hysteresis in the subthreshold regime, are easier to fabricate than metal-oxide gate structures, and feature an inherently biocompatible material. Our results point an interesting path to extending the performance and application of nanowire transistors, and motivate further work on improved electrolyte materials for nanoscale device and bioelectronics applications.

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