Nonvolatile Gate Effect in a Ferroelectric-Semiconductor Quantum Well

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Field effect transistors with ferroelectric gates would make ideal rewritable nonvolatile memories were it not for the severe problems in integrating the ferroelectric oxide directly on the semiconductor channel. We propose a powerful way to avoid these problems using a gate material that is ferroelectric and semiconducting simultaneously. First, ferroelectricity in semiconductor (Cd,Zn)Te films is proven and studied using modified piezoforce scanning probe microscopy. Then, a rewritable field effect device is demonstrated by local poling of the (Cd,Zn)Te layer of a (Cd, Zn)Te/CdTe quantum well, provoking a reversible, nonvolatile change in the resistance of the 2D electron gas. The results point to a potential new family of nanoscale one-transistor memories.

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Ferroelectric materials possess spontaneous polarization that can be reversed by an external electric field. Among other applications, this property is employed in field effect transistors with ferroelectric gate (FeFET) [1,2]. These devices would make ideal memories offering random access, high speed, low power, nondestructive reading, and nonvolatility were it not for the severe problems in integrating the ferroelectric oxide directly on the semiconductor channel [3]. This incompatibility can be avoided if the gate were a nonoxide ferroelectric-semiconductor compatible with silicon technology. Here we focus our attention on such a material, cadmium zinc telluride (Cd,Zn)Te.

Ferroelectricity in (Cd,Zn)Te single crystals with 4% Zn was reported in 1989 by Weil *et al.* [4] based on an observation of ferroelectric hysteresis, supported by dielectric anomaly. More recently, Fu *et al.* [5] confirmed the hysteretic behavior of the spontaneous polarization and conduction in this material. However, understanding ferroelectricity in (Cd,Zn)Te and other related semiconductors is limited; ferroelectricity is forbidden in the zinc-blend structure adopted by pure CdTe. A ferroelectric transition in (Cd,Zn)Te implies that Zn doping provokes a lattice distortion, lowering the symmetry. Most of the polarization hysteresis measurements reported in the literature have been performed on compositions with low Zn content, such as $Cd_{0.96}Zn_{0.04}Te$, but no structural distortions have been reported for such low Zn concentrations. A rhombohedral structure had been found in more heavily Zn-doped crystals [6], though in recent diffraction studies employing synchrotron radiation, crystals of $Cd_{0.7}Zn_{0.3}Te$ revealed an undistorted zinc-blend structure [7].

Polarization hysteresis is the most significant evidence of ferroelectricity in (Cd,Zn)Te reported so far. However, the shape of the (Cd,Zn)Te hysteresis loops are typically characterized by widened or even rounded tips indicating a substantial conduction contribution. The relatively small spontaneous polarization reported for (Cd,Zn)Te ($\approx 1\ \mu C/cm^2$ or less) that can often be hardly discriminated from conductivity effects adds to the difficulties. An observation of a hysteretic piezoelectric response could enhance the confidence in the existence of ferroelectricity in (Cd,Zn)Te. Such a study is even more important for the (Cd,Zn)Te thin films, where ferroelectricity has never been demonstrated so far. The ferroelectric properties of thin films commonly differ from the bulk material due to, for example, strain caused by the lattice mismatch [8].

Here we start by an investigation of ferroelectricity in (Cd,Zn)Te single crystals and thin films by piezoforce scanning probe microscopy (piezo-SPM). Unlike the traditional polarization hysteresis approach, this technique measures the mechanical displacement instead of the switching charge and hence is less influenced by conduction artifacts that are especially problematic in weakly ferroelectric semiconducting materials. We have modified this technique to specifically adopt the detection method for semiconductors, and for the first time demonstrated ferroelectricity in (Cd,Zn)Te thin films and in (Cd, Zn)Te/CdTe heterostructure. Further, we demonstrate reversible nonvolatile gate effect associated with ferroelectricity in a (Cd, Zn)Te/CdTe quantum well.

The (111)-oriented $Cd_{0.94}Zn_{0.04}Te$ bulk single crystal used in this work was a commercial specimen prepared at MTI Corporation [9] using the Bridgman technique. The polycrystalline 1.5 μm ($Cd_{0.97}Zn_{0.03}Te$) film was grown by molecular beam epitaxy on *n*-doped Si substrate. The heterostructure used in this study was grown on 4.5 μm thick $Cd_{0.5}Mg_{0.5}Te$ epitaxial layer deposited on (100) GaAs substrate. The structure consisted of a 15 nm thick CdTe quantum well separated from the doped region by a 20 nm undoped (Cd,Mg)Te spacer. 2D electron gas (2DEG) in the well originates from iodine donors introduced to a 20 nm doped (Cd,Mg)Te region. The quantum

well was capped by a 400 nm thick $Cd_{0.94}Zn_{0.06}Te$ layer. The charge carrier concentration and mobility measured at 77 K were 1.22×10^{11} cm^2 and 2920 cm^2/Vs, respectively.

To study (Cd, Zn)Te/CdTe heterostructures, mesas in the form of Hall bars were defined by chemical etching. In order to explore the effect of the spontaneous polarization on the electron concentration in the 2DEG, a 50×100 μm^2 central area of the mesa was poled using a conductive SPM cantilever [Fig. 1(a)] The resistance was measured at 77 K in order to avoid parallel conduction, while the poling was performed at room temperature by scanning the 50×100 μm region with the SPM tip driven with bias of 15 V as described in Ref. [10].

Piezo-SPM consists of application of a weak ac electric field to the sample and monitoring the converse piezoelectric effect through the detection of amplitude and phase of the local mechanical displacements with atomic force microscope [11]. In the present study this method is implemented in two configurations. In the first, a standard one, the free surface of the sample is scanned with a conductive SPM cantilever driven with ac and in some cases dc voltage. In the second case, the sample is covered with a thin top electrode and the SPM cantilever is used to sense the piezoelectrically induced vibration through the top electrode [12]. The first configuration delivers a better resolution, whereas the second one better eliminates the electrostatic interaction between the SPM tip and sample.

The amplitude of the vertical piezoresponse measured is proportional to the transverse piezoelectric coefficient d_{33}, which is coupled to the normal component of the polarization P:

$$d_{33} = 2Q_{11}\varepsilon\varepsilon_0 P, \quad (1)$$

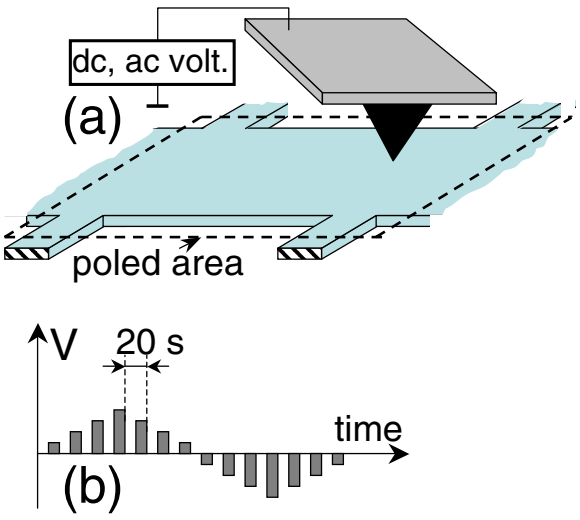

FIG. 1 (color online). (a) Sketch showing the poling or measuring procedure for the Hall bar prepared on (Cd, Zn)Te/CdTe quantum well for study of nonvolatile gate effect. (b) Voltage profile used for d_{33} loop measurements.

where Q_{11}, ε, and ε_0 are the electrostriction coefficient, dielectric constant, and dielectric permittivity of vacuum. For conversion of the amplitude detected by piezo-SPM to d_{33}, a conventional ferroelectric 400 nm $Pb(Zr, Ti)O_3$ film was measured independently using a double beam interferometer [13]. The loop of d_{33} vs dc voltage is an efficient way to characterize hysteretic properties of ferroelectrics presenting essential advantages compared to the standard technique of polarization hysteresis probing. Specifically, piezoloop measurements rely upon the mechanical displacement and not on the switching charge, so the loop is not affected by conduction artifacts.

The piezo-SPM technique is suitable for insulating materials, whereas in semiconductor media it encounters problems. The application of the dc voltage, which is required for the piezoelectric loop measurements, provokes a rather high current flowing through the SPM cantilever. This current may influence considerably the measured signal and mask the piezoelectric response. The technique we propose to overcome this problem employs a special dc voltage profile consisting of a sequence of rectangular pulses with 10 s duration and 10 s interval instead of the routinely used bipolar triangle voltage [Fig. 1(b)]. The amplitude and phase of the local piezoelectric response are detected during the intervals when no dc voltage is applied. This approach results in a more reliable identification of the piezoelectric loop since there is no dc current flowing through the SPM tip and no electrostatic interaction associated with it.

Figures 2(a) and 2(b) display piezoelectric hysteresis loops showing the longitudinal piezoelectric coefficient d_{33} of a (Cd,Zn)Te polycrystalline film [Fig. 2(a)] and a single crystal [Fig. 2(b)]. Both the film and the single crystal show distinct hysteresis loops, whereas for a similar nonferroelectric (Cd,Mg)Te film only a noiselike random response is detectable [Fig. 2(c)]. In all samples, the (Cd,Zn)Te single crystal and thin films alike, the piezoelectric loops were measurable only on submicron-size spots; the major part of the surface did not show any hysteretic behavior. In order to confirm that the measured loops represent the real mechanical displacement rather than electrostatic interaction between the tip and charged surface, the piezoelectric loop has been measured on the same crystal after depositing a top electrode. Both the SPM cantilever and the top electrode were grounded for better elimination of the electrostatic interaction while the ac voltage was applied to the bottom electrode. The piezoelectric ac-displacement measurements through the top electrode resulted in a clearly observed, though deformed, piezoelectric loop [Fig. 2(d)], which confirmed that the effect is related to the real mechanical displacement.

The issue of charge trapping/detrapping has been carefully addressed, to rule out possible artifacts that may result in a hysteretic behavior similar to that observed in our study. The built-in electric field induced by trapped

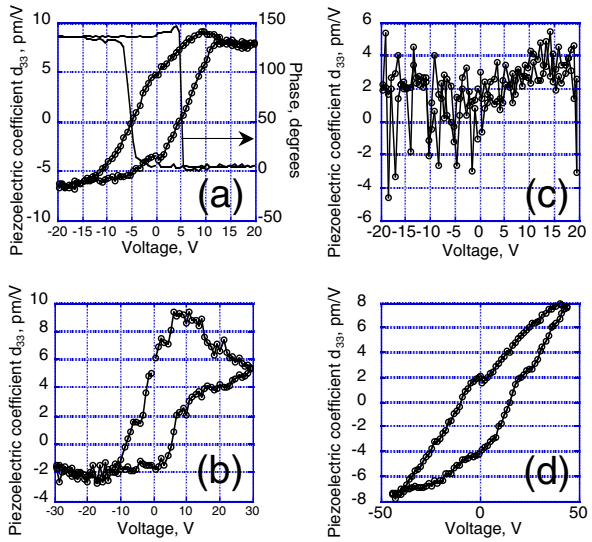

FIG. 2 (color online). Piezoelectric hysteresis loops of longitudinal piezoelectric coefficient d_{33} for the (Cd,Zn)Te polycrystalline film (a), (Cd,Zn)Te single crystal without top electrode (b), (Cd,Mg)Te nonferroelectric film (c), and (Cd,Zn)Te single crystal with top electrode (d). The loops are measured using piezo-SPM on the area of 0.4×0.4 μm.

charges may modify the measured piezolelectric activity, but in our (Cd,Zn)Te samples with a relatively low resistance trapped charge is screened on a rather short time scale. In particular, the (Cd,Zn)Te single crystal had a resistance of less than 10^4 Ω cm, which gives a dielectric relaxation time $\tau = \varepsilon\varepsilon_0/\sigma$, where σ stands for conductivity, residing in the microsecond range. Hence, we adopted for the loop measurements a sequence of voltage pulses separated by 10 s intervals, largely sufficient to screen completely any induced space charge.

In the case of the (Cd,Zn)Te single crystal, the loop is offset, showing a maximum value of positive d_{33} larger than the negative swing [Fig. 2(b)]. This offset arises from the fact that the high temperature paraelectric phase of this material is noncentrosymetric (zinc blend) and possesses piezoelectric activity, albeit nonhysteretic. The net piezoelectric coefficient measured in the ferroelectric phase therefore includes a component d_0 independent of the spontaneous polarization P,

$$d_{33} = d_0 + 2Q_{11}\varepsilon\varepsilon_0 P. \quad (2)$$

Obviously, only the second term in Eq. (2) is reversed by applying the external dc bias, so that the hysteresis loop is offset by d_0 along d_{33}. In the randomly oriented polycrystalline film the response associated with d_0 is averaged, resulting in a smaller offset as seen in Fig. 2(a).

The coercive field of the (Cd,Zn)Te single crystal is much lower than that of the thin film. The 1.5 μm film and 0.4 mm crystal [Figs. 2(a) and 2(b)] are both characterized by similar coercive voltage close to 5 V. A rough estimation shows that the coercive fields in Figs. 2(a) and 2(b) differ by 2 orders of magnitudes at least. Similar differences between coercive field in bulk crystals and thin films are commonly observed in classic ferroelectrics such as barium titanate [14].

To get further insight of the ferroelectricity in (Cd,Zn)Te we explored the ferroelectric domain patterns using piezo-SPM imaging. Surface topography [Fig. 3(a)] and amplitude/phase of local piezoresponse [Figs. 3(b)–3(d)] were collected from 2×2 μm scans using 10531 Hz ac signal with 1.2 V amplitude. The initial image taken without applying any dc bias [Fig. 3(b)] showed a weak response with virtually uniform phase. No change of the phase was observed after applying a negative dc bias to the SPM cantilever, suggesting that the as-deposited film has a preferential polarization oriented from bottom to top. A positive dc bias of 15 V applied to the cantilever while scanning the same 2×2 μm area changes the picture considerably. The image measured at 1 h delay after applying positive voltage shows regions with changed phase seen in the phase map as bright spots [Fig. 3(c)]. These switching regions are also clearly seen in the corresponding amplitude images. A second measurement done after 24 h delay on the same 2×2 μm area shows a similar pattern [Fig. 3(d)] indicating that the switched regions remain stable. This stability strengthen our confidence that the results observed originate from ferroelectric switching, because charge trapping would be expected to show considerable evolution during the 24 h period.

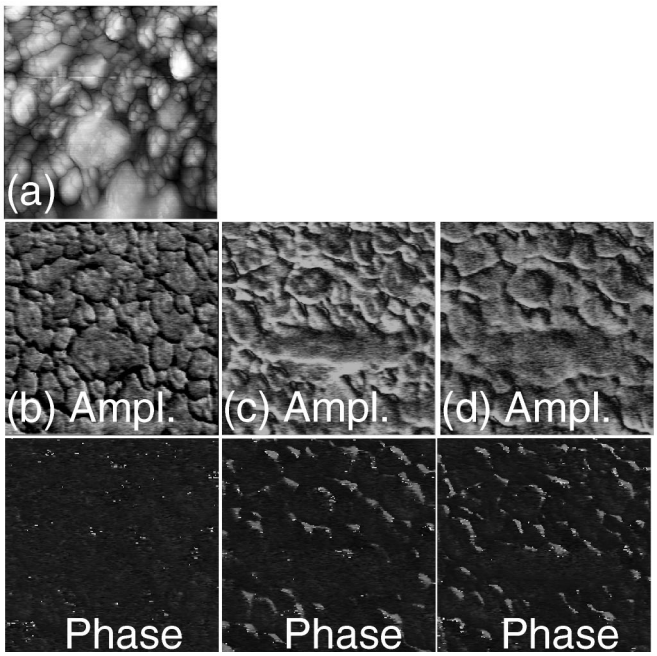

FIG. 3. 2×2 μm topography image (a) and maps of amplitude and phase of local piezoelectric response measured on (Cd,Zn)Te polycrystalline film (b)–(d). Image (b) was taken before poling, image (c) after poling with +15 V at 1 h delay, and image (d) at 24 h delay.

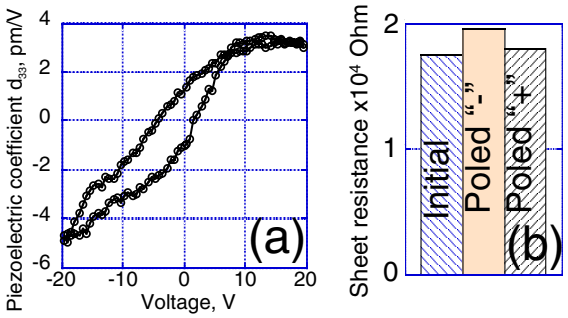

FIG. 4 (color online). (a) Hysteresis loops of longitudinal piezoelectric coefficient d_{33} for the (Cd,Zn)Te epitaxial layer in (Cd, Zn)Te/CdTe quantum well. (b) Sheet resistance of 2DEG measured at 77 K before poling and after poling the (Cd,Zn)Te layer in the quantum well with negative and positive voltage of 15 V.

Attempts to achieve a homogenous switching state by applying a higher voltage were not successful. We speculate that the switching inhomogeneity originates from local variation of Zn concentration.

Local piezoelectric hysteresis loops were also observed on a ZnCdTe/CdTe heterostructure [Fig. 4(a)]. In order to explore the possibility of influencing the 2DEG by switching polarization in the (Cd,Zn)Te layer, the resistance through the well was measured at 77 K before and after room-temperature gate poling [Fig. 4(b)]. Conduction measurements performed after poling the structure with +15 V yielded virtually the same resistance as before poling. On the contrary, the negative voltage corresponding to the 2DEG depletion increased the sheet resistance by 10%–15%. The initial conduction properties were restored nearly completely by poling the sample with positive voltage. This effect was observed on all three tested samples, and the error due to the data scattering did not exceed 3%. The observed switching in 2DEG conduction is interpreted as a partial depletion of carriers in the well as a result of poling the ferroelectric gate. The small magnitude of this effect is related to the nonhomogeneous polarization switching; indeed the 10% magnitude is close to the fraction of the (Cd,Zn)Te gate that can be poled [see Figs. 3(c) and 3(d)]. The physical origin of this nonhomogeneity still needs to be clarified in order to reach better control over the poling process for potential applications.

To summarize, an array of experimental results has been presented to constitute a solid argument in favor of ferroelectricity in (Cd,Zn)Te and show that the spontaneous polarization in both bulk crystals and thin films can be switched by a reasonably low external voltage. A conductivity change in a buried 2DEG upon poling the (Cd,Zn)Te top layer indicates that the built-in ferroelectric gates can be implemented in CdTe-based heterostructures. This may be used in field effect devices and resistive memories [15]. Moreover, the ferroelectric field effect in (Zn, Cd)Te/CdTe heterostructures can be used for 2DEG patterning with nanoscale resolution through polarization domain engineering. The essential advantage of this system is that the ferroelectric layer is an integral part of the heterostructure, relaxing the technological difficulties in integration which have limited the application of ferroelectrics in gate structures [3]. The absence of a buffer layer between the gate and the conductive channel may give an additional important advantage, since it should lead to a smaller depolarization field and a better polarization stability.

(Cd,Zn)Te and similar ferroelectric semiconductors show strong promise and deserve to be investigated as an important group of materials both for the fundamental description of ferroelectricity in distorted zinc-blend semiconductors and for potential applications.

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