# Tunneling Versus Thermionic Emission in One-Dimensional Semiconductors

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This Letter focuses on the role of contacts and the influence of Schottky barriers on the switching in nanotransistors. Specifically, we discuss (i) the mechanism for injection from a three-dimensional metal into a low-dimensional semiconductor, i.e., the competition between thermionic emission and thermally assisted tunneling, (ii) the factors that affect tunneling probability with emphasis on the importance of the effective mass for transistor applications, and (iii) a novel approach that enables determination of barrier presence and its actual height.

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Nanostructures are increasingly relevant for electronics applications. Metallic nanoconductors are explored as interconnects in integrated circuits, and the potential of nanoscale semiconductors as active device components is studied intensively. Of particular interest to the future of nanoelectronics are one-dimensional (1D) components such as nanowires [1] and nanotubes [2]. The reduced phase space for scattering events in those components decreases the probability of backscattering and results in improved transport characteristics. For example, carbon nanotubes were found to be ballistic conductors at room temperature with minimum scattering lengths of a couple of hundred nanometers [3–5].

While nanostructures will undoubtedly become the central components of novel integrated circuits, it is obvious that a connection between these structures and the ''outside world'' must be made. Therefore, interfaces between 1D systems and three-dimensional (3D) contacts will inevitably occur. For a *ballistic conductor*, these interfaces become the dominant source of resistance (see, e.g., [6]). The situation becomes more complex for a *semiconductor/metal* contact.

Here we focus on the details of current injection from a conventional metal into a ballistic, 1D semiconductor in a field-effect transistor (FET) geometry. Depending on the lineup between the metal Fermi level and the conduction/valence band of the semiconductor, a barrier may form at the interface. We discuss the impact of this barrier on the mechanisms of current injection from the metal into the semiconductor, i.e., thermionic emission and thermally assisted tunneling. Specifically, we consider the dependence on sample and material-specific parameters and point out the critical importance of the effective mass of the semiconductor. As an example, we discuss experimental results on carbon nanotube (CNT) and boron-nitride nanotube (BNNT) FETs. Following this, we apply our general observations to quantitatively analyze the barrier height in the case of a CNTFET.

We first consider a nanotransistor that consists of two metal contacts (source and drain) attached to a semiconducting nanostructure. This could be a nanotube, a nanowire, or a long molecule. A third electrode, the gate, is isolated from the semiconducting channel by a dielectric film of thickness $t_{ox}$. The current $I_d$ under source/drain bias depends on the details of the potential profile along the semiconductor. If a Schottky barrier (SB) of arbitrary height exists between the metal and the semiconductor, current can be modulated by the gate by changing the barrier thickness and the tunneling probability through this barrier accordingly. The band bending situation for hole injection into the valence band for two gate voltages is qualitatively depicted in the upper right of Fig. 1. Higher currents are expected for thinner barriers. However, it is well known that tunneling does not play an important role in conventional semiconductor/metal structures at room temperature, especially for high barriers and/or low doping levels. The dominant mechanism for current injection in this case is thermal emission (see, e.g., [7]). Recently it has been proposed that CNTFET operation is entirely based on tunneling [8]. The question

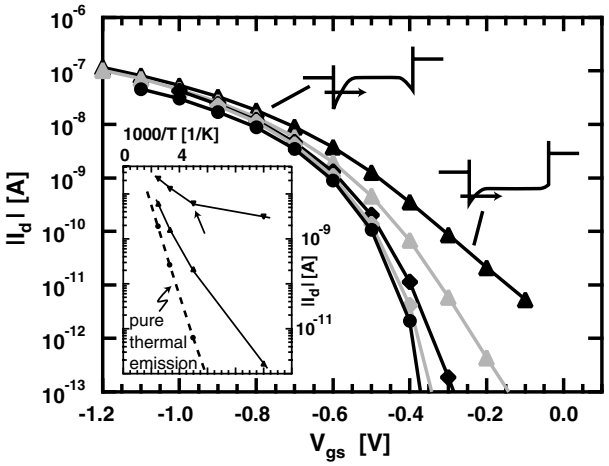


FIG. 1. Simulated $T$-dependent current as a function of $V_{gs}$ for a CNTFET ($t_{ox} = 10$ nm and $\tilde{\Phi}_B = 300$ meV). $T = 300$, 200, 150, 100, and 50 K from top to bottom. The inset shows $I_d(1/T)$ for another simulation with $t_{ox} = 2$ nm and $\tilde{\Phi}_B = 150$ meV at $V_{gs} = -0.2$, $-0.1$, and 0 V (from top to bottom).

  

is: How do these opposite statements relate to each other and what are the key requirements for one or the other mechanism to become dominant for current injection?

To address these questions, we have modeled the transistor geometry introduced above. If only thin semiconducting layers (1 to 5 nm) are considered, the electrostatics of such a system can be described by a modified 1D Poisson equation [9] that effectively reproduces the situation in the transistor if the layer thickness $t_s$ is associated with the size of the nanostructure (e.g., the nanotube diameter). To accurately calculate the charge in and the current through the channel the nonequilibrium Green's function formalism is used [6]. Carriers are injected into the channel from contacts that are considered to be in thermal equilibrium. Scattering in the channel is neglected; i.e., transport through the nanotransistor is considered to be ballistic [5]. A self-consistent solution is achieved by iteratively solving the modified Poisson equation together with the equations for the Green's function [10]. In all simulations, flatband conditions at zero gate voltage $V_{gs}$ and a fixed Schottky barrier height $\tilde{\Phi}_B$ are assumed. Our simulations allow easy assessment of the role of material-specific parameters such as the effective mass $m^*$, tube size, gap energy, etc. on the performance of the nanotransistor under consideration.

Figure 1 shows results of a simulation for a parameter set that describes the electrostatics in a CNTFET ($t_s$ = 1.4 nm) with SBs in both contact regions of $\tilde{\Phi}_B$ = 300 meV for a bias of $-0.5$ V and a $t_{ox} = 10$ nm. The more negative $V_{gs}$, the thinner the barrier for hole injection and the larger the tunneling current through the device. For increasing temperature $T$, the simulated device shows a higher current level for any $V_{gs}$ due to thermal excitation of carriers. But, as will be explained below, a conventional analysis in terms of thermal emission theory does not simply yield the expected Schottky barrier height. Instead, it reveals that the current injection mechanism into 1D semiconductors is often dominated by thermally assisted tunneling.

The inset of Fig. 1 shows Arrhenius-type plots constructed using results of another set of simulations [11] for a number of different gate voltages. The data presented in the inset were calculated for $\tilde{\Phi}_B = 150$ meV and $t_{ox}$ = 2 nm for $V_{gs} = -0.2, -0.1$, and 0 V (from top to bottom). For flatband conditions (dashed curve), a clear linear relation between $\log I_d$ and $1/T$ is observed. This is the thermal emission limit, and the slope of this curve indeed gives a barrier of $\Phi_B = 150$ meV (i.e., exactly the barrier we have used in the simulation) if we use $I_d \sim T^2 \exp(-q\Phi_B/k_B T)$ in our analysis [12]. In other words, for flatband conditions, as assumed for $V_{gs} = 0$, the *only* possibility for carrier injection into the semiconductor is by thermal activation, and we find the expected "true" height of the Schottky barrier. On the other hand, *any* negative gate voltage that results in some band bending at the metal/nanotube interface gives a *smaller* effective barrier $\Phi_B < \tilde{\Phi}_B$ [13]. This is because part of the current through the device now results from tunneling through the barriers. For example, the total current for $V_{gs} = -0.2$ V and $T = 300$ K is $\sim$15 nA, almost 2 orders of magnitude higher than the contribution from thermal emission at the same temperature. While for sufficiently high temperatures (e.g., $T > 200$ K for $V_{gs} = -0.2$ V) $I_d$ still depends exponentially on $T$ (see inset of Fig. 1) allowing the extraction of an effective barrier, thermal assisted tunneling is in fact the dominant mechanism of current injection over the entire temperature range [14]. The obvious change in slope, e.g., for $V_{gs} = -0.2$ V (see arrow) does *not* indicate the transition from thermal emission for high temperatures to tunneling at sufficiently low $T$. It is instead a characteristic of the dependence of the tunneling current on $T$.

The reason for this unexpected behavior is the choice of material and sample specific parameters. The case discussed above is characterized by (a) an ultrathin gate oxide film of $t_{ox} = 2$ nm, (b) a small size of the semiconducting nanostructure of $t_s = 1.4$ nm (e.g., the diameter of a CNT), and (c) a rather small effective mass of $m^* = 0.1 m_0$ ($m_0$ is the free electron mass). Each of these variables has an impact on the tunneling probability. Small values of $t_{ox}$ and $t_s$ ensure a thin barrier at any gate voltage and a smaller $m^*$ results in a larger tunneling probability.

Figure 2 summarizes the dependence of the extracted barrier heights $\Phi_B$ on $V_{gs}$ for different parameter sets. In all simulations $\tilde{\Phi}_B = 150$ meV was used as an input. (i) displays the case discussed in the previous paragraph. At $V_{gs} = 0$, we obtain the expected value of 150 meV. For decreasing $V_{gs}$, the analysis that assumes thermal emission increasingly underestimates the barrier. In fact, for gate voltages of $-0.2$ and $-0.3$ V, even a negative barrier

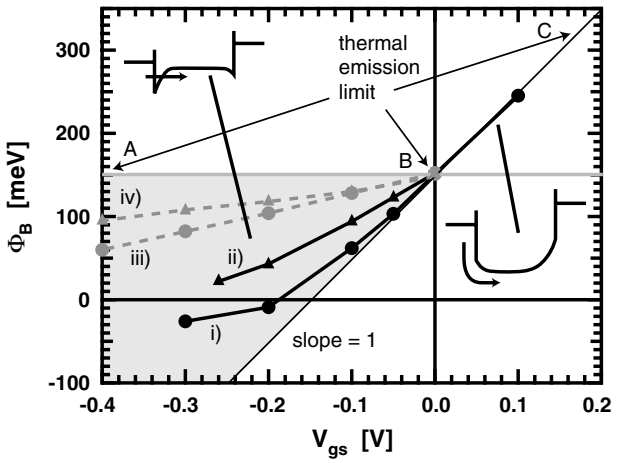


FIG. 2. Barrier height as evaluated assuming thermal emission theory as a function of $V_{gs}$ for various FETs. (i) $m^* = 0.1 m_0$, $t_{ox} = 2$ nm, and $t_s = 1.4$ nm, (ii) $m^* = 1.0 m_0$, $t_{ox} = 2$ nm, and $t_s = 1.4$ nm, (iii) $m^* = 1.0 m_0$, $t_{ox} = 10$ nm, and $t_s = 1.4$ nm, (iv) $m^* = 1.0 m_0$, $t_{ox} = 10$ nm, and $t_s = 5$ nm.

can be extracted. For these $V_{gs}$, the transistor is almost "on," and the case is similar to the one analyzed in [15]. Obviously, the transistor on state is not a good measure of the true SB height. From (i) to (iv) one parameter is changed at a time. In (ii) $m^*$ is increased to $1.0m_0$, then in (iii) $t_{ox}$ is changed from 2 to 10 nm. Finally, in (iv) the size of the nanostructure (e.g., the nanotube diameter) is increased to $t_s = 5$ nm. For the same gate voltage, the extracted barrier height increases from (i) to (iv). Tunneling becomes progressively less important, and the extracted $\Phi_B$ values correspond more closely to the true barrier height of $\tilde{\Phi}_B = 150$ meV. In general, in the limit of a thick gate oxide (or a two terminal device), a large size semiconductor (as in a conventional 3D semiconducting system) or for a large effective mass, one reaches the thermal emission limit indicated in Fig. 2 by the line from A to B to C. There is no dependence of $\Phi_B$ on $V_{gs}$ up to zero, and the true barrier height can be extracted from thermal emission theory for any $V_{gs}$.

Now we consider gate voltages $V_{gs} > 0$. For *all* simulations, changing $V_{gs}$ from 150 to 250 meV results in an increase of the effective barrier by the same amount. The band bending situation for this scenario is sketched in Fig. 2. For positive gate voltages, the valence band bends downward and an effectively higher barrier must be overcome by the holes injected from the left metal contact. Since (1) there is no possibility for tunneling (unlike the situation in the gray octant) and (2) the potential of the valence band is given by $V_{gs}$ if there is no charge on the tube, any change of $V_{gs}$ directly translates into a corresponding change of $\Phi_B$. This is true for *any* set of parameters and thus all simulations coincide for $V_{gs} > 0$. Also note that the line between B and C is the expected result for a conventional 3D semiconductor. Identifying this transition region allows the quantitative determination of the barrier height for any 1D semiconductor/metal contact. The true SB height $\tilde{\Phi}_B$ and the corresponding flatband voltage are obtained when the slope of the $\Phi_B(V_{gs})$ curve becomes equal to one. The entire gray octant shifts up or down depending on the actual Schottky barrier height (given by the point B).

Next, we compare our simulations with experimental results. First, we focus on the importance of $m^*$ on the performance of nanotransistors. Figure 3 shows transistor characteristics for two CNTFETs and a BNNTFET as a function of $V_{gs}$. Details about the sample fabrication can be found elsewhere [16]. While the channel lengths $L$ and gate oxide thicknesses $t_{ox}$ are quite comparable ($L = 300$ nm, $t_{ox} = 5$ and 20 nm for the CNTFETs; $L = 200$ nm, $t_{ox} = 10$ nm for the BNNTFET), the characteristics are significantly different for the two nanotube materials. While the current can be modulated by at least 4 orders of magnitude and can become as large as 1 $\mu$A in the case of the CNTs, the current change is below 1 order of magnitude and does not exceed $\sim$100 pA for the BNNTFET. This is particularly surprising given that in

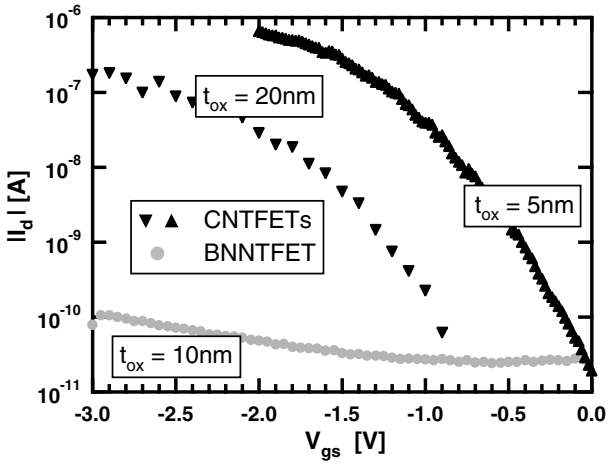


FIG. 3. Experimental transfer characteristics for two CNTFETs and a BNNTFET with similar $t_{ox}$, $L$, and $\tilde{\Phi}_B$. $V_{ds} = -1$ V for all cases.

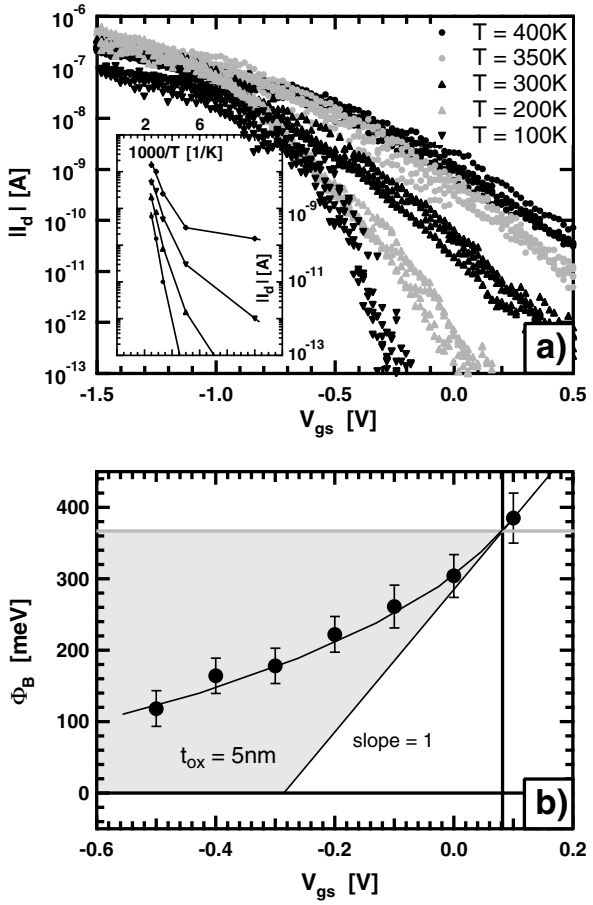


FIG. 4. (a) $T$ dependence for a CNTFET with $t_{ox} = 5$ nm taken at $V_{ds} = -0.5$ V. The inset displays the analysis performed for $V_{gs}$ values of $-0.5$, $-0.3$, $-0.1$, and $+0.1$ V (from the top to bottom). (b) $\Phi_B$ for the same device as a function of $V_{gs}$.

both cases Schottky barriers with heights of ~300 to 400 meV are observed between the metal Fermi level and the valence band of the tube [15,17]. Scattering inside the boron-nitride nanotube may in part be responsible for the smaller current level observed but cannot account for the experimental observation alone since scattering is not expected to alter the slope of $\log I_d(V_{gs})$. However, there is a pronounced difference between the two types of tubes in terms of $m^*$. While one can extract $m^* \sim 0.06 m_0$ for CNTs with a diameter of 1.4 nm from the corresponding dispersion relations $E(\underline{k})$, BNNTs of similar size give $m^* \sim 0.75 m_0$ [17]. According to our previous discussion, tunneling is suppressed with increasing $m^*$ and the current through the device decreases accordingly. Correspondingly, the thermal emission components dominate current injection as previously found [17] and the reason is now understandable within the framework of the discussion in this article. Simulations for BNNTs indicate that the difference in $m^*$ may account for as much as 2 orders of magnitude difference in current in the transistor on state. Thus, small effective masses are desirable in a SB controlled transistor device.

Next, we apply the above analysis to quantitatively evaluate $\Phi_B$ in a CNTFET. To test our approach, we performed measurements on transistors with a 5 nm backside dielectric of silicon dioxide. Titanium contacts were used for all experiments. Figure 4(a) shows the current as a function of $V_{gs}$ for different Ts for a CNTFET with a source/drain separation of $L = 300$ nm [18]. Measurements were repeated 5 times at the same bias with actual data displayed. From these curves we can extract the current level at a given value of $V_{gs}$ and temperature. The inset of Fig. 4(a) shows part of the analysis performed. Note that this inset appears very similar to the one shown in Fig. 1. In particular, a nearly linear relation between $\log I_d$ and $1/T$ can be observed for $V_{gs} = +0.1$ V. Also, there is a clear transition between an exponential dependence of current on inverse temperature to an almost constant current for lower $T$ visible for more negative $V_{gs}$. Both types of behavior are consistent with our simulations and our previous discussion.

From these data we extract $\Phi_B$ vs $V_{gs}$ as shown in Fig. 4(b). There is a striking resemblance between the experimental $\Phi_B(V_{gs})$ dependence and the simulation in Fig. 2. The slope is between 0 and 1 for all $V_{gs}$ as indicated by the gray octant area and as expected from our simulations. The slope of $\Phi_B(V_{gs})$ increases for increasing $V_{gs}$ up to a value of approximately one at around +0.08 V. The true barrier height deduced from the measurement for this CNTFET is $\tilde{\Phi}_B \sim 360 \pm 40$ meV. This is a very reasonable number; approximately half the expected band gap of ~700 meV for the laser ablation tubes used and in agreement with former observations [8,15].

In summary, we have studied the mechanism of charge injection from a 3D metal electrode into a 1D semiconductor. The transition between thermal emission and tunneling in 1D structures has been discussed in detail. We analyzed the impact of various parameters on device characteristics and identified the importance of the effective mass by evaluating experimental data on boron nitride and carbon based nanotube transistors. Finally, we have proposed and demonstrated an approach to quantify the barrier height in metal/semiconductor nanostructures, enabling a more quantitative study of nanodevices.


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[11] To highlight the universal applicability of our approach different barrier heights are simulated.

[12] The prefactor $T^2$ arises from electrons in the 3D metal having a random direction of wave vector when impinging on the metal/semiconductor interface. $T^2$ does not significantly impact the exponential dependence of $I_d$ on $1/T$.

[13] Curves are analyzed with an emphasis on the high temperature regime by determining an "average slope" taking into account at least three different $I_d(T)$ values.

[14] As we assume that $V_{gs}$ has no impact on $\tilde{\Phi}_B$, thermal emission results in the same dashed curve for all $V_{gs}$.

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[18] To account for an observed threshold voltage jump of 260 meV that consistently and reproducibly occurred for all samples between 300 and 200 K presumably due to freeze out of water residuals, the two curves for 100 and 200 K are offset by $\Delta V_{gs} = +260$ meV.