Neuron-Semiconductor Chip with Chemical Synapse between Identified Neurons

R. Alexander Kaul,[1] Naweed I. Syed,[2] and Peter Fromherz[1,*]

[1]*Department of Membrane and Neurophysics, Max Planck Institute for Biochemistry, Martinsried/Munich, Germany 82152*
[2]*Respiratory and Neuroscience Research Groups, University of Calgary, Calgary, Canada T2N 4N1*

(Received 29 August 2003; published 23 January 2004)

Noninvasive electrical stimulation and recording of neuronal networks from semiconductor chips is a prerequisite for the development of neuroelectronic devices. In a proof-of-principle experiment, we implemented the fundamental element of such future hybrids by joining a silicon chip with an excitatory chemical synapse between a pair of identified neurons from the pond snail. We stimulated the presynaptic cell (VD4) with a chip capacitor and recorded the activity of the postsynaptic cell (LPeD1) with a transistor. We enhanced the strength of the soma-soma synapse by repetitive capacitor stimulation, establishing a neuronal memory on the silicon chip.

DOI: 10.1103/PhysRevLett.92.038102 PACS numbers: 87.18.Sn, 73.40.Mr, 87.80.Xa

The nervous system's unique properties to control all animal functions, including learning and memory, hinge upon the synaptic connectivity between many neurons within a network and their ability to exhibit synaptic plasticity in response to environmental stimuli [1]. For a development of neuroelectronic systems, the features of neuronal dynamics and of electronic circuitry have to be combined. In contrast to approaches that electronically emulate neurons [2] or that join neuronal nets with electronics by impaled microelectrodes [3–5], a direct noninvasive interfacing of semiconductor chips and nerve cells leads to real hybrids that are microscopically integrated [6–10]. Here we report on the direct coupling of a silicon chip with the basic element of neuronal learning. We interfaced the pre- and postsynaptic neuron of an excitatory chemical synapse by a silicon chip using identified respiratory neurons from the pond snail *Lymnaea stagnalis* [11–14]. We successfully stimulated the presynaptic neuron VD4 (visceral dorsal 4) by a chip capacitor and recorded postsynaptic excitation in LPeD1 (left pedal dorsal 1) by a transistor. With the soma-soma paired neurons the strength of the cholinergic synapse was potentiated by tetanic capacitor stimulation.

Previous studies demonstrated how individual neurons can be noninvasively coupled to electronic microstructures of a semiconductor substrate, such as capacitors for stimulation [7] and transistors for recording [6]. Two neurons from *L. stagnalis* were electrically connected through a chip [9], and a chip was interfaced with two neurons from *L. stagnalis* that were electrically joined through their grown neurites [8]. The implementation of a neuronal memory on a semiconductor required a microelectronic interfacing of two neurons that formed a chemical synapse as illustrated in Fig. 1(a). It is known that *in vivo* the neuron VD4 from *L. stagnalis* forms a cholinergic synapse with the neuron LPeD1 [11,12]. That synapse can be reconstituted *in vitro* in a soma-soma configuration [13]. By using soma-soma contacts, we avoided problems with a displacement of neurons from their contact sites as caused by neuronal outgrowth [8]. We paired VD4 and LPeD1 neurons on a linear array of microelectronic contacts for stimulation and recording as illustrated in Fig. 1(b). Presynaptic action potentials were

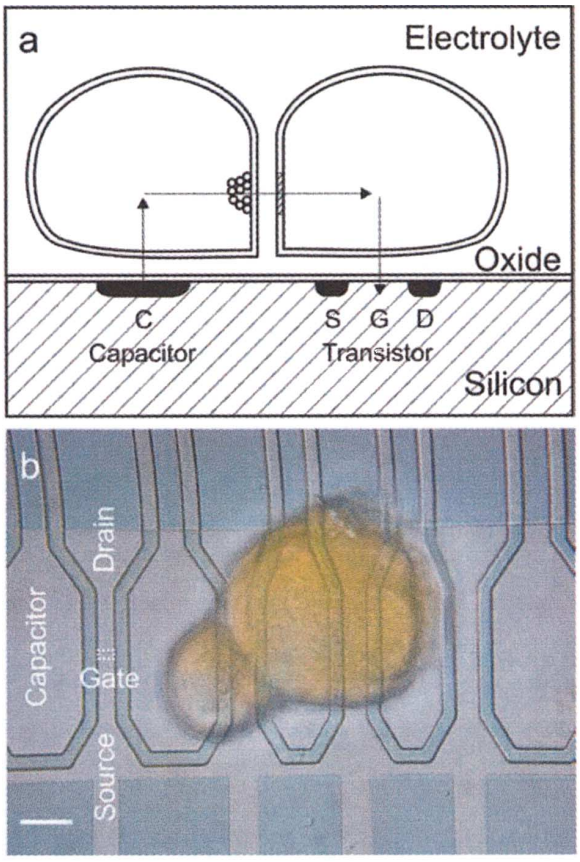

FIG. 1 (color). Silicon chip with synapse. (a) Hybrid device with capacitor (C), chemical synapse, and transistor (gate G, source S, drain D). Not to scale. (b) Micrograph with presynaptic VD4 neuron (left) and postsynaptic LPeD1 neuron (right) from *Lymnaea stagnalis* on a linear array of capacitors and transistors. Scale bar 20 μm.

elicited by a capacitor; pre- and postsynaptic activities were recorded by transistors. Capacitor stimulation was applied to potentiate synaptic strength.

Transistors and capacitors were made by boron doping of *n*-type silicon [6,7]. They were insulated from the electrolyte by a 10 nm layer of silicon dioxide and from one another by narrow lanes of 600 nm local field oxide [15–17]. The chips were wire bonded to a standard package (Spectrum, CPGA 208L, San Jose, CA, USA). A Perspex chamber was attached for the culture medium. Before each use, the chip was wiped with a 10% solution of detergent (FOR, Dr. Schnell, Munich, Germany) in milli-Q water of 70 °C, rinsed with milli-Q water, and sterilized with UV light for 15 min. A solution of poly-L-lysine (MW 84 000, P-1274, Sigma, Munich, Germany) was applied for 8 h (1 mg/ml in 150 mM Tris, *p*H 8.4). Finally the chip was rinsed three times with aqua ad (Braun, Melsungen, Germany), once with antibiotic saline [18], and three times with aqua ad and dried. To obtain individual VD4 and LPeD1 neurons of *L. stagnalis*, the central ring of ganglia of snails (shell length 15–22 mm) was isolated and the neuronal somata were extracted with a suction pipette (60–90 μm diameter) attached to a syringe (Gilmont GS-1200 2 ml, VWR, Brisbane, CA, USA) by a polyethylene tubing [18]. Pairs of VD4 and LPeD1 neurons were incubated for 12–18 h on the chip in 1 ml conditioned medium [18] at room temperature and 80% humidity.

Figure 2(a) shows a chip with the pair of VD4 and LPeD1 neurons that was used to carry out a complete set of experiments as presented below. First, we tested whether a chemical synapse was formed [11]. Conventional intracellular recordings were made from the pre- and postsynaptic neurons. The cells were impaled with microelectrodes made from borosilicate capillaries (1403547, Hilgenberg, Malsfeld, Germany) with a puller (Zeitz, Augsburg, Germany), filled with a saturated solution of K_2SO_4 (15–20 MΩ), contacted with chlorinated silver wires and connected to bridge amplifiers (BA-1S, NPI Instruments, Tamm, Germany). Spontaneous spiking was suppressed by a hyperpolarizing current. Action potentials were elicited by depolarizing pulses of 0.3 nA and 500 ms. We found that presynaptic action potentials in VD4 generated 1:1 excitatory postsynaptic potentials (EPSPs) in LPeD1, as shown in Fig. 2(b) ($n = 6$). These were similar to those seen *in vivo* [11] and *in vitro* [13].

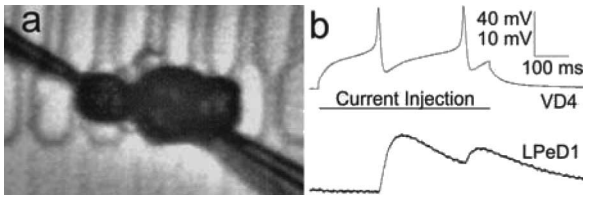

FIG. 2. Neurons with soma-soma synapse on a silicon chip. (a) Micrograph of three neurons on a silicon chip with the central LPeD1 and the left VD4 impaled by micropipette electrodes. (b) Intracellular recording. Upper trace: two action potentials in VD4 elicited by a current injection of 1 nA (holding voltage −60 mV). Lower trace: excitatory postsynaptic potentials (EPSPs) in LPeD1 (holding voltage VD4 −90 mV).

We tested whether action potentials in VD4 could be elicited from the chip by capacitor stimulation, while keeping the cell impaled with a microelectrode. Using a waveform generator (33120A, Hewlett-Packard, Palo Alto, CA, USA) positive voltage pulses were applied to a capacitor (bulk silicon at +7.5 V) with respect to the bath at ground potential (Ag/AgCl electrode) [7–9]. A stimulus consisted of two pulses with +3 V amplitude and 0.5 ms [Fig. 3(a)]. A sequence of three paired pulses gave rise to short responses of the intracellular voltage that induced sustained intracellular depolarizations [Fig. 3(b)]. Action potentials generally occurred after the second or third stimulus.

Excitatory postsynaptic potentials in LPeD1 were induced by capacitively elicited activity in VD4, as observed by intracellular recording (not shown). The EPSPs were indistinguishable from EPSPs induced by intracellular stimulation of VD4. Yet, we focused on the presynaptic stimulation of postsynaptic action potentials, because transistor recording of EPSPs was not possible due to noise. In fact, with intracellular recording we observed postsynaptic action potentials after two to three presynaptic spikes elicited by capacitor stimulation [Fig. 3(d)], in analogy to intracellular presynaptic stimulation [13]. The result provides experimental evidence that capacitor stimulation is able to trigger synaptic transmission ($n = 4$).

To complete the interfacing of synaptic transmission by the silicon chip, we tested whether pre- and postsynaptic activity could be observed with transistors. Before each measurement, the transistors (source at +2.5 V, drains at +0.5 V, source-drain current 50–100 μA) were calibrated by applying defined voltages to the bath. Voltage pulses were applied to a capacitor beneath a VD4 neuron. Short transients appeared in both transistor records beneath VD4 and LPeD1 [Figs. 3(c) and 3(d)] due to extracellular voltages beneath the neuron pair and to electrical cross talk on the chip [8,9]. The action potential in the presynaptic VD4 neuron was recorded by a transistor as a positive transient of extracellular voltage with an amplitude around 3 mV [Fig. 3(c)]. The action potential elicited in the LPeD1 neuron by synaptic transmission was recorded by a transistor as a sharp peak of about 3 mV in its rising phase [Fig. 3(e)]. This experiment demonstrates the interfacing of a chemical synapse by a semiconductor chip with presynaptic capacitor stimulation and pre- and postsynaptic transistor recording. The results with intracellular monitoring of both cells ($n = 3$) were confirmed by experiments without impaling LPeD1 ($n = 2$) and without impaling either cell ($n = 2$) (not shown).

A particularly interesting aspect of the VD4-LPeD1 synapse is its capability to exhibit short-term potentiation [14] that is thought to form the basis of working memory

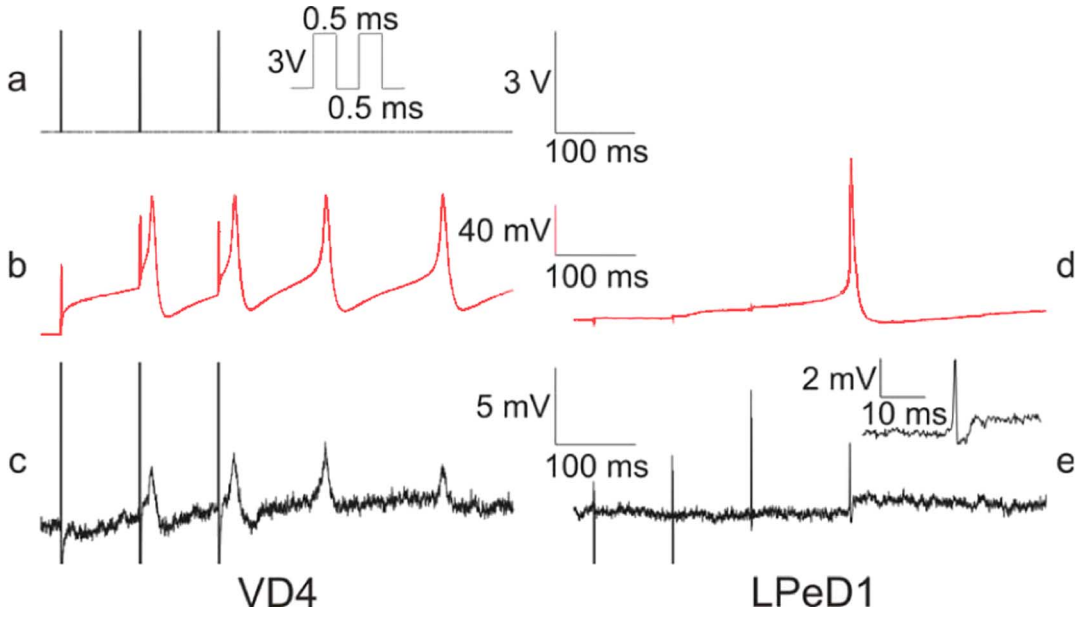

FIG. 3 (color online). Synaptic transmission on silicon chip. (a) Voltage at the capacitor beneath VD4 with three double-pulse stimuli (blowup). (b) Intracellular voltage of VD4 with four action potentials (holding voltage −60 mV). (c) Transistor record of VD4 with responses to the presynaptic action potentials. (d) Intracellular voltage of LPeD1 with one postsynaptic action potential (holding voltage −70 mV). (e) Transistor record of LPeD1 with the response to the postsynaptic action potential (blowup). The short transients in the transistor records are due to extracellular voltages beneath the neuron pair and to electrical cross talk on the chip.

in animals [1]. Specifically, a presynaptic tetanus in VD4 consisting of five to ten action potentials enhances the amplitude of subsequent EPSPs which generate postsynaptic spikes in LPeD1 [14]. At first, we reproduced that short-term plasticity on the chip with current injection through intracellular electrodes ($n = 5$, not shown). Then we tested whether the potentiation could be elicited by capacitor stimulation and recorded with a transistor. Since transistor recording of EPSPs was not possible, we probed the potentiation by the appearance of postsynaptic action potentials. First as a control, a single action potential was elicited in VD4 by a pair of voltage pulses applied to the capacitor. In that case postsynaptic depolarization was not sufficient to elicit an action potential in LPeD1 [Fig. 4(a)]. Then a capacitive tetanus of six single voltage pulses (3 V, 0.5 ms) was applied that triggered five action potentials in VD4 [Fig. 4(b)]. To test for potentiation, again an action potential was elicited in VD4 a few seconds after the tetanus [Fig. 4(c)]. The post-tetanic action potential in the presynaptic cell reproducibly caused a postsynaptic spike in LPeD1 that was recorded by the transistor [Fig. 4(c)]. The experiment shows that the modulation of a soma-soma synapse can be directly induced and monitored by the silicon chip ($n = 2$).

For an interpretation of pre- and postsynaptic interfacing, we have to consider the nature of the neuron-silicon junction. With *Lymnaea* neurons plated on silicon with poly-L-lysine, the lipid core of the plasma membrane is separated from the chip by a cleft of about 50 nm width with the specific conductivity of bulk electrolyte [8,19]. The electrical coupling of cell and chip — of capacitor stimulation as well as of transistor recording — is determined by the area specific conductance of the cleft g_J which is proportional to its width [10]. When a voltage step of height V_S^0 is applied to the capacitor, an exponential voltage transient $V_J(t)$ is induced in the junction according Eq. (1) where c_S and c_M are the area specific capacitances of chip and membrane.

$$V_J(t) \approx V_S^0 \frac{c_S}{c_S + c_M} \exp\left(-\frac{g_J}{c_S + c_M} t\right). \qquad (1)$$

At $V_S^0 = 3$ V with $g_J = 30$ mS/cm^2, $c_S = 0.34$ μF/cm^2, and $c_M = 4$ μF/cm^2 [8] we estimate an amplitude of 230 mV and a time constant of 110 μs. Such strong, short extracellular voltage pulses may affect the conductance of the attached membrane with a depolarizing current that gives rise to action potentials. The process is reversible without persisting damage of the neurons. Transient electroporation may be involved.

An action potential with the intracellular voltage $V_M(t)$ gives rise to capacitive and ionic currents through the attached membrane. A transistor records the resulting extracellular voltage $V_J(t)$ between cell and chip [10] as described by Eq. (2) with the area specific conductances g_{JM}^i of the attached membrane and the reversal voltages V_0^i.

$$V_J(t) \approx \frac{1}{g_J}\left[c_M \frac{dV_M}{dt} + \sum_i g_{JM}^i (V_M - V_0^i)\right]. \qquad (2)$$

Different weights of capacitive current [first term of Eq. (2)] and ionic currents [second term of Eq. (2)] give rise to different shapes of the response $V_J(t)$ for VD4

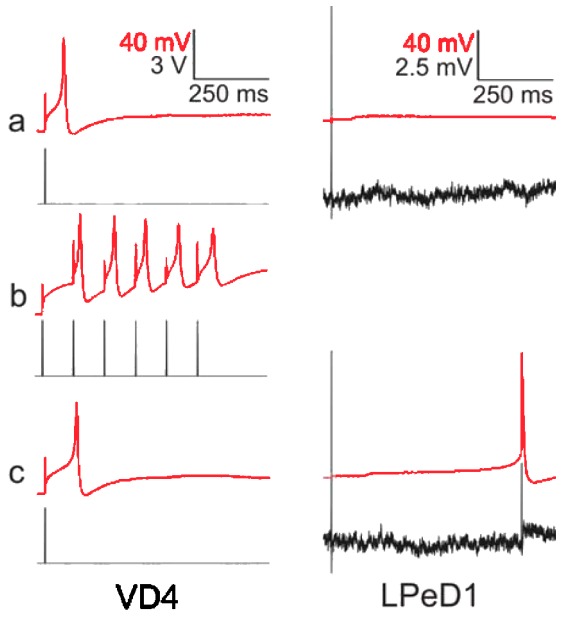

FIG. 4 (color online). Synaptic potentiation on a silicon chip. The upper traces show intracellular voltages in red, the lower traces capacitor stimuli (left) and transistor records (right) in black. (a) Control. Capacitor stimulation of VD4 neuron with action potential in VD4 (left) and no postsynaptic action potential in LPeD1 (right). (b) Potentiating stimulus. Train of six capacitor stimuli applied to VD4 with action potentials. (c) Potentiated response. Capacitor stimulation of VD4 with action potential in VD4 (left) and postsynaptic action potential in LPeD1 (right).

neurons and for LPeD1 neurons (Figs. 3 and 4). A capacitive outward current dominates in the narrow positive response in LPeD1 matching the rising phase of the action potential $V_M(t)$. In VD4 the wide positive response resembles the shape of $V_M(t)$ itself. In this case ionic outward currents dominate through potassium or leak conductance.

The cholinergic nature of the synapse between VD4 and LPeD1 is well established [11,12]. The electronically controlled synaptic transmission and potentiation (Figs. 3 and 4) are consequences of successful interfacing the pre- and postsynaptic neuron. A presynaptic mechanism of potentiation is likely, induced by calcium ions [20]. A direct effect of Ca entering the cell through leaks induced by capacitor stimulation can be excluded, as its intracellular diffusion (diffusion coefficient $<20\ \mu m^2/s$) [21] is too slow to reach the synapse during a potentiation experiment.

In the present Letter, we have shown that chemical synapses exhibiting short-term memory can be directly joined to a semiconductor chip. The study forms the basis for various directions of research, such as long-term investigations of memory in neuronal nets, developments of biochips for chemicals interfering with synaptic activity, and implementations of hybrid systems that integrate electronic circuits with typical features of neuronal dynamics and memory [22,23]. Stimulators with higher capacitance and transistors with lower noise will improve the quality of interfacing and enable a gating of ion channels and a monitoring of postsynaptic potentials. Homologous chips fabricated by complementary metal-oxide-semiconductor (CMOS) technology with two-dimensional arrays of transistors [24] and capacitors will allow an interfacing of large neuronal networks.

We thank Günther Zeck and Paolo Bonifazi for the chips, Carool Popelier (Free University of Amsterdam) for the generous gift of the animals, and Wali Zaidi for excellent technical assistance. We acknowledge the support of the Max Planck Society for funding the cooperation between Munich and Calgary.

*To whom correspondence should be addressed.
Electronic address: fromherz@biochem.mpg.de

[1] E. R. Kandel, Science **294**, 1030 (2001).
[2] M. Mahowald and R. Douglas, Nature (London) **354**, 515 (1991).
[3] D. Kleinfeld, F. Raccuia-Behling, and H. J. Chiel, Biophys. J. **57**, 697 (1990).
[4] Y. Yarom, Neuroscience **44**, 263 (1991).
[5] A. A. Sharp *et al.*, J. Neurophysiol. **69**, 992 (1993).
[6] P. Fromherz *et al.*, Science **252**, 1290 (1991).
[7] P. Fromherz and A. Stett, Phys. Rev. Lett. **75**, 1670 (1995).
[8] G. Zeck and P. Fromherz, Proc. Natl. Acad. Sci. U.S.A. **98**, 10 457 (2001).
[9] P. Bonifazi and P. Fromherz, Adv. Mater. **14**, 1190 (2002).
[10] P. Fromherz, in *Nanoelectronics and Information Technology*, edited by R. Waser (Wiley-VCH Verlag, Berlin, 2003), pp. 781–810.
[11] T. Hamakawa *et al.*, J. Neurosci. **19**, 9306 (1999).
[12] A. B. Smit *et al.*, Nature (London) **411**, 261 (2001).
[13] M. A. Woodin *et al.*, Learning & Memory **6**, 307 (1999).
[14] H. Naruo *et al.*, in *Proceedings of Neuroscience Meeting 2002* (Society for Neuroscience, Orlando, FL, 2002), Abstract No. 552.8.
[15] R. Weis, B. Muller, and P. Fromherz, Phys. Rev. Lett. **76**, 327 (1996).
[16] A. Stett, B. Muller, and P. Fromherz, Phys. Rev. E **55**, 1779 (1997).
[17] M. Ulbrich and P. Fromherz, Adv. Mater. **13**, 344 (2001).
[18] N. I. Syed, H. Zaidi, and P. Lovell, in *Modern Techniques in Neuroscience Research*, edited by U. Windhorst and H.H. Johansson (Springer-Verlag, Berlin, 1999), pp. 361–377.
[19] G. Zeck and P. Fromherz, Langmuir **19**, 1580 (2003).
[20] N. Syed (unpublished).
[21] M. Gabso, E. Neher, and M. E. Spira, Neuron **18**, 473 (1997).
[22] J. Foss and J. Milton, J. Neurophysiol. **84**, 975 (2000).
[23] J. J. Hopfield, Proc. Natl. Acad. Sci. U.S.A. **79**, 2554 (1982).
[24] B. Eversmann *et al.*, IEEE J. Solid-State Circuits **38**, 2306 (2003).