

Field-Modulated Carrier Transport in Carbon Nanotube Transistors

J. Appenzeller,¹ J. Knoch,² V. Derycke,¹ R. Martel,¹ S. Wind,¹ and Ph. Avouris¹

¹IBM T.J. Watson Research Center, Yorktown Heights, New York 10598

²Massachusetts Institute of Technology, Cambridge, Massachusetts 02139

(Received 2 April 2002; published 29 August 2002)

We have investigated the electrical transport properties of carbon nanotube field-effect transistors as a function of channel length, gate dielectric film thickness, and dielectric material. Our experiments show that the bulk properties of the semiconducting carbon nanotubes do not limit the current flow through the metal/nanotube/metal system. Instead, our results can be understood in the framework of gate and source-drain field induced modulation of the nanotube band structure at the source contact. The existence of one-dimensional Schottky barriers at the metal/nanotube interface determines the device performance and results in an unexpected scaling behavior.

DOI: 10.1103/PhysRevLett.89.126801

PACS numbers: 73.63.Fg, 73.63.Rt, 85.35.Kt

Since it was experimentally shown that semiconducting carbon nanotubes (CNs) can work as field-effect transistors (FET) [1–3], significant progress has been made. By using thin gate dielectric films, operating voltages were reduced to around 1 V [4,5]. It was also found that the observed *p*-type behavior of carbon nanotube transistors is a contact rather than a bulk effect [6]. Moreover, both *n*-type as well as *p*-type transistor action was realized [7], and individual devices were combined in an intramolecular carbon nanotube-based logic element [8]. All these results suggest that carbon nanotubes may have the potential to function as building blocks in a future nanoelectronics technology.

However, there is still a limited understanding about how transport through a carbon nanotube field-effect transistor (CNFET)—and a transistor based on a one-dimensional (1D) semiconductor in general—is affected by the internal fields. This Letter addresses this question. The most important experimental observation is that the intrinsic tube properties *do not* limit the device characteristics. Instead, the existence of Schottky barriers at the nanotube/metal contact interface and their response to the applied electric fields determines the electrical performance of CNFETs. This rather unusual situation is a consequence of the difficulty to create an ideal Ohmic CN-metal contact. Our data are not a result of a specific procedure for sample preparation, and therefore this new interpretation is universally applicable. It also implies that the extraction of any bulk nanotube related parameter, e.g., mobility from the *I*-*V* characteristics is not justified.

When the current (I_d) in a CNFET is monitored as a function of the source/drain field, it is typically found [4,5,9] that for the right gate field polarity this current saturates for large enough source/drain voltages (V_{ds}) (see Fig. 1). For conventional metal oxide semiconductor field-effect transistors (MOSFETs) this is a very well known effect and is attributed to the so-called channel pinch-off [10]. Because of this similarity between conventional

MOSFET characteristics and those of CNFETs, it was argued that the electrical data can be analyzed in the context of bulk switching of a nanotube in the diffusive transport regime [2].

In order to investigate this hypothesis and to study the physics of transport in a nanotube transistor as an example of a 1D device structure, we have fabricated and characterized various CNFETs with dielectric film thicknesses (t_{ox}) ranging from 15 to 150 nm, effective dielectric constants (ϵ_{eff}) between 2.5 and 7.5, and channel lengths (L) from 100 nm to 1 μ m. Nanotubes produced by laser ablation [11] were dispersed from a 1,2-dichloroethane solution. Different types of contact and gate configurations were studied. In most cases source and drain contacts of titanium were positioned above SWNTs and the silicon substrate was used as a gate electrode.

First, we focus on devices with a dielectric film thickness of about 20 nm. For these devices gate and source/

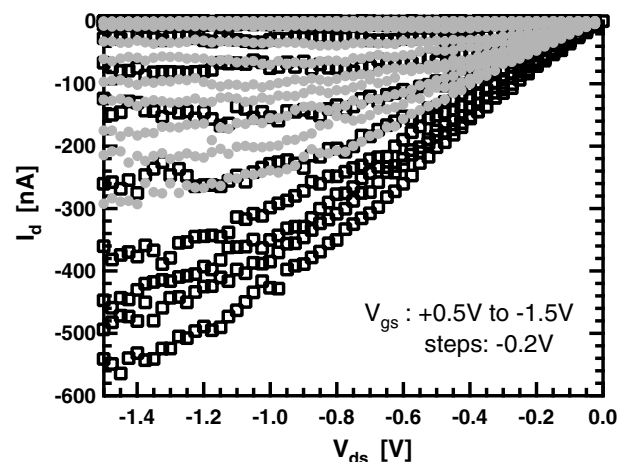


FIG. 1. Output characteristics of a bottom-gated *p*-type CNFET with $L = 300$ nm and $t_{ox} = 20$ nm HfO_2 at $T = 300$ K. The two curve sets belong to the same device exchanging the source and drain electrode.

drain voltages of around 1 V are sufficient to fully turn the transistors on and off. Figure 1 shows typical output characteristics for a CNFET with $L = 300$ nm and $t_{\text{ox}} = 20$ nm HfO_2 ($\epsilon \approx 11$). The difference between the two sets of measurements shown is that source and drain have been exchanged. Note that exchanging source with drain is *not* the same as reversing the polarity of V_{ds} because the gate voltage breaks the field symmetry. While it is still the same nanotube device within the same voltage range, the data look significantly different. The most pronounced difference in the two measurement configurations is visible in the saturation currents $I_{\text{d sat}}$ (for $V_{\text{ds}} \leq -1$ V). If pinch-off were, in fact, what causes the current to saturate, this difference could not exist, since then the nanotube, which is the same in both measurements, would determine $I_{\text{d sat}}$. We find that in some devices saturation currents can differ by as much as a factor of 5 for the *same* nanotube. This observation cannot be explained by nonideal contact series resistances which can alter the slope of the I_{d} versus V_{ds} curves for small V_{ds} but cannot impact the current in the saturation region. In fact, our observation is evidence that the nanotube itself does not determine the electrical performance in state-of-the-art CNFETs.

The same conclusion can be drawn by examining the off-state of carbon nanotube devices. Valuable information about the switching behavior of a transistor can be obtained from the change of current through the device as a function of the gate voltage (V_{gs}) characterized by the inverse subthreshold slope $S = dV_{\text{gs}}/d(\log I_{\text{d}})$. In a conventional MOSFET thermal emission over the conduction band (n -FET) or valence band (p -FET) of the semiconductor determines I_{d} as long as there is no charge in the channel (in our case on the tube). This results in an exponential dependence I_{d} on the gate voltage with an exponent proportional to $1/k_{\text{B}}T$ as long as V_{gs} is below the threshold voltage V_{th} [12]. In a conventional long-channel MOSFET, S shows a significant dependence on neither the gate-to-channel coupling given by the gate capacitance (C_i) nor on the source/drain voltage V_{ds} [10]. Instead, S depends only on temperature according to $S \approx (k_{\text{B}}T/q) \ln 10$, with $S = 60$ mV/dec for $T = 300$ K.

Figure 2 shows the current versus gate voltage dependence for devices with (a) a SiO_2 film thickness of $t_{\text{ox}} = 120$ nm and (b) a HfO_2 film of $t_{\text{ox}} = 20$ nm for various V_{ds} ($L = 300$ nm). The insets display the corresponding temperature dependence of S as defined above. The following details can be noticed: (A) S remains constant for temperatures $T < 200$ K for both devices, (B) at $T = 300$ K the slopes in Figs. 2(a) and 2(b) are much larger than 60 mV/dec and differ by a factor of more than 12, and (C) the curves in Fig. 2(a) for the *thick* oxide are shifted to the right for decreasing (more negative) V_{ds} . All these findings cannot be explained assuming that CNFETs behave as ordinary MOSFETs. On the other hand, they can easily be understood as a consequence of the gate and

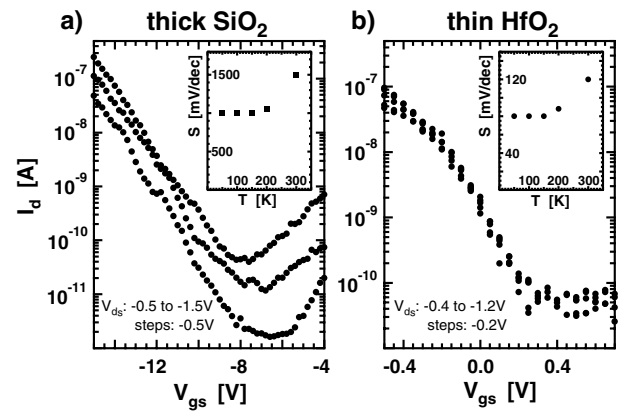


FIG. 2. Source-drain current at 300 K as a function of gate voltage for different V_{ds} for two p -type devices with (a) $L = 300$ nm and $t_{\text{ox}} = 120$ nm SiO_2 and (b) $L = 300$ nm and $t_{\text{ox}} = 20$ nm HfO_2 . The inset shows the dependence of the inverse subthreshold slope S as a function of temperature for both devices.

source-drain field induced modulation of the nanotube band structure in the vicinity of the source contact.

Figure 3 shows the band bending in a three-terminal nanotube device qualitatively for two different gate field conditions. In case Fig. 3(a) the device is essentially off—there is no charge accumulated on the tube [13]. In Fig. 3(b) the gate voltage is sufficiently large to turn the transistor on. Since hole transport is considered, the important part to focus on is the valence band and here, in particular, the source side as emphasized by the circle in Fig. 3(a). For discussion purposes, we divide the transistor into three segments. (i) and (iii) describe the situation close to source and drain, respectively, while (ii) accounts for the bulk part of the carbon nanotube. The most important ingredients are the Schottky barriers in (i) and (iii). The existence of these barriers at a nanotube/metal interface has been pointed out before [6,14], and their critical role for the transport in a CNFET is clarified here.

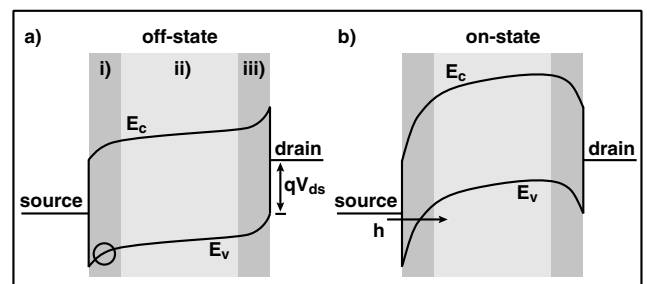


FIG. 3. Qualitative response of the nanotube conduction and valence band on the gate voltage for a fixed negative source-drain voltage. (a) A gate voltage below threshold voltage describing the situation in the transistor off-state. (b) The band bending situation for a gate voltage well above V_{th} .

In Fig. 3(a) the current from source to drain is blocked by the barrier in the source region. However, the barrier thickness and thus the tunneling current through the barrier can be modulated by both the gate and the source-drain field. In contrast to former discussions of CNFETs, the bulk part (ii) of the nanotube is not directly involved in controlling the off-current below V_{th} .

In this context our experimental observation (A) on the temperature dependence of S is crucial. If the nanotube itself would pose a barrier for current transport and thus bulk switching would dominate, S should decrease for decreasing temperature. This is not the case. Instead, S saturates at $T < 200$ K (see insets of Fig. 2) indicating that the change in the CNFET current is determined by tunneling through the source Schottky barrier [15]. In this picture, for V_{ds} exceeding a few hundred mV, the current through the nanotube device in the off-state is determined by the coupling of the gate field to the 1D Schottky barrier in the source region since no barrier exists in region (iii) [13]. Because of this coupling, S becomes a function of the gate capacitance and thus the dielectric film thickness t_{ox} in agreement with our observation (B) in Fig. 2, a behavior not expected for a regular MOSFET. The dependence of the off-current on the source-drain field—observation (C) from Fig. 2(a) for *thick* oxides—can also be understood in this model. Increasing the drain voltage reduces the barrier thickness in (i) of Fig. 3(a).] To compensate for the impact of a drain voltage change (ΔV_{ds}) on the shape of the barrier in region (i), the gate voltage has to be adjusted by ΔV_{gs} . Doing so, the former field condition (i.e., the same I_d) can be recovered. The thicker the gate oxide, the smaller is the impact of the gate field and the larger ΔV_{gs} . For a 120 nm SiO_2 film $\Delta V_{gs}/\Delta V_{ds}$ can be as much as 2000 mV/V as seen in Fig. 2(a).

The transport properties of a CNFET as a function of gate voltage can be summarized as follows: For a given value of V_{ds} , increasing the gate field results in an exponential-like increase of I_d . This is the case since the transmission probability for tunneling through the source Schottky barrier increases with decreasing barrier thickness (Fig. 3(a)). The situation changes when the gate voltage reaches a value (V_{th}) where the valence band in region (ii) coincides approximately with the Fermi level in the source electrode (Fig. 3(b)). From this voltage on charge starts to accumulate in the tube, and the movement of the bands with the gate voltage slows down. The barrier thickness at the source contact no longer changes as significantly as before, and the increase in tunneling current as a function of gate voltage is reduced accordingly. While the resulting characteristics are very similar to those of conventional MOSFETs, the physics behind both, the exponential change of current with the gate field and the reduced increase of I_d for gate voltages beyond a certain voltage, identified as V_{th} , are different. In particular, scaling the device dimensions has a different impact

on the device operation than in a conventional MOSFET because of the different ways the fields influence the nanotube band structure.

Figure 3(b) also explains the electrical characteristics in Fig. 1. Exchanging the source and the drain electrodes while keeping the gate voltage and source-drain voltage conditions constant can result in a quite different current response of the system if the barriers in regions (i) and (iii) are slightly different. This is due to the exponential sensitivity of the tunneling current on the actual barrier height of the source Schottky barrier. The role of the bulk section (ii) of the nanotube is minor as can be seen from the significantly different dependence on the internal fields for the *same* nanotube. The main function of the tube is to provide Schottky barriers at the source and the drain of the CNFET. This means that the nanotube could, in principle, be replaced by another one-dimensional semiconducting system with the same work function. It also implies that neither the linear region nor the saturation region in Fig. 1 can be used to extract information about the intrinsic tube properties. The shape of the curves in Fig. 1 simply reflects the response of the source and the drain Schottky barriers to the gate and source-drain fields.

Having established the critical dependence of the transport properties in a CNFET on the Schottky barrier, we want to study the impact of various device parameters on the electrical performance. This information is necessary if we aim to understand the physics behind the scaling behavior of carbon nanotube field-effect transistors. We focus again on the inverse subthreshold slope S . According to our model, there should be a strong, monotonic variation of S with the gate capacitance C_1 since the coupling between the gate and the source Schottky barrier depends on the dielectric film thickness t_{ox} . On the other hand, the source-drain field and thus the channel length L are not expected to have a significant impact on S . This is supported by the data in Fig. 2(a) where S is not affected by V_{ds} .

In Fig. 4 the data (dots) present measurements on *p*-type, *n*-type, and ambipolar devices of various lengths L , gate oxide thicknesses t_{ox} , and effective dielectric constants ϵ_{eff} [16]. We also show S values extracted from Refs. [4,17,18] (gray stars in Fig. 4). All the data follow the expected universal trend of decreasing S with decreasing oxide thickness. Note that S varies by almost 2 orders of magnitude. The data also reveal a significant variation between devices for the same ϵ_{eff} to t_{ox} ratio. This observation is not unexpected since the barrier height in the source region is strongly influenced by the environmental conditions, particularly by the concentration of adsorbed oxygen in the contact region [6]. Furthermore, the plot indicates that the nanotube length L does not significantly affect S . This is observed, e.g., from the three data points marked L_1 to L_3 which belong to samples with channel lengths of $L_1 = 30$ nm, $L_2 = 800$ nm, and $L_3 = 300$ nm,

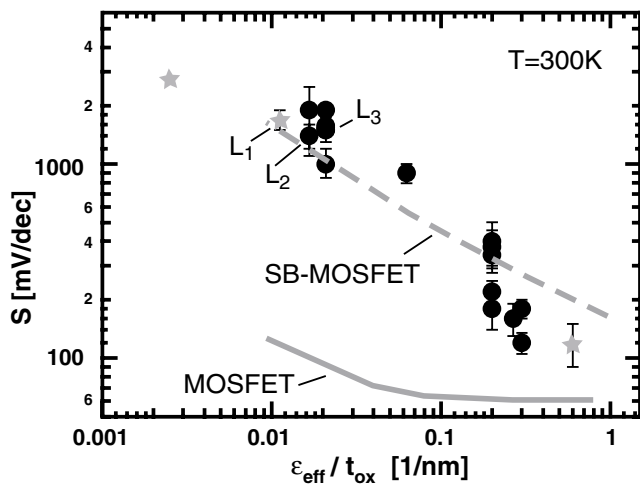


FIG. 4. Inverse subthreshold slope S as a function of gate capacitance. Gray stars are data extracted from publications of other groups (see text for details). The data marked L_1 , L_2 , and L_3 belong to devices with channel lengths of 30, 800, and 300 nm, respectively. The lines represent calculations on MOSFETs with (dashed line) and without (solid line) Schottky barriers (SB) of 0.3 eV.

respectively. Although the nanotube length differs by more than a factor of 20 between the longest and the shortest device, the actual slope S is almost the same in all three cases.

Figure 4 also shows simulations for field-effect devices with (dashed line) and without (solid line) Schottky barriers of $\Phi_B = 0.3$ eV. We model a system consisting of Schottky barriers in the source and drain region connected by an ultrathin channel layer. This layer simulates well the situation in the off-state of a carbon nanotube and ensures that screening in the device is correctly incorporated. In order to accurately describe the tunneling contribution to the overall current, the Schrödinger equation is solved self-consistently with the Poisson equation in the entire system. No scattering inside the tube is taken into account. Our calculations strongly support the qualitative description of the nanotube transistor action. The experimental behavior observed does not follow the expected trend for a conventional MOSFET (solid line). It does, however, agree very well with the behavior of a Schottky barrier (SB) carbon nanotube field-effect transistor SB-CNFET (dashed line).

In conclusion, we have discussed experimental results on the electrical transport in carbon nanotube field-effect transistors. We have shown clear evidence that the experimental findings can be consistently explained with a Schottky barrier CNFET model. The results presented are essential for both a better fundamental understanding

of transport in one-dimensional systems and the evaluation of the potential of carbon nanotubes as active components in a future nanoelectronics technology.

The authors thank P. Solomon and S. Heinze for helpful discussions and D. Neumayer for chemical vapor deposition of HfO_2 .

- [1] S. J. Tans, A. Verschueren, and C. Dekker, *Nature (London)* **393**, 49 (1998).
- [2] R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and Ph. Avouris, *Appl. Phys. Lett.* **73**, 2447 (1998).
- [3] H. T. Soh, C. F. Quate, A. F. Morpurgo, C. M. Marcus, J. Kong, and H. Dai, *Appl. Phys. Lett.* **75**, 627 (1999).
- [4] A. Bachtold, P. Hadley, T. Nakanishi, and C. Dekker, *Science* **294**, 1317 (2001).
- [5] S. Wind, J. Appenzeller, R. Martel, V. Derycke, and Ph. Avouris, *Appl. Phys. Lett.* **80**, 3817 (2002).
- [6] V. Derycke, R. Martel, J. Appenzeller, and Ph. Avouris, *Appl. Phys. Lett.* **80**, 2773 (2002).
- [7] M. Bockrath, J. Hone, A. Zettl, P. L. McEuen, A. G. Rinzler, and R. E. Smalley, *Phys. Rev. B* **61**, R10606 (2000).
- [8] V. Derycke, R. Martel, J. Appenzeller, and Ph. Avouris, *Nano Lett.* **1**, 453 (2001).
- [9] C. Zhou, J. Kong, and H. Dai, *Appl. Phys. Lett.* **76**, 1597 (2000).
- [10] S. M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981).
- [11] A. Thess, R. Lee, P. Nikolaev, H. Dai, P. Petit, J. Robert, C. Xu, Y. H. Lee, S. G. Kim, A. G. Rinzler, D. T. Colbert, G. E. Scuseria, D. Tomanek, J. E. Fischer, and R. E. Smalley, *Science* **273**, 483 (1996).
- [12] V_{th} is the voltage for which charge starts to get accumulated in the channel region.
- [13] For small source/drain voltages a barrier may also exist in section (iii) of Fig. 3 for certain V_{gs} . To suppress the impact of the drain Schottky barrier, all measurements in Fig. 2 were carried out at sufficiently large $|V_{ds}|$.
- [14] M. Freitag, M. Radosavljević, Y. Zhou, A. T. Johnson, and W. F. Smith, *Appl. Phys. Lett.* **79**, 3326 (2001).
- [15] Tunneling through a triangular shaped barrier is temperature dependent and results in the observed increase of S above $T = 200$ K.
- [16] We investigated samples with nanotubes fully embedded in SiO_2 ($\epsilon_{eff} \approx 4$), with the tubes in air and either SiO_2 or HfO_2 as a back side dielectric material ($\epsilon_{eff} \approx 2.5$ and 6, respectively), and with the tubes embedded in HfO_2 on a back side SiO_2 film ($\epsilon_{eff} \approx 7.5$). ϵ_{eff} was determined as described in Ref. [2].
- [17] M. Radosavljević, Ph.D. thesis, University of Pennsylvania, Philadelphia, 2001, p. 53.
- [18] M. W. Bockrath, Ph.D. thesis, University of California, Berkeley, 1999, p. 29.