Quantitative Electron Holography of Biased Semiconductor Devices

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Electron holography is used to measure electrostatic potential profiles across reverse-biased Si *p-n* junctions *in situ* in the transmission electron microscope. A novel sample geometry based on focused ion-beam milling is developed, and results are obtained for a range of sample thicknesses and bias voltages to allow the holographic contrast to be interpreted. The physical and electrical nature of the sample surface, which is affected by sample preparation and electron beam irradiation, is discussed.

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The ability to determine electrically active dopant distributions on a nanometer scale is of fundamental importance for understanding semiconductor device properties and performance [1]. Transmission electron microscopy (TEM) techniques provide the sub-10 nm resolution required to characterize microstructure and chemistry, but conventional intensity (amplitude) images reveal little or no information about the local concentration of ionized dopant atoms. Electron holography is an interference-based TEM technique, which can be used to record the phase shift of a high-energy electron wave that has passed through a sample [2]. The resulting phase image can be analyzed to determine the electrostatic potential within the specimen (projected in the incident electron beam direction), from which the local charge density can be calculated using Poisson's equation. The characterization of two-dimensional dopant potentials in unbiased semiconductor samples has recently been demonstrated [3–5]. Here we extend the electron holography technique to quantify the electrostatic potential across a Si *p-n* junction as it is biased electrically *in situ* in the TEM. Our approach makes use of a novel TEM sample geometry based on focused ion beam (FIB) sample preparation. The effect of this type of sample preparation on holographic contrast observed from both biased and unbiased samples is investigated, and the results are used to assess the physical and electrical nature of the surface of the TEM sample.

A nominally abrupt Si *p-n* junction was formed by using molecular beam epitaxy to grow a 2.5 μm thick 4×10^{18} cm^{-3} B-doped (*p*-type) layer on a 4×10^{18} cm^{-3} Sb-doped (*n*-type) substrate. Samples were prepared for TEM examination by using a 30 kV FEI 200 FIB workstation to machine parallel-sided electron-transparent membranes at the corners of 1 mm × 1 mm 90° cleaved squares of wafer, as shown schematically in Fig. 1(a). This sample geometry allowed electrical spring contacts to be made to the front and back surfaces of the cleaved wafer in a modified single tilt sample holder [Fig. 1(b)] for a Philips CM300 field emission gun TEM. Off-axis electron holograms were obtained at an accelerating voltage of 200 kV using a rotatable Möllenstedt-Düker biprism located in the selected area aperture plane of the microscope [Fig. 2(a)], and recorded digitally on a 2048 × 2048 pixel charge coupled device camera located at the end of a Gatan imaging filter. A biprism voltage of 100 V was used, and operation of the microscope in Lorentz mode [6] allowed a holographic interference width of 800 nm to be achieved. The sampling density of each hologram was typically 1 nm/pixel, while that of the reconstructed phase and amplitude images was 8 nm/pixel. Samples were always tilted by 1°–2° from the ⟨100⟩ zone axis, while keeping the *p-n* junction edge-on to better than ~0.2°, to ensure that dynamical diffraction effects were minimized, and reference holograms were used to remove distortions associated with the imaging and recording system [7]. Great care was taken during sample preparation to minimize the implantation of Ga ions into the sample by exposing the area of interest to the focused beam of Ga ions only at a glancing angle to its surface. The final stage of milling was performed parallel to the surface of the

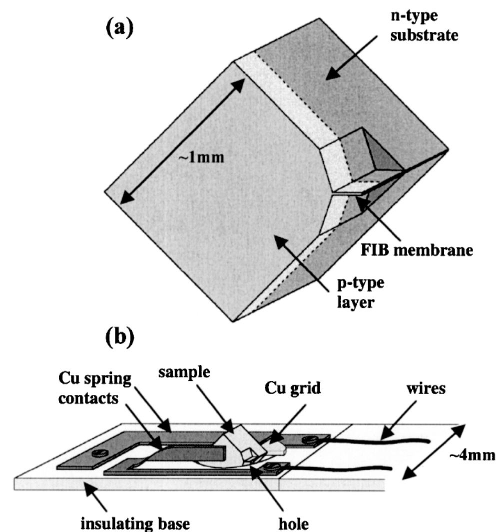

FIG. 1. (a) Schematic diagram showing the specimen geometry used for biasing experiments. FIB milling has been used to machine a membrane of uniform thickness that contains a *p-n* junction, at one corner of a 90° cleaved wedge. (b) Schematic diagram showing the sample position in a single tilt electrical biasing holder. The sample is glued to the edge of a Cu grid using conducting epoxy and then clamped between two spring contacts on an insulating base.

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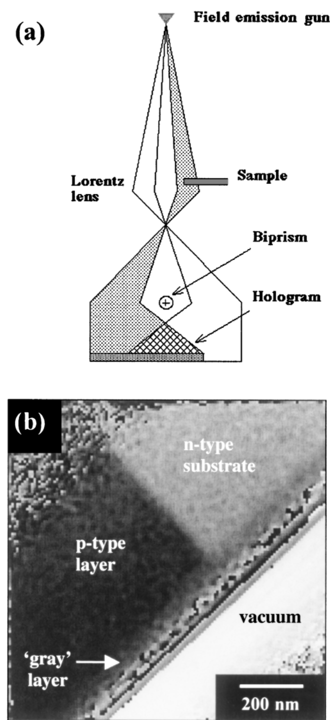

FIG. 2. (a) Schematic diagram illustrating the formation of an electron hologram. The field emission gun provides coherent illumination and the biprism enables overlap of the object and reference waves. (b) Reconstructed phase image of an unbiased Si sample containing a p-n junction. Note the "gray" layer running along the edge of the membrane, which is discussed in the text. No attempt has been made to remove the 2π phase "wraps" at the edge of the sample.

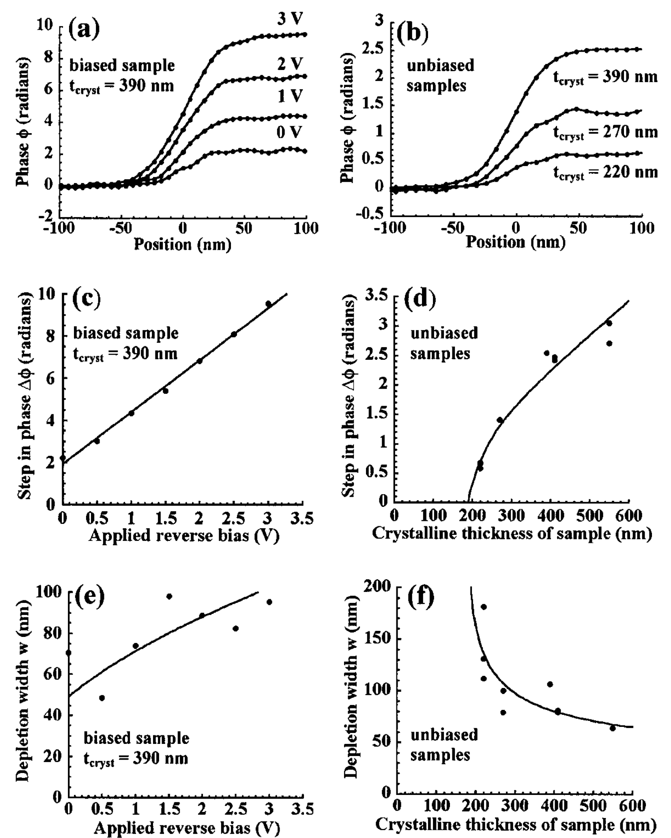

FIG. 3. Phase (ϕ) measured across p-n junctions as a function of (a) reverse bias for a single sample of crystalline thickness 390 nm (measured using convergent beam electron diffraction), and (b) crystalline sample thickness for three unbiased samples. (c) and (d) show the height of the measured step in phase ($\Delta\phi$) across the junction as a function of reverse bias and sample thickness, respectively. The downturn in the fitted curve in (d) at small sample thickness is explained in the text. (e) and (f) show the corresponding depletion widths (w) obtained by fitting simulated phase profiles to the data. The fit to (e) is proportional to the square root of the net voltage across the junction. The curves added to (d) and (f) are simple empirical fits to the data.

electron-transparent membrane using a small spot size of 10 nm with a low beam current of 150 pA. Problems that have been noted when examining doped semiconductor samples in the past, including sample charging, thickness corrugations, and strain [8,9], were not observed in this study.

Figure 2(b) shows a representative electron holographic phase image obtained from an unbiased sample, whose crystalline thickness was measured to be 550 nm using convergent beam electron diffraction. The p-type and n-type regions are delineated clearly as areas of dark and bright contrast, respectively. An additional "gray" band at the sample edge corresponds to an electrically "inactive" layer, which is visible in cross section in this image and is thought to run around the entire sample surface. Line profiles across the p-n junction were obtained from such phase images by averaging the recorded signal parallel to the junction, both for different reverse bias voltages applied to a single sample whose crystalline thickness was measured to be 390 nm [Fig. 3(a)] and for several unbiased samples of different thicknesses [Fig. 3(b)]. Ignoring dynamical contributions to the contrast, which are negligibly small at the orientations chosen, the phase profiles ϕ in Figs. 3(a) and 3(b) are proportional to the electrostatic potential in the sample V integrated in the electron beam direction z, according to the equation

$$\phi(x,y) = C_E \int V(x,y,z)\,dz\,, \qquad (1)$$

where x and y are directions in the plane of the sample and C_E is a sample-independent constant and takes the value 7.29×10^6 rad $\mathrm{V^{-1}\,m^{-1}}$ at 200 kV. Each of the profiles in Figs. 3(a) and 3(b) is qualitatively consistent with the expected potential profile of a p-n junction contained within a sample of uniform thickness [10]. The potential step across the junction $\Delta\phi$ increases with both reverse bias voltage and sample thickness, as expected from Eq. (1) and shown in Figs. 3(c) and 3(d), respectively.

Assuming that the p-n junction is contained within an electrically active layer of thickness t_{active} within the total sample thickness t, $\Delta\phi$ can be related to the built-in voltage across the p-n junction V_{bi} and to the applied reverse

bias voltage V_{appl} using the equation

$$\Delta\phi = C_E(V_{\mathrm{bi}} + V_{\mathrm{appl}})t_{\mathrm{active}}, \tag{2}$$

where

$$t = t_{\mathrm{active}} + t_{\mathrm{inactive}} \tag{3}$$

and t_{inactive} is the total thickness of the electrically "dead" layers on the two sample surfaces. Such layers are thought to result from a combination of surface depletion, damage and implantation from sample preparation, and the buildup of surface charge as a result of secondary electron emission in the TEM. Neglecting them would result in artificially low measured values for V_{bi} [3].

Several conclusions can be drawn from Figs. 3(c) and 3(d). According to Eq. (2), the gradient of Fig. 3(c) is $C_E t_{\mathrm{active}}$. This expression can be used to determine a value for t_{active} of 340 ± 10 nm, indicating that 50 ± 10 nm of the crystalline sample thickness (25 ± 5 nm on each surface of the sample) is electrically inactive. Similarly, the intercept of the graph with the vertical axis is $C_E V_{\mathrm{bi}} t_{\mathrm{active}}$, which provides the expected value for V_{bi} of 0.9 ± 0.1 V. It is significant that the results in Fig. 3(c) confirm that the p-n junction appears to work correctly as a function of applied bias within the TEM sample, despite the fact that simple spring contacts were used to connect the sample holder to the surfaces of the wafer. The results from the unbiased and the biased samples are consistent with each other, and the gradient of Fig. 3(c) would be lower if significant series resistance were present in the circuit. The only anomaly in the results is the deviation of Fig. 3(d) from a straight line, suggesting that the thickness of the electrically inactive layer on the sample surfaces increases at the lowest sample thicknesses. (A simple straight line would lead to a poor fit to the data points, and would be inconsistent with other results.) Anomalous results at low sample thicknesses have also been observed in defocused images of p-n junctions by Beleggia *et al.* [11].

Simulations were fitted to the profiles shown in Figs. 3(a) and 3(b) to obtain an estimate of the depletion width w. The results are shown as a function of reverse bias voltage and sample thickness in Figs. 3(e) and 3(f), respectively. Although there is some scatter in the data points, the expected increase in depletion width with bias voltage is confirmed. The depletion width is expected to be proportional to the square root of the net voltage across the junction, and the fitted curve shows this dependence. The measured depletion widths are higher than expected (a value close to 30 nm is predicted at zero applied bias), suggesting that the electrically active dopant concentration in the sample is lower than the nominal value. This point will be discussed elsewhere. Figure 3(f) shows an increase in depletion width at the lowest sample thicknesses, again suggesting [as in Fig. 3(d) above] that the thinnest samples exhibit anomalous behavior.

Further information about the physical and electrical nature of the sample surfaces is shown in Fig. 4. Figure 4(a) shows a comparison of the *total* thickness of each sample t measured from the holographic amplitude image (in units of inelastic mean free path) [12] with the *crystalline* thickness t_{cryst} obtained by convergent beam electron diffraction. These parameters are related to the total thickness of the amorphous layers on the sample surfaces $t_{\mathrm{amorphous}}$ by the equation

$$t = t_{\mathrm{cryst}} + t_{\mathrm{amorphous}}. \tag{4}$$

The fact that the graph does not pass through the origin but through a value of −60 ± 10 nm on the horizontal axis suggests that 30 ± 5 nm thick amorphous layers are present on each surface of the sample, in agreement with direct measurements of damage produced by FIB milling [13]. The electrical nature of the sample surface was investigated by examining the vacuum region just outside the edge of the sample. Figure 4(b) shows a phase image obtained from a 90° cleaved wedge sample that had *not* been FIB milled, under an applied reversed bias of 2 V, in which an external electrostatic fringing field similar to that predicted by Beleggia *et al.* [14] is visible. Such fringing fields were not observed outside either unbiased cleaved wedges or any FIB-milled samples, indicating that, in contrast to chemically thinned samples [15], the surface of an FIB-prepared sample is an equipotential under applied bias. The effect of surface charging on contrast from

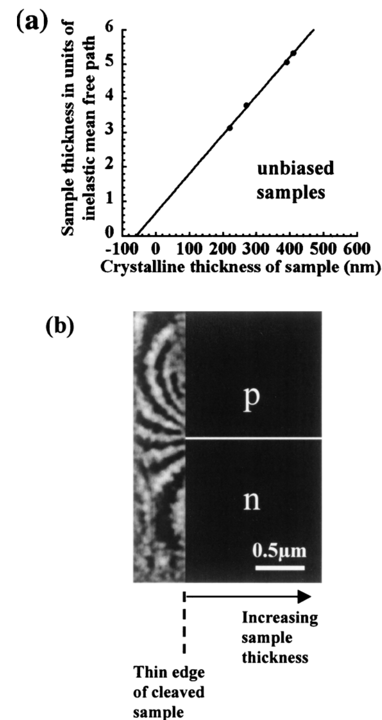

FIG. 4. (a) Sample thicknesses measured from holographic amplitude images and using convergent beam electron diffraction, suggesting the presence of a 30 nm thick amorphous layer on each surface of the sample. (b) 4× phase-amplified reconstructed phase image, showing the vacuum region outside a p-n junction in a 2 V reverse biased cleaved wedge specimen that had not been FIB milled.

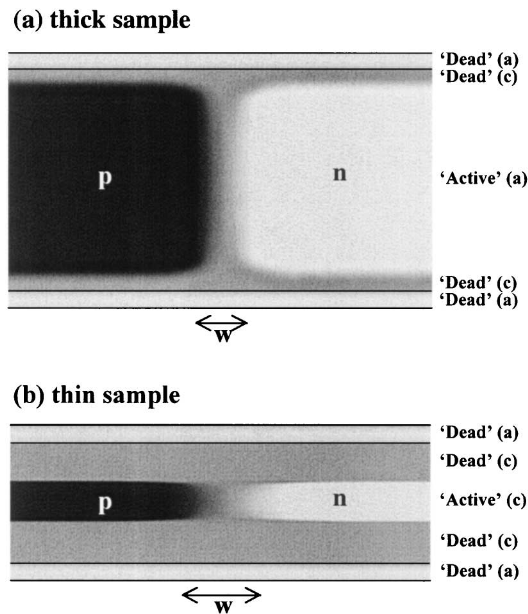

FIG. 5. Schematic diagrams, for two different sample thicknesses, showing the cross-sectional structure of the sample inferred from data obtained over a range of sample thicknesses and bias voltages. The sample surfaces are amorphous, within these are crystalline but electrically dead layers, and within these is the electrically active junction of depletion width w. "c" and "a" refer to crystalline and amorphous regions of the sample, respectively. The shading provides a schematic representation of the variation in potential within the crystalline region.

p-n junctions in TEM samples, and, in particular, on the presence of electrostatic fringing fields, has been discussed by Beleggia *et al.* [16].

Combining the results in Figs. 3 and 4 allows a consistent, semiquantitative picture of the cross-sectional structure of the FIB milled samples to be inferred. Figure 5 illustrates the layered structure suggested by the experimental results. The sample surfaces are covered by a 30 nm thick amorphous layer, which results from sample preparation. Beneath this amorphous layer is an electrically inactive crystalline layer. This layer is 25 nm thick when the crystalline thickness of the sample is 390 nm, and within it is the electrically active junction of depletion width w. Both the thickness of the crystalline electrically inactive layer and the depletion width increase at the lowest sample thicknesses. This effect may result from the proximity of the two sample surfaces to each other. The results suggest that a sample thickness of at least 350 nm is required to obtain accurate results from FIB milled samples, and that a similar systematic analysis should be performed to understand the effect of other types of TEM sample preparation on holographic contrast, as well as the apparent absence of surface depletion layers on wedge-polished TEM samples [17].

In summary, a novel sample geometry has allowed off-axis electron holography to be used to provide quantitative information about a semiconductor device as a function of applied bias. A p-n junction has been examined to address issues associated with hologram interpretation without the additional complications from thickness corrugations and strain that may be present when examining a real integrated circuit. Such effects may be removed in future experiments by making use of differences between holograms obtained at different bias voltages. Results obtained as a function of reverse bias voltage and sample thickness have been found to be reproducible. The nature of the sample surface has been assessed, and criteria have been established for obtaining reliable results from samples prepared using FIB milling. In particular, great care is required to minimize the extent of damage and Ga implementation introduced by FIB sample preparation. An increase in depletion width and dead layer thickness has been observed at the lowest sample thicknesses, and the surface of an FIB milled sample has been found to be an equipotential under applied bias. With the increasing use of electron holography in semiconductor characterization, these results should aid in holographic interpretation and help in improving analysis and quantification of hologram reconstruction.

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