Bistability in Scanning Tunneling Spectroscopy of Ga-Terminated Si(111)

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(Received 11 October 1999)

Bistable electron transport, a phenomenon usually associated with double-barrier structures, has been observed with a conventional STM junction formed between a metal tip and a Ga-terminated Si(111) surface at 77 K. Large hysteresis loops appear in the current-voltage characteristics when electrons are injected from the tip to the surface. The *turn-on* bias varies from -3.1 to -4.0 V and shows an inverse dependence on the tip-sample distance, indicating a strong field effect. The *turn-off* bias, however, is essentially pinned at a conductance threshold of -2.7 V.

PACS numbers: 73.40.Gk, 61.16.Ch, 72.20.–i, 73.20.–r

The bistable current-voltage (I-V) characteristic of a semiconductor device is a manifestation of the hysteretic switching between a high-impedance, low-current (*off*) state and a low-impedance, high-current (*on*) state. This nonlinear transport phenomenon has been the basis of a family of power switching devices since the early development of semiconductor physics [1]. The advent of high speed tunneling devices, particularly the resonant tunneling diodes, has rekindled interest in bistable tunneling because of its important digital applications [2–9]. While historical power switching devices are comprised of a stack of p-n-p-n junctions, modern high speed switching devices consist of epitaxially grown multiheterojunctions or δ-doped layers. All these devices share a common and essential feature of having at least one potential well bound by two barriers, known as the double-barrier structure (DBS). It is the charge accumulation in the well that results in an electrostatic feedback and prolongs the initial conductance state. Subsequent relinquishing of the excess charges from the well then brings the device to the opposite conductance state. Although the conditions or origins leading to the bistability for various device structures may differ, the necessity of a double- or multibarrier structure in a switching device is widely acknowledged and indeed is incorporated in all the reported devices that exhibit bistable I-V characteristics.

Here, we report the first experimental observation of bistable scanning tunneling spectra obtained at 77 K in an ultrahigh vacuum (UHV) chamber. As schematically shown in the inset of Fig. 1, the basic elements of our tunnel junction, as embodied in a typical scanning tunneling microscope (STM) setup, are the metal tip and an n-type Si(111) surface terminated by Ga atoms. Despite its structural simplicity, this apparent single-barrier structure exhibits functions that were previously observed only in a more complex DBS. Indeed, the lack of a typical DBS in our tunneling junction poses a serious challenge for interpreting this unusual finding.

Our experiment was performed in an UHV system with a base pressure of 3×10^{-11} Torr. To form the tunnel junction, we used a tungsten tip in a homemade UHV low temperature STM and an n-type Si(111) wafer phosphorus doped to 2×10^{17} cm^{-3}. The quality and chemical compositions of the surface, both before and after Ga deposition, were monitored with Auger spectrometer, reflection high energy electron diffraction and STM. Following the preparation of a clean and well ordered Si(111) 7×7 surface, approximately one monolayer (ML) of Ga atoms (1 ML $\approx 8 \times 10^{14}$ atoms/cm^2) was deposited onto the cold substrate and subsequently annealed to 400–500 °C. This procedure yields a 6.3×6.3 reconstruction of Ga atoms on Si(111), as is well documented in the literature [10]. The sample was then transferred to the STM anchored at the bottom of a vapor-shield cryostat in the same UHV system. All tunneling measurements were performed at 77 K.

The superlattice structure of the 1 ML Ga-covered Si(111) has been previously studied by standing wave x-ray and STM measurements, and by *ab initio* total-energy calculations [11–13]. It is found that at least 80% of the Ga atoms locate at a single top layer forming a network of domains with a period of 24 Å. Each domain contains ~10 Ga atoms arranged in a two-dimensional close-packed configuration with a 4.1 Å atomic separation. The inset of Fig. 1 depicts the model most consistent

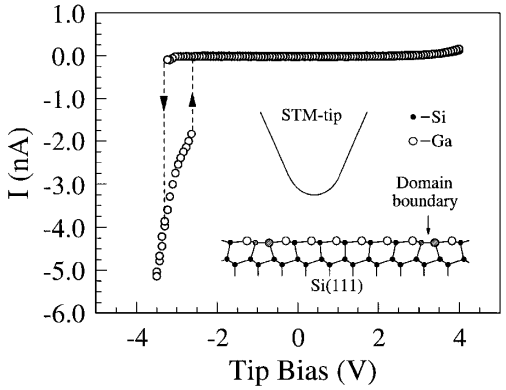

FIG. 1. An I-V spectrum acquired with a full sweep of the tip bias from +4 to −4 V and returning back to +4 V. The negative tip bias regime displays a hysteresis loop. The inset depicts the tunnel junction formed between an STM tip and the Ga-terminated Si(111) surface.

 0031-9007/00/84(6)/1284(4)$15.00

with both the experimental results and the calculation. Ga atoms substitute the outermost Si atoms in the last bilayer through the $sp2$ hybridization of the valence states. At the expense of a stain buildup in the bulk, this bonding configuration leads to an inward relaxation of the Ga atoms by as much as 0.52 Å (from 0.78 Å) and a 7% lateral expansion, resulting in a nearly planar structure stabilized by a network of domain boundaries. The detailed atomic arrangement of the boundary is not known.

Although it has yet to be verified experimentally, the above model implies that the $sp2$-like Ga-Si states, replacing the Si surface states in the energy band gap, should appear near the valence band edge, and that the lowest unoccupied p_z orbital of the Ga atoms is expected to have a stronger atomic character and to lie above the conduction band edge. Thus, an otherwise semimetallic Si(111) surface is transformed into an ideal insulating overlayer, and the Si sample into a flat band semiconductor. A tunnel junction formed between this surface and a metal tip of an STM separated by a vacuum barrier is equivalent to a typical metal-insulator-semiconductor device [1]. For n-type Si, both the conduction and valence bands will bend downward when the tip is biased positively or upward when negatively biased, resulting in carrier accumulation or depletion and inversion, respectively. This will give rise to asymmetric diodelike I-V characteristics. Because of effective screening of the external field under strong carrier accumulation or inversion at the Si surface, the overall band bending is limited to the size of the Si band gap, E_g, and the current onset should be delayed by no more than $\sim E_g/e$ in either bias polarity. A similar transport behavior has been observed for a H-terminated Si surface [14]. As we shall demonstrate below, however, the effect of terminating the Si(111) surface with a 1 ML Ga atoms goes far beyond the passivation of a semiconductor.

Figure 1 is a typical tunneling spectrum acquired with a full sweep of the tip bias, V_{tip}, from $+4$ to -4 V and then reversed back to $+4$ V. During the sweep, the tip-sample distance is held constant. Unlike a typical tunneling I-V spectrum of a semiconductor surface, a pronounced *hysteresis loop* appears at the negative polarity. In the forward sweep (0 to -4 V), the tunnel current I does not turn *on* until V_{tip} reaches -3.2 V while, in the reversed sweep, I does not turn *off* until V_{tip} is reduced to -2.6 V. We refer to these two characteristic tip biases as V_{on} and V_{off}, respectively. Apart from this hysteresis loop, the I-V spectrum exhibits a typical diode character with $V_{\text{tip}} > 0$ corresponding to a *forward bias* and $V_{\text{tip}} < 0$, the *reverse bias*. These I-V characteristics do not seem to depend on whether the tip is placed over the domains or domain boundaries, nor do they depend on a specific shape of the tip. When proper care is exercised, repetitively sweeping the tip bias across the low and high conductance regimes does not cause destruction of the surface atomic arrangement. Identical measurements have been performed on a number of different Si samples and we obtained similar hysteresis loops. Furthermore, stable imaging conditions of this surface can be obtained either under positive tip bias or in the high conductance regime of the negative bias.

The hysteresis loop as characterized by V_{on} and V_{off} depends strongly on the tip-sample distance d. Figure 2 shows a set of the hysteresis loops of incremental d acquired as follows. We first set the tip at the initial distance, the feedback is then opened, and an I-V loop measurement is performed; while keeping the feedback circuit open, we adjust successively the tip to the next separation and repeat the I-V measurements. An opposite sequence of measurements from larger to smaller distances has also been used and yielded similar results. As d increases from 5 to 8 Å, V_{on} reduces from -3.95 to -3.35 V. In contrast, V_{off} changes only a miniscule amount but also shows a reversed dependence on d as shown in the inset of Fig. 2. The measured V_{on} and V_{off} vs d is plotted in Fig. 3(a). While V_{off} is essentially pinned at the *threshold* of $V_0 = -2.7$ V, V_{on} can be fitted to the expression $V_{\text{on}} = -A/d^{\gamma} + V_0$ (solid curve), where $\gamma \approx 1.5$. The smallest detectable V_{on} in our experiment is -3.1 V (not shown here).

The dependence of the hysteresis loop on the tip-sample distance is manifested in a different set of measurements. Again, the tip is set at an initial position, but this time V_{tip} is kept at a constant value *inside* a hysteresis loop while the tip is moved back and forward with respect to the surface. As shown in Fig. 3(b), during the retraction, I abruptly turns on when d reaches 6.25 Å. On the other hand, when the tip is approaching the surface, I increases smoothly at a rate of one decade per Å, as is typical for vacuum tunneling, indicating that the STM vacuum junction dominates the impedance once the tunneling is turned on.

Although our STM junction consists apparently of only the vacuum barrier, the above evidence strongly points to the presence near the surface of a second barrier, henceforth the *surface barrier,* which has the following characteristics. First, the magnitudes of V_{on} and V_{off} suggest

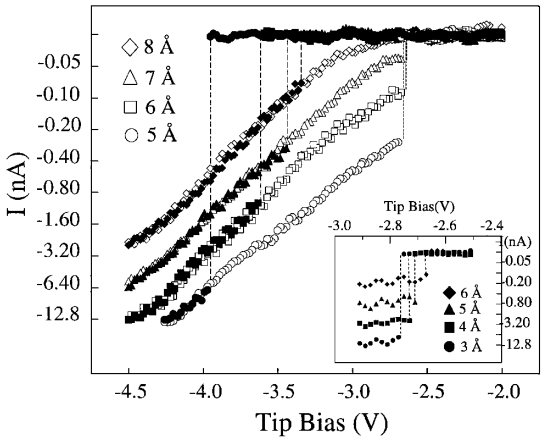

FIG. 2. Tunneling hysteresis loops obtained with a number of tip-sample distances. The inset is the magnified portion near the *turn-off* biases.

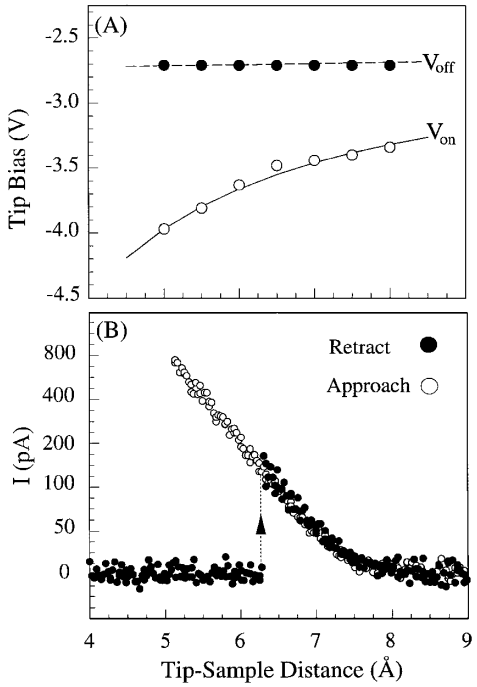

FIG. 3. (A) Measured V_{on} and V_{off} vs the tip-sample distance. The dashed line is a linear fit to V_{off} while the solid curve is the fitting of $V_{on} = -A/d^{\gamma} + V_0$, with $V_0 = -2.7$ V, $\gamma \approx 1.5$, and $A \approx 15$, (B) Change of the tunneling current as the tip retracts from or approaches the surface. The tip bias is kept at -3.7 V during the ramp.

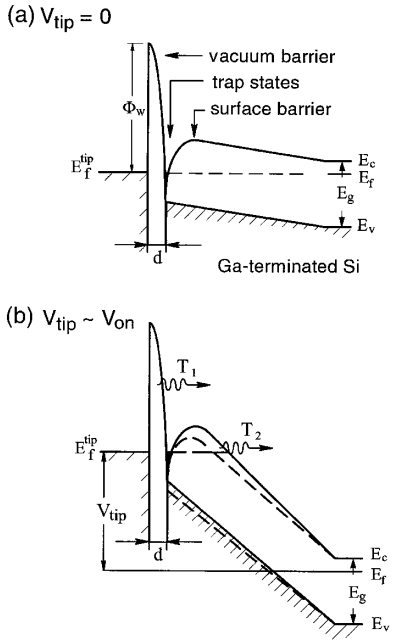

FIG. 4. Energy diagram for the tunnel junction formed between the metal-tip and the Ga-terminated Si surface: (a) under equilibrium and (b) around the *turn-on* point. E_c and E_v indicate the conduction and valence band edge of the Si, respectively.

that a large portion of V_{tip} falls across the surface barrier so that it must be related to a space charge region that varies with V_{tip}. Second, under the negative tip bias condition, the surface barrier is much more opaque than the vacuum barrier for small V_{tip}, and becomes transparent when $V_{tip} > V_{on}$. We are, therefore, led to the assumption that a high density of localized trap states below the Fermi level (E_F) exists near the surface. Note that the *localized* nature of the traps is essential for the electrostatic feedback for delocalized surface states or impurity bands will prevent charge accumulation under the tip. Although the microscopic origin of these traps is not yet clear, we speculate that they are associated with ~0.2 ML ($\sim 1 \times 10^{14}$ cm^{-2}) Ga atoms that are not accounted for by the coverage over the domains [12]. The up limit of the Ga bulk concentration in Si is $\sim 2 \times 10^{20}$ cm^{-3} [15], so the majority of these Ga atoms should reside near the surface, most likely along the domain boundaries. In the absence of the external field, these trap states are partially filled by the majority carriers (electrons), creating a charge depletion region and, hence, a barrier around the traps as illustrated in Fig. 4. This is similar to a one-sided abrupt *pn* junction. The depletion region is sufficiently large to make an opaque barrier despite its relatively small height compared with the vacuum barrier [16]. Conversely, the capacitance of the surface barrier is much smaller than that of the vacuum barrier so that the former will share a much larger portion of the applied voltage through serial capacitive division. When the tip is biased positively or negatively, the charge depletion region in the proximity of the tip will shrink or grow, resulting in a forward or reverse bias situation of a typical diode. In addition, charge accumulation Q in the localized trap states can take place, causing the surface potential to rise or fall by the amount of the charging potential.

We can now show that together the unfilled trap states, the vacuum barrier, and the surface barrier will function as a conventional DBS and can give rise to the observed hysteresis. Let T_1 be the tunneling rate from the metal tip to the traps through the vacuum barrier and T_2 from the traps and the bulk Si through the surface barrier. Both are determined by the transfer Hamiltonian [17]. Following the above arguments, we have $T_1 \gg T_2$ when $V_{tip} = 0$. As V_{tip} increases towards V_{on}, electrons injected from the tip will accumulate in the trap so that $\Delta Q < 0$ and the charging potential (U) keeps the trap states in equilibrium with the metal [Fig. 4(b)]. Since most of the bias falls on the surface barrier, T_2 will increase rapidly while T_1 sees little change [solid line of Fig. 4(b)]. As soon as T_2 passes T_1, the accumulated charges are drained to the bulk ($\Delta Q > 0$), a drop of U occurs, and T_2 goes up further [dashed line of Fig. 4(b)]. As a result, the current is turned on abruptly. Once in the low impedance state $T_2 \gg T_1$, the condition is sustained even when V_{tip} is subsequently reduced to less than V_{on}. But as V_{tip} decreases so does T_2. When T_2 drops below T_1, electron accumulation ($\Delta Q < 0$) and the rise of T_2 will accelerate, and I will be abruptly turned off, returning the system to the high impedance state. Therefore, the switching between the high- and low-impedance states is controlled by the matching condition

of $T_1 = T_2$, and hysteresis arises because such a condition can be met at two distinct charging states of the traps.

In the simplest approximation, T_1 and T_2 can be regarded as the transmission coefficients of the vacuum and surface barrier, respectively. Thus, $T_1 \propto \exp\{-\alpha d\}$ but an analytical form of T_2 is not available. From the measured dependence of V_{on} on d [Fig. 3(b)] and the criterion $T_1(V_{\text{on}}) = T_2(V_{\text{on}})$, we can obtain an empirical expression: $T_2 \propto \exp\{-\beta/(V_0 - V_{\text{tip}})^{1/\gamma}\}$ (for $V_{\text{tip}} \leq V_0$), where the parameters α and β are related to the barrier heights and are under the strong influence of V_{tip} and U. To see qualitatively the inverse dependence of V_{on} on d, let us consider the tip at d and biased just below the turn-on point V_{on} (Fig. 4). If we now increase d, T_1 will go down but at the same time the depletion region in Si will be reduced because of the smaller voltage division and, hence, T_2 will go up. This means that the balance condition can be reached at a smaller V_{tip}. Obviously, a similar argument for V_{off} will lead to a conclusion contradicting the fact that the V_{off} is essentially pinned at -2.7 V, regardless of the change of d. This can be reconciled somewhat by noting that after turn-on, $T_2 > T_1$, and the charge accumulation in the traps can adjust dynamically to compensate for the effect of changing d [2]. Or, perhaps, it is more likely that the conductance threshold is connected with an energy threshold between the trap states and the bulk Si band structure when the detailed coupling matrix is considered.

The above discussion does not require that the tunneling be limited to a two-step process. Direct tunneling from the metal tip to the Si conduction band will certainly take place once $T_2 \gg T_1$. In fact, in a nonresonant situation, the global transmission coefficient T for both processes is indistinguishable [2], i.e., $T = T_1 T_2$. The hysteresis loop spans from -4.0 to -2.7 V. This implies that electrons entering the Si are *hot carriers* and will dissipate their excess kinetic energy through inelastic processes. Although the energy of these *hot carriers* is insufficient to trigger the *avalanche multiplication* [1] which requires a threshold energy of $\sim 6E_g$, it can additionally contribute to the positive feedback of the current by several means. First, the local heating will ionize the dopant ($\sim$70%) that is otherwise frozen at 77 K. This will reduce the depletion region and, hence, increase its capacitance significantly. As a result, T_1, T_2 and the total number of available states are increased. Second, the heating of the junction will raise the probability of phonon-assisted tunneling so that the tunneling current is further enhanced. Finally, it has been shown that, in a two-step tunneling process, the increase of the electron temperature, and, hence, the thermal emission rate in the traps, can also result in hysteresis [5].

In conclusion, bistable electron transport has been observed with a conventional STM junction formed between a metal tip and a Ga-terminated Si surface. The size of the hysteresis loop strongly depends on the tip-sample distance and, therefore, is tunable in an STM setup. We have shown a plausible scenario in which the presence of a single atomic layer of Ga on the Si surface can enable such a simple junction to function as a more complex double barrier structure. Furthermore, the magnitude of the switching voltage is comparable to practical hot carrier devices that exploit a shorter carrier transport time. This new finding could become the basis for developing new types of switching devices that are simpler, smaller, and faster.

We wish to thank M. Burns, K. Matveev, V. Narayanamurti, H. Okamoto, S. Pryadkin, and T. Yamada for valuable discussions.

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[16] For a rough estimate, we note that the dopant concentration of our n sample is $N_D = 2 \times 10^{17}$ cm^{-3} and about 30% of them are ionized at 77 K which gives the Debye length $L_D = (\varepsilon_s kT/q^2 N_D^+)^{1/2} \approx 80$ Å (q being the elementary charge). At zero bias with a maximum junction potential $V_{pn} \approx E_g/q$, the depletion width $W_0 = L_D(2qV_{pn}/kT)^{1/2} \approx 1450$ Å, and the amount of charge drawn from the depletion layer to the surface traps is $\sim 8.8 \times 10^{11}$ cm^{-2}, equivalent to only 0.02 ML of Ga atoms. For the planar junction geometry, the transmission coefficient through a 10 Å vaccum barrier is $\sim \exp\{-2d(2m^*\phi_W/\hbar^2)^{1/2}\} \approx \exp\{-10\}$, while for the 1450 Å surface barrier it is $\sim \exp\{-(4W_0/3)(2m^*E_g/\hbar^2)^{1/2}\} \approx \exp\{-1000\}$.
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