Giant Permittivity in Epitaxial Ferroelectric Heterostructures

A. Erbil,[1,*] Y. Kim,[1,†] and R. A. Gerhardt[2]
[1]*School of Physics, Georgia Institute of Technology, Atlanta, Georgia 30332*
[2]*Materials Science and Engineering, Georgia Institute of Technology, Atlanta, Georgia 30332*
(Received 17 April 1996)

A giant permittivity associated with the motion of domain walls is reported in epitaxial heterostructures having alternating layers of ferroelectric and nonferroelectric oxides. At low frequencies, permittivities as high as 420 000 are found. Real and imaginary parts of the dielectric constant show large dispersion at high frequencies. In dc measurements, a nonlinear resistance is observed with a well-defined threshold field correlated with the dc bias-field dependence of ac permittivities. We interpret the observations as a result of the motion of a pinned domain wall lattice at low electric fields and sliding-mode motion at high electric fields. [S0031-9007(96)00938-6]

PACS numbers: 77.84.Lf, 77.22.Ch, 77.55.+f, 77.80.Dj

Under epitaxial strain, a single crystal ferroelectric thin film has an equilibrium structure with a periodic array of domain walls [1,2]. Theoretical [3–6] and experimental [1,2,7] studies show that, in ferroelectric thin films, the formation of a periodic domain pattern limits the extension of the interfacial strain field—thus minimizing the total energy of the heterostructure. This is in contrast to an unclamped single crystal system, for which a single domain is the equilibrium state. It is found that the nature of the domain pattern depends very strongly on the epitaxial mismatch, the film thickness, and measurement temperature.

In a system without defects, we would expect a domain wall to move freely under an external driving force in the host material in the continuum limit. In a domain wall lattice, this property is expected to lead to low energy excitation modes, called dyadons, corresponding to the acoustic waves in the domain wall lattice [5]. A rigid translation of the domain wall lattice can take place without having an energy barrier. However, the nucleation of a domain wall, the presence of defects, including dislocations, surface steps, compositional variation, etc., can lead to the pinning of the domain walls. For an external field below a certain threshold field, the domain walls can oscillate in the pinned state and its motion is bound. Above the threshold field, the domain wall lattice can slide continuously to contribute to the dc conductivity, by creating domain walls at one electrode and annihilating at the other. The phenomenon is reminiscent of the Frohlich sliding-mode conductivity in charge-density waves [8], and phase-slip resistivity in Josephson junctions in superconductors [9].

In this Letter, we demonstrate experimentally that these effects yield giant dielectric permittivity in epitaxial ferroelectric heterostructures.

Epitaxial ferroelectric $PbTiO_3$ and paraelectric $Pb_{1-x}La_xTiO_3$ thin films with $x = 0.28$ were grown on [100]-oriented single-crystal $SrTiO_3$ substrates using metal-organic chemical vapor deposition. The details of the deposition process have been reported previously [10]. We have studied in detail three superlattices of $PbTiO_3/Pb_{1-x}La_xTiO_3$ with periodicities of 10 nm (sample S-40), 40 nm (sample S-10), and 200 nm (sample S-2). In each superlattice, the $PbTiO_3$ and $Pb_{1-x}La_xTiO_3$ layers had equal thicknesses, and the total thickness was 400 nm. The first and last layers deposited were $PbTiO_3$ and $Pb_{1-x}La_xTiO_3$ respectively.

X-ray diffraction, pole figure, and ion channeling experiments were performed to determine the epitaxial quality of the superlattice. Secondary ion mass spectroscopy was utilized to examine the compositional modulation. An interdigital gold electrode pattern with 50 fingers was deposited by using photolithography on the sample surface for impedance measurements. Each finger was 25 μm wide and 2 mm long, and the oppositely biased neighboring fingers were spaced center to center by 50 μm.

The θ-2θ x-ray diffraction patterns of the samples S-2 and S-10 show the coexistence of *a* and *c* domains as expected for the ferroelectric state. With decreasing period, the spontaneous strains become smaller consistent with the earlier observations [1]. The sample S-40 exhibits a single peak, providing evidence that the superlattice is paraelectric for a period of 10 nm. The broad widths for the peaks of S-10 and S-2 suggest that different ferroelectric layers in the superlattices have different spontaneous strain values depending on their locations. This would lead to a distribution of parameters for the equilibrium and dynamical states. Since the ferroelectric superlattices show qualitatively similar behaviors, in this Letter only the data for S-10 are presented and discussed in detail.

Figure 1(a) shows a dc *I*-*V* curve taken at room temperature for the sample S-10. This figure shows highly nonlinear resistance with a well defined threshold voltage V_T of about 5 V. Well above the threshold voltage, the data show Ohmic behavior. The measured dc current shown in Fig. 1 is the time and space averaged current over the electrodes. Possible current oscillations due to wall-antiwall creation [11] shall be the subject of a future study.

 0031-9007/96/77(8)/1628(4)$10.00

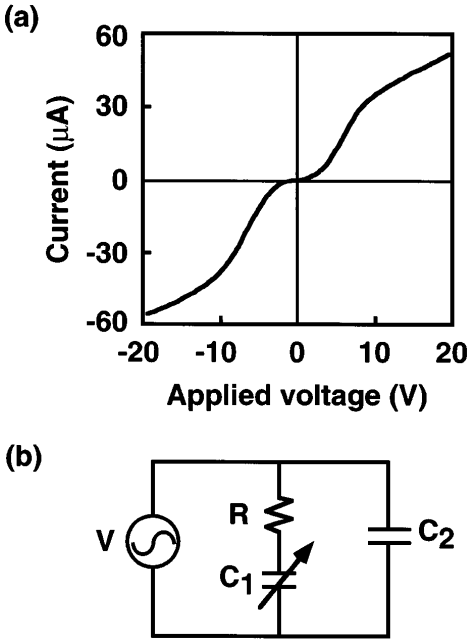

FIG. 1. (a) The dc I-V curve at room temperature for the sample S-10. (b) An electronic circuit analog of the superlattice system.

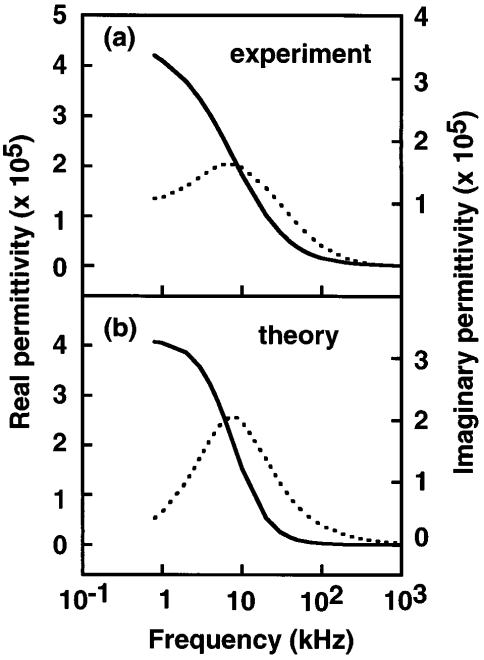

FIG. 2. (a) The measured real (solid line) and imaginary (dotted line) parts of the dielectric constant for the sample S-10 at $V_{ac} = 0$ V as a function of frequency on a logarithimic scale. (b) The calculated real (solid line) and imaginary (dotted line) parts of the dielectric constant at $V_{dc} = 0$ V as a function of frequency as a logarithmic scale.

Figure 1(b) shows an electronic circuit analog used in the analysis of the system response as described below. The result of the dielectric constant measurements as a function of frequency is shown in Fig. 2(a) in semi-log scale for the sample S-10. The real part (ε') of the dielectric constant (solid line) for S-10 has giant values approaching 420 000, and Debye-like frequency dispersion [12]. At high frequencies, ε' approaches the paraelectric-phase dielectric constant of about 750. As would be expected, ε' for the sample S-40 is about 750, and has no significant frequency dependence in the frequency range of 300 Hz–1 MHz. Figure 2(a) also shows the imaginary part (ε'') of the dielectric constant (dotted line) for S-10. For sample S-10, a broad peak for ε'' is observed in the frequency range corresponding to the largest dispersions for ε'.

Figures 3(a) and 4(a) show the measured variations of ε' and ε'', respectively, as a function of applied dc bias at three different ac signal frequencies of 0.5, 10, and 50 kHz. The excitation ac signal amplitude was kept at 0.01 V for all the frequencies used. The values of both ε' and ε'' are suppressed very strongly at high dc bias fields. The most rapid variations in the dielectric constants take place at or close to the threshold voltage observed in Fig. 1(a). Even though both ε' and ε'' are monotonically decreasing for most of the frequencies used, we note a complicated variation in ε'' as a function of dc bias voltage at low frequencies.

We propose a model based on the rigid-body motion of a domain wall lattice to explain the observations described above. This model reduces the motion to a single-particle type in a sinusoidal washboard potential [8,11]. The response of the superlattice under an electric field is obtained easily from an electronic circuit analog as shown in Fig. 1(b). In this circuit diagram, R represents the resistance for the screening current flow between the electrodes and the domain walls, C_1 is the capacitance associated with the polarization due to domain wall motion, and C_2 is the capacitance of the superlattice in the absence of domain walls. From the impedance measurements of the sample, the circuit parameters R, C_1, and C_2 can be determined. The dielectric constants are obtained from the capacitance values by using the approximate formula of Shiosaki *et al.* [13]. The expression for C_2 can easily be obtained by following the procedure given earlier [13] by substitution of the appropriate parameters for the sample S-10 and the interdigitated electrode pattern.

To determine C_1, we start with the equation of a rigid-body motion for a domain wall lattice in a sinusoidal potential. The equation of motion is given by

$$m\ddot{x} + \gamma\dot{x} + \frac{2\pi e_d Lh}{\lambda}\sin\frac{2\pi}{\lambda}x - LhP_sE = 0. \quad (1)$$

In Eq. (1), m and γ are the mass and the intrinsic damping parameters, respectively. x is the center-of-mass coordinate for a domain wall lattice [11]. e_d is the domain wall pinning energy per unit area, and L and h are the lateral dimensions of a domain wall. λ is the period of the pinning potential, and P_s is the value of the permanent polarization. E is the effective average field driving

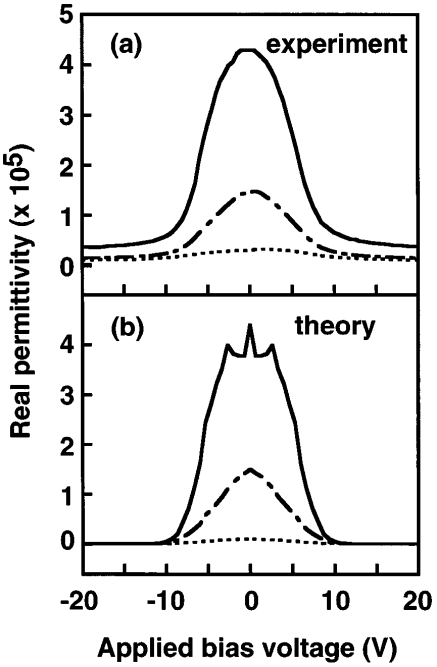

FIG. 3. (a) The measured ε' for S-10 as a function of applied dc bias at three different ac signal frequencies of 0.5 kHz (solid line), 10 kHz (dot-dashed line), and 50 kHz (dotted line). (b) The calculated ε' as a function of applied dc bias at three different ac signal frequencies of 0.5 kHz (solid line), 10 kHz (dot-dashed line), and 50 kHz (dotted line).

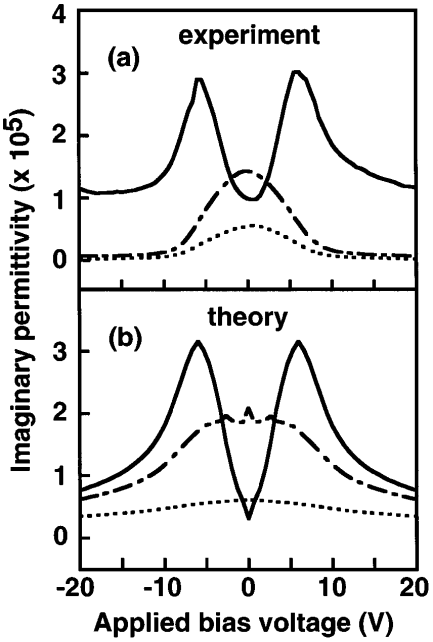

FIG. 4. (a) The measured ε'' for S-10 as a function of applied dc bias at three different ac signal frequencies of 0.5 kHz (solid line), 10 kHz (dot-dashed line), and 50 kHz (dotted line). (b) The calculated ε'' as a function of applied dc bias at three different ac signal frequencies of 0.5 kHz (solid line), 10 kHz (dot-dashed line), and 50 kHz (dotted line).

the motion determined by taking into account the field distribution on the superlattice [14] due to electrodes. It is expected that E is proportional to the applied voltage V between the fingers, with some proportionality constant a. In Eq. (1), the first and second terms can be ignored, since they will be important only at microwave frequencies.

The current due to domain wall motion is given by

$$I = P_s L \frac{dx}{dt} = P_s L \frac{dx}{dE}\frac{dE}{dt}. \tag{2}$$

In the presence of both an ac signal $V_{\rm ac}$ and a dc bias $V_{\rm dc}$ (with $V_{\rm ac} \ll V_{\rm dc}$), the capacitance C_1 can be expressed as

$$C_1 = C_{10}(1 - V_{\rm dc}^2/V_T^2)^{-1/2}, \tag{3}$$

where $V_T = 2\pi e_d/\lambda P_s a$ and $C_{10} = L\lambda P_s/2\pi V_T$. We note that V_T is the threshold voltage and C_{10} is the capacitance due to domain wall motion at $V_{\rm dc} = 0$ V.

The complex permittivity is determined by calculating the total admittance of the equivalent circuit shown in Fig. 1(b) and dividing by ωC_0. Here, ω is the angular frequency for the applied ac signal and C_0 is the capacitance of the interdigital electrode pattern in vacuum. C_0 is equal to 3.6×10^{-13} F for the electrode pattern used. ε' and ε'' are determined to be

$$\varepsilon' = \begin{cases} \dfrac{\varepsilon_1 + \varepsilon_2 + \varepsilon_2\tau^2\omega^2}{1 + \tau^2\omega^2} & \text{for } V < V_\tau \\ \varepsilon_2 & \text{for } V > V_\tau \end{cases} \tag{4}$$

and

$$\varepsilon'' = \begin{cases} \dfrac{\varepsilon_1\tau\omega}{1 + \tau^2\omega^2} & \text{for } V < V_\tau \\ \dfrac{\varepsilon_1}{1 + \tau\omega} & \text{for } V > V_\tau, \end{cases} \tag{5}$$

where $\tau = RC_1$ is the relaxation time for the polarization charge associated with the domain wall motion, $\varepsilon_1 = C_1/C_0$ is the dielectric constant due to domain walls, and $\varepsilon_2 = C_2/C_0$ is the dielectric constant in the absence of domain walls. We define the zero-frequency dielectric constant at $V_{\rm dc} = 0$ V as $\varepsilon_{10} = C_{10}/C_0$. Note that the domain wall contribution is purely capacitive for voltages below V_T and purely resistive above V_T. At threshold voltage V_T, τ becomes very large, leading to a divergence within the approximation made above. This behavior also leads to a divergent dielectric behavior as $\omega \to 0$. However, intrinsic damping and a distribution in V_T values would eliminate this divergence in real samples. A distribution in values of V_T is expected since a large volume is sampled during the measurement. Figure 1(a) supports this idea by showing a rounding at the threshold voltage.

We calculate ε' and ε'' as a function of ω and $V_{\rm dc}$ by using Eqs. (4) and (5) with an assumption of a Gaussian distribution for the values of V_T. In Fig. 2(b), the solid line and the dotted line show the calculated ε' and ε'', respectively, as a function of frequency for the sample S-10 at $V_{\rm dc} = 0$ V. We obtain good agreement with the measurements shown in Fig. 2(a) for the parameter values of $\varepsilon_{10} = 150\,000$, $\varepsilon_2 = 800$, and $R = 140\ \Omega$. In the

Gaussian distribution, the values used were 5 and 2 V for the average threshold V_{T0} and its standard deviation, respectively.

The pinning potential period can be expressed as

$$\lambda = \frac{\pi \varepsilon_{10} \varepsilon_0 V_{T0}}{P_s},$$

where ε_0 is the vacuum permittivity. We calculate λ as 41 ± 16 μm by using $\varepsilon_{10} = 150\,000$, $V_{T0} = 5$ V, and value of $P_s = 0.51$ C/m^2 for the polarization obtained from x-ray measurements. This value for λ is equal to the center-to-center electrode spacing within the error. From Eq. (3), we determine the domain wall pinning energy e_d as 0.33 ± 0.13 J/m^2 for sample S-10, a value very close to the calculated domain wall creation energy of 0.24 J/m^2 [1]. The values determined for λ and e_d suggest that the electrode pattern deposited plays a crucial role in controlling domain wall dynamics. Below the threshold voltage the domain wall lattice oscillates between neighboring electrodes. Pinning comes from the nucleation barrier to the creation of new domain walls.

Figures 3(b) and 4(b) show the calculated ε' and ε'', respectively, as a function of applied dc bias at three different ac signal frequencies of 0.5, 10, and 50 kHz by using the parameters determined previously. As can be seen, without any adjustable parameter, the agreement is reasonably good with the measurements presented in Fig. 3(a) and Fig. 4(a). The agreement is very good at low dc bias voltages. However, the deviation becomes significant at dc bias voltages higher than the threshold voltage. We suggest that this is due to the shape of the pinning potential not truly having a sinusoidal shape.

These experiments suggest a cornucopia of new measurements, including studies on the effects of temperature, doping, electrode geometry, and superlattice period. High dielectric constants up to 400 000 may be obtainable up to microwave frequencies by increasing the conductivity of the ferroelectric superlattices through impurity doping. Finally, the external control of domain wall dynamics in these material systems should open up some new device applications.

We would like to thank A. Zangwill for a number of helpful discussions. This work was supported in part by the NSF Low-Cost Electronic Packaging Research Center, and in part by ARPA.

*To whom all correspondence should be addressed.
†Current address: Advanced Devices/P. I. Department 1, Memory R&D Division, Hyundai Electronics Industries Inc., South Korea.

[1] B. S. Kwak, A. Erbil, B. J. Wilkens, J. D. Budai, M. F. Chisholm, and A. L. Boatner, Phys. Rev. Lett. **68**, 3733 (1992).
[2] B. S. Kwak, A. Erbil, J. D. Budai, M. F. Chisholm, L. A. Boatner, and B. J. Wilkens, Phys. Rev. B **49**, 14 865 (1994).
[3] A. L. Roitburd, Phys. Status Solidi (a) **37**, 329 (1976).
[4] R. Bruinsma and A. Zangwill, J. Phys. (Paris) **47**, 2055 (1986).
[5] B. Horovitz, G. R. Barsh, and J. A. Krumhansl, Phys. Rev. B **43**, 1021 (1991).
[6] J. S. Speck and W. Pompe, J. Appl. Phys. **76**, 466 (1994).
[7] J. Speck, A. Seifert, W. Pompe, and R. Ramesh, J. Appl. Phys. **76**, 477 (1994).
[8] G. Gruner, Rev. Mod. Phys. **60**, 1129 (1988).
[9] V. Ambegaokar and B. I. Halperin, Phys. Rev. Lett. **22**, 1364 (1969).
[10] Y. Kim, Y. H. Han, A. Erbil, and L. A. Boatner, in *Ferroelectric Thin Films IV*, edited by B. A. Tuttle, S. B. Desu, R. Ramesh, and T. Shiosaki, MRS Symposia Proceedings No. 361 (Materials Research Society, Pittsburgh, 1995).
[11] A. R. Bishop, B. Horovitz, and P. S. Lomdahl, Phys. Rev. B **38**, 4853 (1988).
[12] A. R. von Hippel, *Dielectrics and Waves* (The M. I. T. Press, Cambridge, 1954).
[13] T. Shiosaki, M. Adachi, S. Mochizuki, and A. Kawabata, Ferroelectrics **63**, 227 (1985).
[14] G. W. Farnell, I. A. Cermak, P. Silvester, and S. K. Wong, IEEE Trans. Sonics Ultrason. **SU-17**, 188 (1970).