Conduction Threshold, Switching, and Hysteresis in Quantum Dot Arrays

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We investigate low temperature transport in 200 × 200 arrays of GaAs quantum dots in which coupling between dots and electron density is controlled by a single gate. Current-voltage curves obey a power law above a threshold voltage with exponent ~1.5, and show discontinuous and hysteretic jumps in the current, or "switching events." Multiple switching events result in a hierarchy of hysteresis loops. Switching and hysteresis decrease with increasing temperature and disappear above 1 K. A possible mechanism for the hysteresis involving gate-to-dot tunneling is discussed.

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The nature of charging effects and electron-electron interactions are central to much of the recent experimental [1–3] and theoretical [4,5] work on semiconductor quantum dots. A very interesting and experimentally assessable system is a two dimensional array with adjustable coupling between the array elements. As discussed in recent theoretical studies [6,7], and as we will demonstrate experimentally, it is possible in this system to investigate possible collective effects in transport and their relation to the strength of dot-to-dot interactions. In particular, it has been predicted that arrays of quantum dots show a threshold for conduction due to the effects of disorder and Coulomb blockade [6].

In this Letter, we describe experiments on two dimensional quantum dot arrays where a single gate is used to form and control the barriers between the individual elements, as well as to change the density of the two dimensional electron gas (2DEG) [Figs. 1(a) and 1(b)]. As shown in Fig. 2, the current-voltage (I-V) characteristics of the arrays have two main features: a threshold for conduction and multiple switching events accompanied by hysteresis. These features are very similar in appearance to those observed in a variety of other strongly interacting systems, including sliding charge density waves (CDWs) [8] and magnetically induced Wigner solid (MIWS) systems [9]. By changing the gate voltage V_g, it is possible to move between the hysteretic and nonhysteretic regime. This also resembles the dynamics of the CDWs where switching and hysteresis are known to be highly temperature dependent [10,11]. In a control dot fabricated on the same chip, we also observed a single hysteresis loop accompanied by a single switching event. This is different than the behavior of most top-gated quantum dots studied so far, an exception being the hysteresis observed by Wu *et al.* [12] in double barrier lateral structures. In this case, hysteresis was attributed to electron heating once the current begins to flow through the device [13]. Because the hysteresis and switching in our arrays occurs for currents as low as 1.5 nA at voltages of 3.0 mV, that is, at picowatt levels of input power, we believe that electron heating is not the cause of hysteresis in our case. Instead, we propose that the hysteresis is associated with charge exchange in the form of a small leakage current to the gate in these structures. Since the I-V curves were repeatable within a cooldown and stable during very slow sweeps, we believe these effects are not related to changes in occupation of impurity states.

Arrays of 200 by 200 dots were fabricated using a standard modulation doped GaAs/$Al_{0.34}Ga_{0.66}As$ 2DEG structure with an electron mobility of ~200 000 $cm^2/V\,s$ and a sheet density of 3.5×10^{11} cm^{-2} at 4.2 K. The 2DEG layer is 770 Å below the surface consisting of a 300 Å AlGaAs spacer above the 2DEG, a 170 Å Si doping layer ($N_D = 3.8 \times 10^{18}$ cm^{-3}), and a 300 Å undoped GaAs cap layer. To form the dots, "plus sign" patterns with a spatial period of 0.8 μm [Fig. 1(b)] were formed by electron-beam lithography and subsequent wet etching roughly 800 Å deep, through the 2DEG layer. We use a single Cr/Au gate deposited over the entire array as

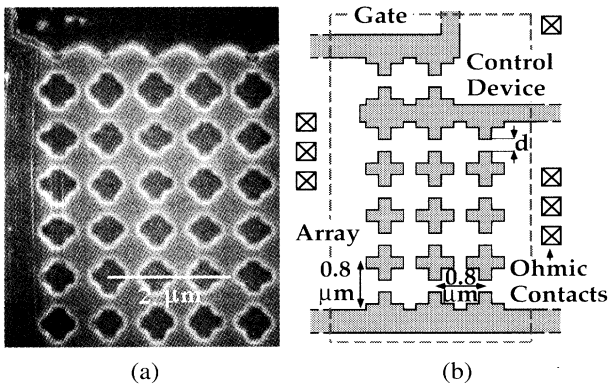

FIG. 1. (a) Electron micrograph of part of the 200 × 200 array. Electron gas is removed beneath darker regions; channels between dots can be depleted with a gate voltage in the range −40 to −150 mV depending on the device. (b) Schematic shows the layout of the array, control device, and Ohmic contacts. The lithographic distance "d" is 300, 250, and 200 nm for device 1, 2, and 3, respectively.

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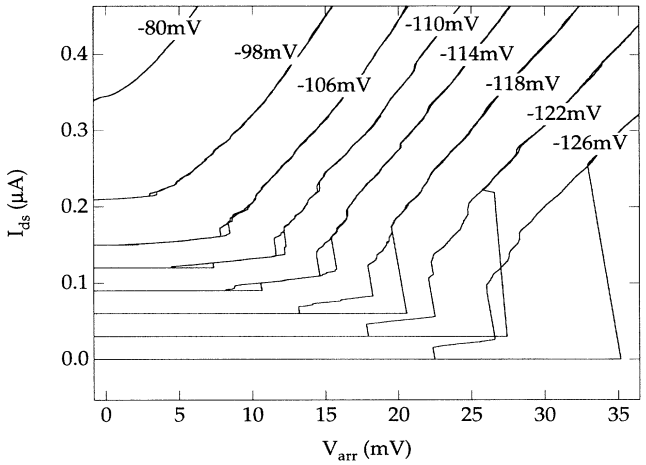

FIG. 2. Typical I-V curves for several gate voltages (device 2) measured at base temperature ($T \sim 20$ mK). The curves are offset in proportion to gate voltage (V_g) for clarity. V_{arr} is the voltage measured directly across the array in a four-lead configuration.

well as over an isolated control dot which has the same dimensions as each individual array element (Fig. 1). A small negative voltage ($|V_g| \lesssim 300$ mV, typically) constricts the barriers by increasing the lateral depletion and raising the potential in the barrier. This greatly increases barrier resistances between the dots without producing large density changes within the dots (roughly 630 mV is necessary to fully deplete the 2DEG).

The devices were measured in a dilution refrigerator at mixing chamber temperature from 20 to 700 mK. A dc voltage bias which could be swept, plus a 10 μV, 11.4 Hz ac voltage bias were applied across the array. The voltage dropped across the array (V_{arr}) was measured using two other Ohmic contacts. The ac lock-in measurement directly gives differential conductance dI_{ds}/dV_{arr} as a function of V_{arr}. In practice, however, the dc I-V measurements were quite clean and sufficiently characterized the observed behavior. We will therefore focus on the dc results here. In order to symmetrize the I-V, the gate voltage was referenced to the midpoint of the source-drain voltage by means of two 10 kΩ resistors.

Figure 2 shows general I-V curves as a function of the gate voltage V_g. These curves illustrate typical multiple hysteresis loops as a function of the interdot coupling adjusted by the gate. For $V_g = -98$ mV, the I-V curve has a single loop near 4 mV bias voltage. As the gate voltage becomes more negative, the width of this loop increases and a new hysteresis loop appears for $V_g < -106$ mV. These two loops merge at a gate voltage between -114 and -118 mV. Figure 2 also illustrates the discontinuous jumps in the current (within the resolution of a single data point), which we will refer as "switching events." In the curves for $V_g < -118$ mV, multiple switching events occurring in a single loop can be noticed very clearly. In all hysteresis loops observed, the switching-on voltage for increasing V_{arr} is larger than the switching-off voltage when V_{arr} is decreased, that is, all hysteresis loops are counterclockwise in I vs V. We also find counterclockwise subloops on both the upper and lower parts of the curve if the sweep direction is reversed following a current jump.

Figure 3 shows that switching voltages decrease for increasing temperature, and the width of each hysteresis loop also decreases as the temperature increases. It is possible to see in Fig. 3 the dissociation of big loops into smaller ones and their disappearance at different temperatures lower than ~700 mK. There is also an apparent trade off between gate voltage and temperature: At 700 mK, the hysteresis can be recovered if the gate voltage is made 20–30 mV more negative. However, the ratio of the loop width to the switching voltage is always smaller than that at 20 mK. This suggests that switching and hysteresis will inevitably disappear at sufficiently high temperatures regardless of gate voltage. Indeed, at 4.2 K, we observe no hysteresis at all in any of the samples.

We also investigated the I-V properties of the single control device located adjacent to the array on each sample, using the same experimental measurement configuration as for the arrays (Fig. 4). In the case of a single dot, we observe no hysteresis near pinch off ($V_g \sim -375$ mV), however, beyond a gate voltage ~20 mV more negative than this pinch-off value, a single hysteresis loop appears accompanied by upward and downward switching events. Here we define pinch off as the regime where the device (array or single dot) has negligible

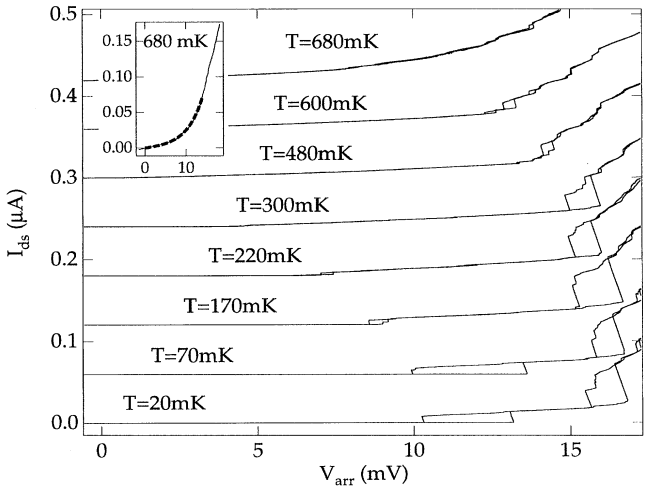

FIG. 3. I-V curves (offset for clarity) for device 2 at $V_g = -115$ mV at various temperatures. Inset shows finite conductance around zero bias for higher temperature data ($T = 680$ mK) (solid curve) on enlarged vertical scale, along with a two-parameter fit by the activated form $I_{ds} = K_1 \sinh(K_2 V_{arr})$ (dashed curve). Fit gives $K_1 = 3.4$ nA and $K_2 = 0.27$ mV^{-1}.

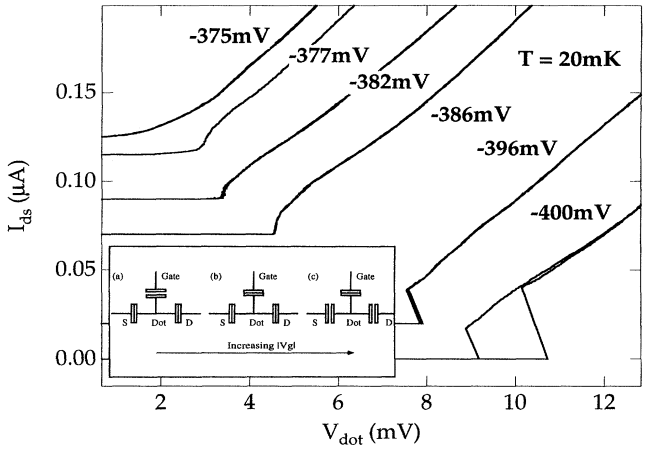

FIG. 4. *I-V* curves for the single dot (control device 2), at various gate voltages V_g. The curves are offset in proportion to gate voltage for clarity. The inset is the schematic illustration of expected change in dot-dot and dot-gate transparencies as a function of gate voltage. At $V_g = 0$, the resistive coupling between dots is large. As the gate voltage becomes more negative dot-dot transparency decreases (a), and, after a crossover (b), the gate-dot transparency can become greater than the dot-dot transparency (c). In this last situation, there is non-negligible resistive coupling between the gate and dots.

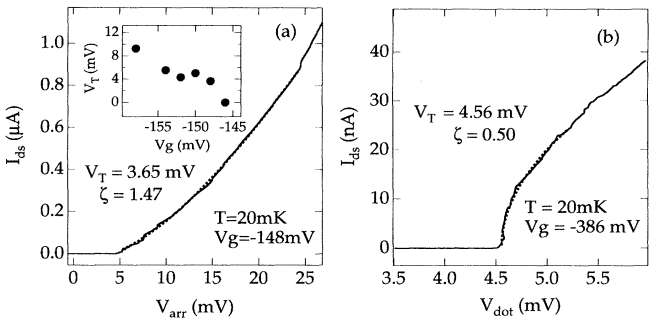

FIG. 5. (a) *I-V* curve of array (device 1) near threshold (solid curve) along with three-parameter fit to the power law $I_{ds} = C(V - V_T)^{\zeta}$ (dashed line) giving $\zeta = 1.47$. Inset shows threshold voltage V_T as a function of gate voltage V_g; power law exponents were $1.4 < \zeta < 1.7$ over this range of V_g. (b) *I-V* curve of single dot (control device 1) near threshold (solid curve) along with three-parameter fit by the power law $I_{ds} = C(V - V_T)^{\zeta}$ (dashed line) giving $\zeta = 0.50$.

conductance near zero bias, i.e., the *I-V* curve has zero slope at the origin. The *I-V* curve for the single dot has a very weak temperature dependence compared to the array, and the width and location of the hysteresis are unchanged up to 700 mK. As in the array, no hysteresis is seen at 4.2 K for any gate voltage. Unlike the arrays, no subloops or multiple switching events are observed in the single dot. Although the lithographic dimensions of the single dot and array are nominally identical, in all cases, pinch off of the single dot occurs at a considerably larger gate voltage than for the array. We do not know at present if this difference is due to the details of the device design and fabrication, or whether it results from a significant dot-dot interaction.

We next discuss an important difference in the curvatures of the *I-V* characteristics of the arrays vs single dots: The *I-V* curves for the arrays are concave up above a threshold, while for the single dots they are concave down above a threshold. More quantitatively both the array and single dot *I-V* curves can be very well fitted with a power law dependence $I_{ds}C(V - V_T)^{\zeta}$, where V_T is a threshold voltage. This form works especially well when the gate voltages are such that the array (or single device) is pinched off but there is yet no hysteresis. For the arrays, this corresponds to a range of gate voltages 2–3 mV more negative than the pinch-off voltage. In this region, ζ for the array is in the range 1.4–1.7 [Fig. 5(a)]. The threshold voltage increases as the gate voltage is made more negative, as shown in the inset of Fig. 5(a). Even when hysteresis is present (at slightly more negative gate voltages) the overall array *I-V* curve remains concave up, with a similar power law dependence with small hysteresis loops and switching events superimposed. For even more negative gate voltages, hysteresis becomes well developed and the exponent ζ decreases towards 1. Theoretically, an *I-V* dependence with an exponent $\frac{5}{3}$ has been predicted for 2D quantum dot arrays by Middleton and Wingreen [6] for small capacitive coupling between the dots, which is the nonhysteretic regime. Our results are consistent with this prediction. The authors also found an increase in the threshold voltage with smaller capacitive coupling between the dots. Experimentally, as the gate voltage is made more negative, the capacitive coupling between the dots decreases and the threshold voltage increases, also consistent with their results.

With increasing temperature, the threshold voltage decreases as seen in Fig. 3. Also, for sufficiently high temperature, the conductance around zero bias becomes finite with an activated form $I_{ds} \propto \sinh(\text{const} \times V_{arr})$. For device 2 at $V_g = -115$ mV (Fig. 3) a small finite conductance around zero bias appears above ~300 mK. Between ~300 and 600 mK this activated conductance continues to be accompanied by a rapid (superexponential) increase of current around $V_{arr} \sim 12$ mV. However, above 600 mK, this sharp turn-on is washed out and the activated form describes the *I-V* curve over the full range $|V_{arr}| < 15$ mV.

For the single dot, the same form of power law $I_{ds} = C(V - V_T)^{\zeta}$ is also observed in the range of gate voltages between the pinch off and the hysteretic regime. For these gate voltages, the array and single dot threshold voltages (V_T) are of the same order of magnitude. We believe that, because of the inherent disorder in the array and the exponential dependence of the tunneling current on barrier height and shape, a large fraction of the applied voltage will be dropped across a few dots, which constitute bottlenecks

to the flow of current. Therefore, the threshold voltage per dot in the array may be comparable to that of the single dot when one considers only those dots with significant voltage drops rather than all dots across the array.

For the single dot $\zeta \sim 0.5$ [Fig. 5(b)] near threshold, and the I-V curve becomes concave up only at high bias voltages (Fig. 3). The concave down shape near threshold ($\zeta \sim 0.5$) is not found at higher temperatures ($T \sim 4.2$ K), and at the same time the possibility for hysteresis at any V_g is also eliminated. There is an intriguing similarity between these experimentally observed exponents for the single dot ($\zeta \sim 0.5$) and the array ($\zeta \sim 1.5$), and those in the sinusoidal washboard potential model used to explain the I-V characteristics of pinned CDWs [8]. For a single degree of freedom the CDW model gives $\zeta = \frac{1}{2}$ [8], while the mean field model with many degrees of freedom gives $\zeta = \frac{3}{2}$ [14].

To address the cause of the hysteresis, we consider a model of a semiconductor quantum dot that includes a weak resistive coupling from the 2DEG to the gate shown in Fig. 4, inset. We believe this coupling is particularly important in our samples because the dots are formed by wet etching with a gate that fills in the etched regions. This allows high resistance (typically $\sim 10^8$ Ω) barriers to form along the sidewalls of the dots. At $V_g = -100$ mV a gate current of ~ 75 pA is measured for the deep etched devices (1, 2, and 3) reported here. In other shallow-etched samples, which in general did not show hysteresis, a typical gate current of ~ 1 pA was measured at the same gate voltage. The mechanism by which a conducting path from the gate to the dot can induce hysteresis has been analyzed recently in a model of a single electron transistor (SET) coupled to a controlling potential (V_g here) through a series resistor R_0 and a capacitor C_g [15]. This model, known as the RC-SET, gives hysteresis in the limit of large coupling resistance to the controlling potential. In making this comparison, our gate-to-dot resistance $R_0(V_g)$, which increases with more negative V_g in our devices, corresponds to the coupling resistance R_0 in Ref. [15]. Experimental parameters for both the arrays and the single dots [$R_0(V_g) \gtrsim 10^8$ Ω, tunnel barriers $R_1(V_g), R_2(V_g) \gtrsim h/e^2$] are in the range where the RC-SET model predicts hysteresis $R_0(V_g) \gg (R_1 + R_2)C_\Sigma/C_g \gg h/e^2$ (C_Σ is the total capacitance of the dot). This model suggests that a dot in an array which is in isolation would not be hysteretic can be pushed into the hysteretic regime by the impedance of its neighbors, which effectively raises R_1 and R_2 for that dot. The connection between hysteresis and switching and a nonzero gate-to-2DEG current is also suggested by a model of controllable switching in CDWs, in which switching and hysteresis are induced by coupling the CDW to the background of uncondensed electrons [16]. We note, however, the microscopic mechanism leading to hysteresis and switching in CDWs remains controversial. Indeed, we believe that the simple and controllable nature of quantum dot arrays provides a useful new system in which to experimentally explore general models for continuous and discontinuous depinning transitions in CDWs and other nonlinear systems. Further detailed studies of the observed hysteresis and its connection to the RC-SET model [15] will be presented in subsequent publications.

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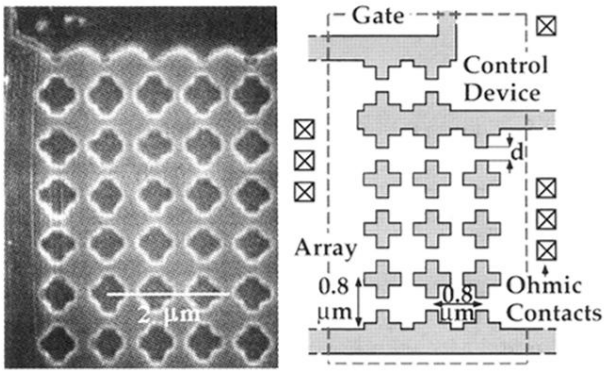

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