Single-Electron Charging Effects in Insulating Wires

Venkat Chandrasekhar, Zvi Ovadyahu,[a] and Richard A. Webb
IBM Research Division, T. J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598
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We present measurements of the transport properties of 0.75-μm-long, narrow, insulating indium oxide wires and rings. These devices have no apparent tunnel barriers, yet they exhibit effects similar to those found in series arrays of very-small-capacitance tunnel junctions: highly nonlinear *I-V* characteristics and a zero-bias conductance which is periodic in a voltage applied by means of a lateral gate. These effects are due to the influence of single-electron charging on transport through localized states in the insulating regime.

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Experiments on artificially fabricated arrays of nanometer-size tunnel junctions have attracted a great deal of interest in the past few years [1]. If the capacitance C of these tunnel junctions is small enough that the energy $E_C = e^2/2C$ required to transfer an electron across a junction is much larger than the thermal energy $k_B T$, new features in the transport properties are observed. The dc *I-V* curves of these arrays are found to be highly nonlinear, with a threshold voltage $V_t \sim 0.1$–0.5 mV below which essentially no current flows through the array. In addition, the zero-bias conductance is a periodic function of a voltage applied by means of a lateral gate. Similar effects have been observed in "squeezable" tunnel junctions formed at the interface of two crossed wires [2], in the tunneling of electrons through a single metallic grain using a scanning tunneling microscope [3], and in one-dimensional (1D) Si and GaAs devices [4,5]. In all these systems, electron conduction is strongly affected by the influence of single-electron charging on transport of electrons across a potential barrier.

In this Letter, we present measurements of the transport properties of short indium oxide rings and wires formed between two metallic contacts. These devices have no apparent tunnel barriers; yet, for samples with resistances greater than ~ 60 kΩ, their behavior is strikingly similar to a series array of two or more small-capacitance tunnel junctions. We observe in our devices both the effects mentioned above: a highly nonlinear *I-V* characteristic, with threshold voltages V_t typically on the order of 0.5 mV, and a zero-dc-bias conductance which is periodic in a voltage applied by means of a lateral gate. In some respects, these features in our samples are far more robust than those found in the tunnel junction arrays. We have observed threshold voltages as large as ~ 3.0 mV, and hundreds of periodic oscillations in many of our samples which persist up to temperatures greater than 10 K. Numerical calculations which model our devices as arrays of junctions reproduce most of the features seen in our data.

A schematic of a typical device is shown in Fig. 1(a). The first level of *e*-beam lithography on oxidized Si wafers is used to generate a liftoff pattern for both the gate and sample, over which *e*-gun evaporated indium oxide is deposited in a partial oxygen atmosphere. As deposited, the samples are in an amorphous state. After liftoff, some of our samples are crystallized by heating in air at a temperature of about 400 °C. Gold contact pads are evaporated over the sample through a second *e*-beam liftoff mask. The sample length is 0.75 μm, and the gate is separated from the wire (or one arm of the ring) by ~ 0.1 μm. The widths of the insulating wires used in our studies vary from 30 to 150 nm, and the average diameter of the rings is 0.3 μm.

Despite the presence of large crystal grains, the electrical conductivity of our samples at low temperatures is characteristic of an insulator due to disorder and deviations from stoichiometry [6]. The strong disorder produces a fluctuating random potential which localizes the electrons. In two-dimensional (2D) films, this leads to a temperature dependence of the resistance which is characteristic of Mott variable-range hopping between localized states [7]. In 1D samples, the hopping process is strongly influenced by single-electron charging effects. If we model our devices as arrays of small-capacitance tunnel junctions, where single-electron charging effects are important, we can account for many of the phenomena we observe. The assumption of the model is that the electrons traverse the device via an electron state in an isolated segment in the middle of the sample. We can think of this segment as equivalent to an intermediate metallic electrode in a series array of small-capacitance tunnel junctions. Figure 1(b) illustrates the simplest case of two junctions with one intermediate electrode. Transport across such an array strongly depends on the charge on

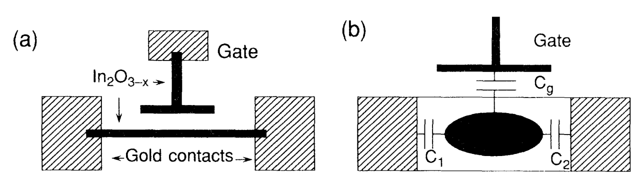

FIG. 1. (a) Schematic of one of our line samples, showing the Au contact pads, In_2O_{3-x} wire, and gate. The length of the devices is 0.75 μm, the linewidths range from 60 to 120 nm, and the gate is separated from the wire by ~ 100 nm. (b) Tunnel junction model of the insulating wire. The solid ellipse represents an isolated segment in the indium oxide.

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each junction [1]. If the charge Q on each junction is an integral number N of charge quanta, transfer of electrons is forbidden unless the energy of the electron exceeds the Coulomb energy E_C. If $Q=N+\frac{1}{2}$ charge quanta, then it costs no energy to transfer an electron across the junction. For intermediate values of Q, the excess energy ΔE required to transfer an electron across is between these two extrema. This implies that, at temperatures $k_BT \ll E_C$, there is a threshold voltage $V_t=\Delta E/e$ below which essentially no current flows through the device. V_t will vary from zero to a maximum of E_C/e, depending on the charge on the junctions. The zero-bias conductance of the array also depends on Q, being a minimum when $Q=N$ charge quanta and maximum when $Q=N+\frac{1}{2}$ charge quanta.

The charge on each junction can be varied *continuously* by changing the voltage on a nearby gate electrode which is capacitatively coupled to the center electrode of the array. This redistributes the charge on the different interfaces of the electrode, and the charge on each junction. As the gate voltage is changed by more than $\Delta V_g = e/C_g$ (where C_g is the capacitance of the gate to the center electrode), an additional electron is pulled to (or expelled from) the electrode, and the whole process is repeated again. Thus, for a two-junction array, both V_t and the zero-bias conductance are periodic functions of the gate voltage, with period ΔV_g [1]. For more than two junctions, additional periods may be evident, corresponding to the capacitance of the gate to different intermediate electrodes. In this case, although V_t will still be periodic in V_g, it may never entirely vanish. This is because, given the different capacitance of the gate to each electrode, varying V_g may lift the Coulomb blockade for one capacitor, but may not change the charge distribution enough to lift the blockade for the other capacitors in the array.

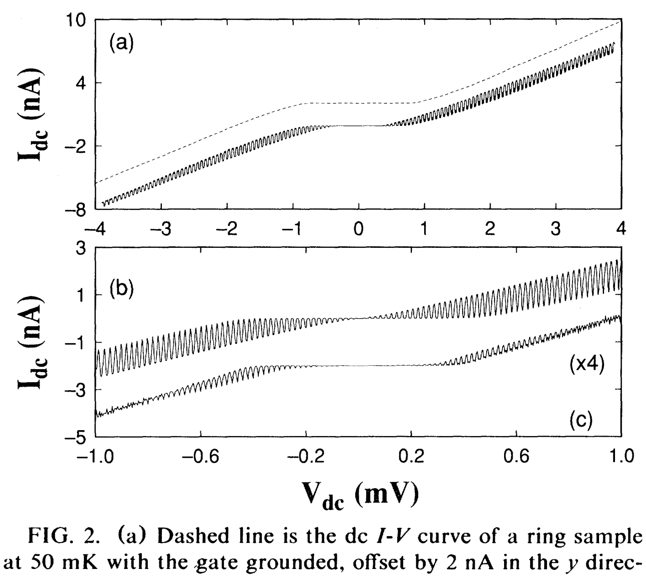

FIG. 2. (a) Dashed line is the dc I-V curve of a ring sample at 50 mK with the gate grounded, offset by 2 nA in the y direction for clarity. Solid line is the I-V curve for the same sample with a ± 5-mV ac voltage applied to the gate electrode at a frequency of 3 mHz, while the dc voltage is linearly increased at a frequency of 13 μHz. (b) dc I-V curve of a line sample at 40 mK with the voltage on the gate modulated as above. (c) Simulation of the I-V curve of a three-junction array at 100 mK using the algorithm of Ref. [9].

The dashed curve in Fig. 2(a) shows the dc I-V curve of one of our ring samples. This is a classic Coulomb blockade I-V characteristic, with a threshold voltage $V_t \sim 0.8$ mV, corresponding to a sample capacitance of $C \sim 10^{-16}$ F ($V_t=e/2C$). V_t can be controlled by varying the gate voltage V_g. To obtain a complete picture of the I-V characteristics, we modulate V_g rapidly at $\pm \Delta V_g/4$ while sweeping the dc voltage across the device [8]. The resulting dc I-V curve is shown in Fig. 2(a). For this sample, V_t always remains finite ($\gtrsim 0.2$ mV), suggesting that the gate is modifying charge on only part of the sample. For other samples, we can modulate V_t to zero by changing V_g [Fig. 2(b)]. Figure 2(c) shows the result of a numerical simulation for a series array of three unequal capacitance junctions with $\pm \Delta V_g/4$ modulation applied to the gate, using the algorithm of Bakhvalov *et al.* [9] and Glazman and Chandrasekhar [10]. Here also V_t is always greater than zero, as we are modifying the charge on only part of the entire array. Note that for both the experimental data in Figs. 2(a) and 2(b), and the simulation of Fig. 2(c), the current through the sample is still a strong function of V_g even far above V_t, where one would normally expect the Coulomb blockade to be suppressed.

Figures 3(a)–3(c) display the V_g dependence of the zero-bias conductance of three different samples at low temperatures, and demonstrate the wide variety of sample

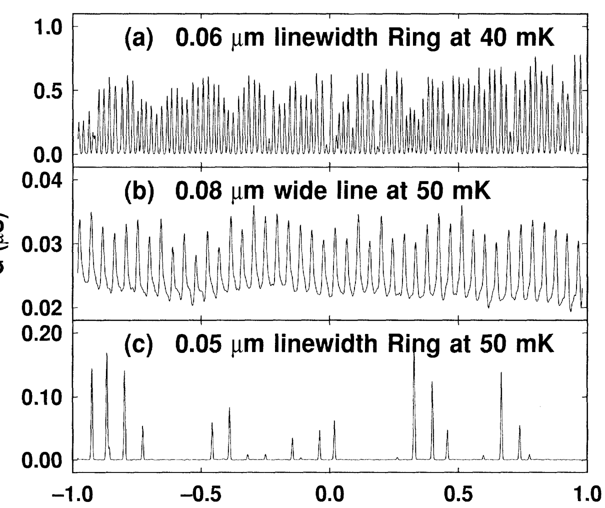

FIG. 3. (a)–(c) The gate voltage dependence of the zero-bias conductance of three samples, measured with a 2-μV, 10-Hz ac voltage bias.

specific behavior we have found in all our samples. The first two samples show clear periodic conductance oscillations as a function of V_g. In both samples, the oscillations persist up to $V_g = \pm 10$ V. The amplitude of the oscillations are temperature independent below 100 mK, and decrease rapidly as the temperature is increased. In some samples, the oscillations persist up to 12 K, with only a slight shift in period observed above 5 K. Figure 3(c) demonstrates a second type of behavior we frequently observe. In this sample, the amplitude of some of the conductance peaks becomes temperature independent at low temperatures. The amplitude of other conductance peaks, however, decreases with the temperature down to our lowest temperatures, obscuring the periodic nature of the oscillations. At higher temperatures the periodicity is recovered, but occasionally there appear to be additional periods in the data. Additional periods are most frequently seen in doubly connected devices such as rings, but are also present in about 30% of our single-line samples [11]. These observations are culled from data taken on over a hundred samples.

Figures 4(a) and 4(b) show the result of our simulations of the conductance as a function of V_g for series arrays of two and three unequal-capacitance tunnel junctions, respectively [10]. For two junctions, all conductance maxima become temperature independent at low temperatures, similar to the sample of Fig. 3(a). This suggests that, in this sample, a single large segment is determining electron transport. The period ΔV_g of the oscillations is related to the capacitance C_g of the gate to the segment by $\Delta V_g C_g = e$. For the sample in Fig. 3(a), $\Delta V_g \sim 20$ mV, giving $C_g = 8 \times 10^{-18}$ F. We can estimate the geometric capacitance C_T of the gate to the entire device, taking into account the dielectric properties of both the Si wafer and the 0.5-μm SiO_2. The ratio C_g/C_T is then an estimate of the size of the segment compared to the total size of the sample. For the sample in Fig. 3(a), $C_g/C_T = 0.82$, i.e., the segment comprises 80% of the sample. For the sample in Fig. 3(c), $C_g/C_T = 0.3$, implying that the size of the segment determining the oscillations is only 30% of the sample size. In this case, more than one segment is likely. For a sample with a single segment, we expect the conductance peaks to become temperature independent at low temperatures, while the conductance valleys should show an activated temperature dependence with the same activation energy for each valley, as we find for the sample of Fig. 3(a). For multiple-segment samples, the temperature dependence of the peaks and the valleys is determined by electron transport across multiple energy barriers of different heights [12]. These energy barriers change as a function of the gate voltage; thus, the temperature dependence of adjacent peaks and adjacent valleys can be vastly different. The simulation in Fig. 4(b) demonstrates that the assumption of two segments of different size, corresponding to three junctions in series, reproduces qualitatively the features seen in Fig. 3(c). The temperature dependence of the conductance valleys of the sample in Fig. 3(b) is anomalous—these valleys show a finite-temperature-independent conductance at low temperatures. We speculate that this may be due to parallel conduction paths or a resonant-tunneling-type process, but at present have no definite explanation for this observation. The temperature dependence of the conductance oscillations in our samples is complicated, and will be discussed in detail in a future publication. In any case, it is interesting to note that the temperature dependence of these samples is definitely not that expected from 1D Mott variable-range hopping. Even the conductance averaged over a large range in V_g is simply activated, in contrast to the $\exp[-(T_0/T)^{1/2}]$ expected for 1D Mott variable-range hopping.

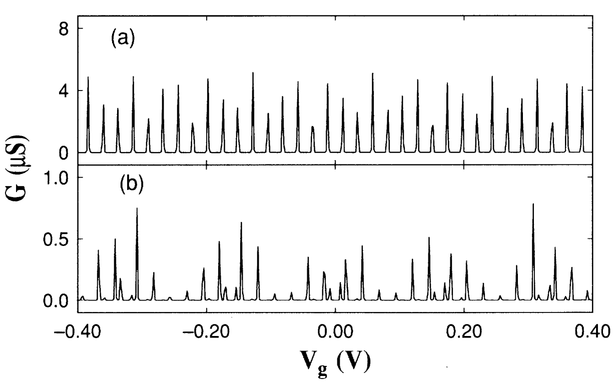

FIG. 4. (a) Numerical simulation of the gate voltage dependence of the zero-bias conductance of a two-junction array, using the algorithm of Ref. [9]. The temperature is 50 mK. (b) Numerical simulation of the gate voltage dependence of the conductance for a three-junction array, at 50 mK.

We have seen how the transport properties of our insulating wires and rings are characteristic of an array of small tunnel junctions where single-electron charging effects play a dominant role in the transport of electrons across the device. The question that naturally arises is: What forms the junctions in the insulating devices? One possibility is that the junctions are formed at the interfaces of crystal grain boundaries in our polycrystalline samples. However, even our amorphous samples, which have no crystal grains, show both nonlinear I-V curves and conductance oscillations. Moreover, crystalline samples whose resistance is less than ~ 60 kΩ at room temperature do not show Coulomb blockade effects. Indeed, for a crystalline sample which shows Coulomb blockade effects, we can induce a transition to a non-Coulomb blockade regime merely by lowering its electrical resistance, by either heat treatment or exposure to ultraviolet (uv) radiation. Either method reduces the degree of localization without affecting the grain size [6]. These observations suggest that it is not the polycrystalline nature of the devices which is responsible for the Coulomb blockade effects. For the same reason, other geometrical properties, such as variations in the linewidth of the sample [13], cannot be the source of these effects.

For the 1D Si and GaAs devices of Ref. [5], it has been proposed [14,15] that the presence of a few impurities cause large fluctuations in the underlying electrostatic potential which leads to the formation of effective tunnel barriers for the electrons. For the Si and GaAs devices, the distance between barriers is thought to be $\sim 0.5-1.0$ μm [5]. In In_2O_{3-x}, the potential fluctuates on a length scale of a few nanometers [6]. This would mean we would have $\sim 10^2-10^3$ separate segments in a 0.75-μm wire, yet the interpretation of data from some of our samples indicates that only one or perhaps two segments are present.

For the analogy with the tunnel junction model to be valid, there must be a spatially localized region within the indium oxide to which multiple charges can be added or subtracted. Within each such region or segment, the localized electronic states are more closely coupled to each other than to states in other sections of the sample, from which they are separated by effective tunnel barriers. These segments can be quite large: From the electron density ($\sim 4\times 10^{25}/\mathrm{m}^3$) and our earlier estimate of the size of a segment (which is roughly on the order of the localization length [6]), the number of electrons in each segment is on the order of 2.2×10^4, consistent with the large number of oscillations observed. The physics that separates our samples into these isolated segments remains unclear, but we believe that any explanation must involve the intrinsic disorder present in the system.

In conclusion, we have observed nonlinear *I-V* characteristics and conductance oscillations in high-resistance In_2O_{3-x} wires and rings that appear to be closely related to Coulomb blockade effects seen in tunnel junction arrays. These effects are observed in both crystalline and amorphous samples over a wide range of sample widths. The two most important criteria for the existence of these effects are that the sample resistance be larger than 60 kΩ, and that the thermal energy be much less than Coulomb blockade energy. The magnitude of the Coulomb blockade energy appears to depend on the microscopic details of the disorder in In_2O_{3-x}, suggesting that the localized states in the indium oxide are important in understanding the physics of these devices.

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[a]Permanent address: Racah Institute of Physics, The Hebrew University, Givat Ram, Jerusalem 91904, Israel.

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