Experimental Evidence for Relaxation Phenomena in High-Purity Silicon

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Experimental evidence of relaxation phenomena associated with majority-carrier depletion has been observed for the first time in a high-purity semiconductor. It has been demonstrated in the low-temperature current-voltage (*J-V*) characteristics of a silicon diode. The material changes from the lifetime to the relaxation regime when the temperature is decreased from 300 to 14 K. A change in the shape of the *J-V* curve, manifested by increased conductance at low bias, is observed and is in good agreement with recent theoretical modeling of minority-carrier behavior in relaxation semiconductors.

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The transport behavior of a solid under nonequilibrium conditions provides fundamental insight into the dynamical response of the system. Almost thirty years ago, van Roosbroeck proposed that two fundamental regimes of behavior could exist for a semiconductor material which is excited by free-carrier injection.[1] In the subsequent development of this concept,[2,3] the term "lifetime regime" was used to describe the regime of semiconductor behavior in which the free-carrier lifetime τ_0 is longer than the dielectric relaxation time τ_D and "relaxation regime" was used to designate the opposite case, $\tau_D > \tau_0$. Although historically most semiconductor research has dealt with low-resistivity material and hence with the lifetime regime, there are a variety of cases, such as semi-insulating and trap-dominated material, large band-gap semiconductors, amorphous semiconductors, and high-purity materials at low temperature, for which the relaxation category is the appropriate one.

Over the past two decades, extensive theoretical work has been done to demonstrate that in the relaxation regime, under nonequilibrium conditions, the assumption of space-charge neutrality is not valid. This leads to predictions of both steady-state and transient transport behavior that is fundamentally different from the more common lifetime regime. Much of the analysis has dealt with the topic of minority-carrier injection into materials which either due to high intrinsic resistivity or high trap populations could, based on their lifetimes and resistivities, be classified as relaxation semiconductors.[4-6] It is not important how the nonequilibrium situation is induced, although solutions to the full set of transport equations will depend on the appropriate boundary conditions.

Experimentally, injection through contacts, either *p-n* junctions or Schottky barriers, or illumination are obvious choices to achieve minority-carrier injection. The relaxation regime of semiconductor behavior has not, however, been as extensively explored experimentally as theoretically. Queisser *et al.*[7] analyzed the current-voltage (*J-V*) characteristics of a *p-n* junction in high-resistivity GaAs, and Illegems and Queisser[8] later performed more extensive measurements in response to controversy regarding the relaxation theory. At the heart of the debate was the role that minority-carrier injection should play with regard to local conductivity near an injecting boundary. Unlike the standard lifetime case, minority-carrier injection into a relaxation semiconductor should lead to majority-carrier depletion through recombination. The goal of the earlier experimental work was to determine the effect of majority-carrier depletion on the *J-V* characteristic of semi-insulating GaAs.

Recent numerical modeling of the governing macroscopic transport equations for minority-carrier injection predicts that the *J-V* characteristic of a trap-free p^+-*i*-n^+ structure in the relaxation regime will actually show a higher effective conductance at low voltages and a lower conductance at higher voltages than a similar structure in the lifetime regime.[6] These new results indicate that earlier experimental work in GaAs does not provide direct proof for relaxation behavior, since the presence of a significant population of midgap traps, which pin the Fermi level in these materials, can actually lead to behavior more typical of conventional lifetime semiconductors.

In this work, the effect of minority-carrier injection in a high-purity semiconductor material at low temperature was studied to observe behavior characteristic of the relaxation regime. The *J-V* characteristics of a high-purity floating-zone Si n^+-*p*-p^+ diode have been measured as a function of temperature. The silicon changes from the lifetime to the relaxation regime upon cooling because the resistivity increases as the free-carrier concentration decreases exponentially due to the freezeout of shallow acceptor levels. The goal was to observe experimentally the theoretically predicted transition in the *J-V* characteristic and to demonstrate relaxation behavior in a material in which space charge is not dominated by midgap traps.

The silicon devices were n^+-*p*-p^+ radiation detectors designed and fabricated at the Lawrence Berkeley Labo-

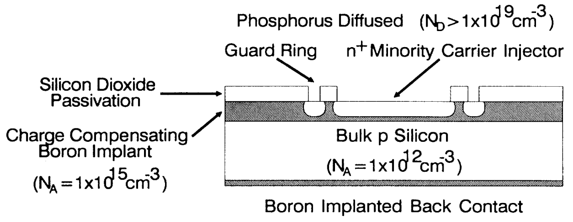

FIG. 1. Schematic cross section of Si diode.

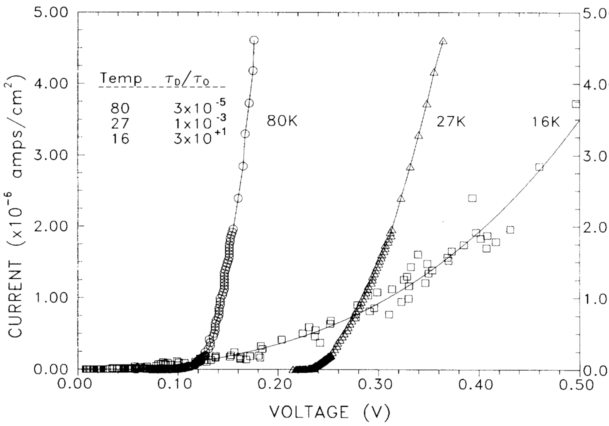

FIG. 2. Low-current-range *J-V* data for n^+-*p* Si diode as a function of temperature.

ratory.[9] A cross-sectional schematic is shown in Fig. 1. The material was floating-zone high-purity Si with a room-temperature resistivity of 4000–6000 Ωcm. The net shallow-acceptor concentration (primarily boron) was 2×10^{12} cm^{-3}. The total diode thickness was 380 μm. The injecting contact was a 0.5-μm n^+ region created by phosphorus diffusion. The back contact was made by 25-keV boron implantation, followed by Au evaporation for mechanical mounting and soldering. The injecting contact (area $=5\times10^{-2}$ cm^2) was surrounded by a phosphorus-diffused guard ring. This guard ring was kept at the same potential as the injecting contact. In addition, a shallow boron implant was used under the passivating SiO_2 on the n^+ side to compensate for electron accumulation at the interface due to the fixed positive charge in the oxide. These last two features are designed to eliminate surface leakage currents on the high-impedance side of the diode.

Variable-temperature *J-V* measurements were made in a continuous-flow cold-finger cryostat. A programmable current source was used as a source for the constant current bias, and a unity-gain amplifier was mounted on the sample stage to convert the high-impedance voltage signal to a low-impedance signal measured externally. Care was taken to shield the device from any long-wavelength radiation sources that would photoionize the shallow-level acceptors.

J-V characteristics were measured over a temperature range from 300 to 14 K over two current ranges: a high-current-density range from 10^{-5} to 10^0 A/cm^2 and a low-current-density range from 2×10^{-10} to 2×10^{-5} A/cm^2. It is the low-current-density measurements which reveal a clear transition from lifetime to relaxation behavior, as predicted theoretically. This is shown in Fig. 2, where data for three temperatures (80, 27, and 16 K) are displayed on a linear scale. One observes increased conductance at low voltage and decreased conductance at higher voltages as the sample temperature is decreased to 16 K. This can be compared to the theoretical predictions by Moreau, Manifacier, and Henisch.[6] The data are plotted on a log-linear scale, more conventional for diode characteristics, in Fig. 3. The relative changes in conductance at low bias are evident.

If the results do represent relaxation behavior, then the temperature range in which the transition occurs should correspond to the range in which the ratio of τ_D/τ_0 changes from $\tau_D/\tau_0 \ll 1$ to $\tau_D/\tau_0 > 1$. As Henisch has discussed,[4] a more appropriate description may be that of characteristic lengths (diffusion lengths versus screening lengths), but we will use the more common language in terms of characteristic times for discussion purposes. The dielectric relaxation time in the bulk material can be expressed as $\tau_D = \rho\epsilon\epsilon_0$. In this experiment, the resistivity increases exponentially upon cooling, at temperatures below approximately 50 K, due to the extrinsic freezeout of the majority acceptor boron. This $\rho(T)$ has been modeled, using existing data for the temperature dependence of mobility in high-purity Si,[10] and the well-known expression for the freezeout of shallow levels.[11]

In the case of extrinsic material under low-level injection, the excess-carrier lifetime corresponds to the minority-carrier lifetime. The minority-carrier lifetime in the bulk material is approximately 1 msec at 300 K. The variation in lifetime with temperature is a function of the changes in thermal velocity, cross section, and trap

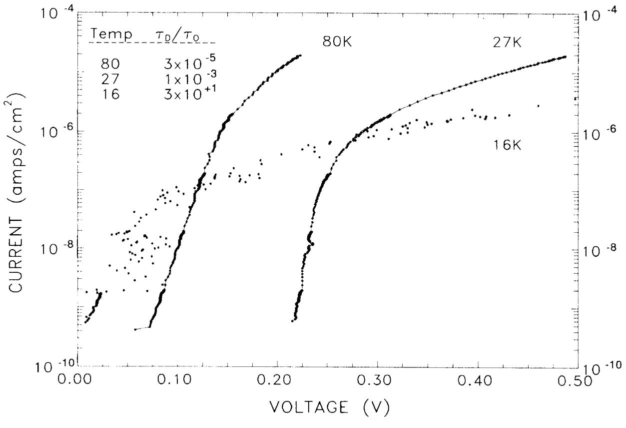

FIG. 3. Log-linear plot of low-current-range *J-V* data.

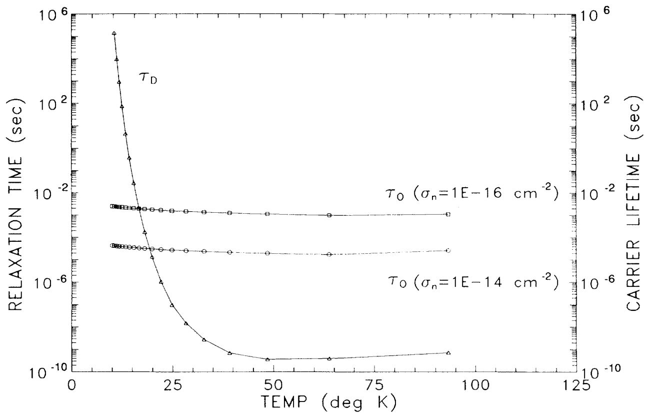

FIG. 4. Comparison of dielectric relaxation time and minority-carrier lifetime showing transition from lifetime to relaxation regime between 25 and 10 K.

occupancy. This change with decreasing temperature was estimated from the standard expression for recombination through midgap traps,[12] where the concentration and ionization energies of the dominant traps were taken from deep-level transient spectroscopy (DLTS) experiments performed on the diode materials. DLTS analysis indicated deep levels at a concentration of approximately 3×10^{11} cm^{-3} at 0.22 and 0.092 eV above the valence band. These are probably associated with Cu or Cu-related complexes,[13,14] although the assignment of DLTS peaks to Cu-related defects is still an area of controversy, and the isolated Cu center has not been directly observed.[15]

Figure 4 shows the calculations for the characteristic times as a function of temperature in the temperature range of interest. Since the dominant traps are not definitely identified, a range of values in the cross section has been used which bracket the reported cross sections. The lifetime and dielectric relaxation time calculations show that the transition from lifetime to relaxation regime would be expected to occur in the range from 25 to 15 K, consistent with experimental results. Similar results are obtained for calculations based on comparison of the diffusion length and the screening length, the appropriate characteristic lengths.

The results can be explained in terms of the model presented by Moreau, Manifacier, and Henisch[6] in which the J-V characteristics were calculated for p^+-i-n^+ structures over a range of τ_D/τ_0 ratios. The results show that the more the material conforms to the relaxation criteria, the more linear the characteristic is. At relatively large forward bias the drift component of the current dominates, and it is the total carrier concentration $(n+p)$ acted upon by the field which determines the conductance. In a lifetime material $n+p$ increases exponentially with voltage, leading to the familiar conductivity modulation characteristic of a diode for these material. The relaxation semiconductor, on the other hand, does not exhibit an increase in carrier concentrations. In fact, exactly the opposite is true for trap-free material. The total $n+p$ is reduced through majority-carrier depletion and the conductance is correspondingly lower. This explains the difference in the J-V characteristics at the higher applied bias.

At lower bias, however, the relaxation semiconductor junction exhibits higher conductivity than would be expected for the lifetime case. Diffusion currents and recombinative current play major roles in the near contact area. In the region immediately adjacent to the boundary, characterized by majority-carrier depletion, the excess electron and depleted hole concentrations lead to a diffusion current which augments the majority-carrier drift current. This increases the local conductivity. Far removed from the contact, the injected-carrier population is very low, and the current is primarily a majority-carrier drift current. In between lies a transition region in which both n and p change rapidly, leading to a diffusion-dominated current and a recombinative current component. In this relaxation case, both diffusion currents associated with the concentration gradients near the contact augment the majority-carrier flow and the increased conductance at low bias is not dependent upon the mobility ratios. This is in contrast to the important role that the mobility ratio can play in determining the effect of minority-carrier injection into a lifetime semiconductor.[16,17]

One should note that the increased conductance cannot be explained by enhanced generation current as a function of increasing depletion width with cooling. The exponential decrease in thermal generation outweighs the increase in depletion width by orders of magnitude.

A transition from lifetime to relaxation behavior has been achieved in high-purity Si by changing the bulk resistivity through the freezeout of majority carriers. The J-V characteristics of a Si n^+-p-p^+ structure exhibit increased conductance at low bias and decreased conductance at high bias compared to the lifetime case. This experimental finding is in good agreement with recent theoretical predictions. Our results extend the experimental studies of relaxation phenomena to materials in which stored space-charge effects due to midgap traps are not dominant. The experiment demonstrates for the first time the steady-state effects of relaxation behavior in a high-purity material which has been reversibly converted from the lifetime to the relaxation regime.

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