Quasi One-Dimensional Conduction in Multiple, Parallel Inversion Lines

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We present results of conductance measurements of ultranarrow inversion layers in which averaging has resulted in what we believe to be a clear observation of a quasi one-dimensional density of states. A 0.2-μm-period grating gate is used to produce 250 inversion lines in parallel, each of which is ~ 50 nm wide and 10 μm long. Summing the conductance of these lines results in a signal-to-noise improvement of of $\sqrt{250}$ (~ 16) which has enabled the observation of the quasi one-dimensional conductance oscillation.

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The quantum-mechanical properties of the two-dimensional (2D) electron gas in silicon inversion layers have been investigated for over 25 years.[1] The electrons are two dimensional at low temperatures because the extreme confinement at the Si/SiO_2 interface produces discrete energy levels (eigenstates) for motion perpendicular to that interface, whose separation in energy is large compared to the Fermi energy and to the thermal energy, k_BT. As a result, electron occupation can be restricted to the lowest 2D subband, yielding transport behavior that is strictly two dimensional. More recently, experiments have been directed at adding lateral confinement to this 2D system so that the electronic states would be *quantized in two directions* and the transport would be one dimensional. Such confinement to widths approaching ~ 50 nm has been achieved by the formation of either a potential well[2-5] or a physical boundary.[6,7] These conductors have been termed *quasi one dimensional* (Q1D) because, for reasonable electron concentrations ($> 2\times 10^{11}/cm^2$), the expected energy-level separations result in several 1D subbands being occupied simultaneously. Random, but "reproducible" features (modulation) in the conductance as a function of gate voltage have consistently been observed in such devices. However, even though the modulation in any given device is fixed, it is (a) different from that in apparently identical devices, (b) too irregular to be caused by a Q1D density of states, and (c) is generally larger in lower-mobility samples.[7] This behavior is consistent with a localization origin and has been attributed to random variations in the confining potential[8] resulting either from linewidth nonuniformities or from fixed scattering centers in close proximity to the inversion lines. Although interesting in its own right, the random modulation or "noise" has totally obscured the regular conductance oscillation expected in a Q1D conductor. In this paper we report the fabrication and measurement of devices in which a periodic gate has been employed to produce 250 ultranarrow inversion lines in parallel. This scheme results in a "signal-to-noise" improvement over single-inversion-line devices by a factor of ~ 16 ($\sqrt{250}$). For the narrowest lines, the transconductance exhibits a regular oscillation that is consistent with the calculated quasi one-dimensional density of states.

The Q1D devices fabricated for this experiment are nearly identical to the grating-gate field-effect transistors (FET's) reported previously for the study of transport in a surface superlattice (SSL).[9] As shown in layout and cross section in Fig. 1, the Q1D devices have a 0.2-μm-period tungsten grating (fabricated with use of x-ray lithography[9-11]) embedded within a dual, stacked-gate configuration. The two gates produce electron confinement in the p-type Si channel by forming a periodic array of potential wells. The advantage of the dual-gate structure is that the mean charge density in the inversion layer (i.e., the Fermi level) and the amplitude of the periodic potential may be controlled independently. The only significant difference between the Q1D and SSL devices is the orientation of this grating relative to the current flow in the channel. In an SSL device, transport is *perpendicular* to the grating lines (and to the resulting periodic potential), while the Q1D device layout results in transport *parallel* to them. Also, in the Q1D devices a strong periodic potential is induced which divides (confines) the electron sheet into isolated lines. This can be contrasted with the operating mode of the SSL devices where the two gates are used to produce a weak potential modulation superimposed on a completely inverted interface.

To form the parallel Q1D conductors, one of the two gate electrodes is used to produce a periodic, confining potential well, while the other is used as the control electrode for variation of the electron concen-

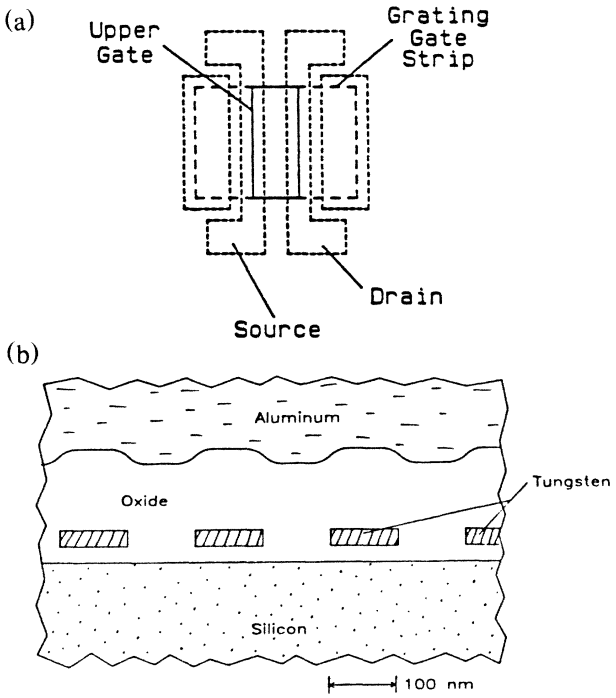

FIG. 1. Q1D grating-gate device structure. (a) Schematic of the device layout, illustrating the n^+ source and drain, grating-gate strip, upper gate, and contact areas. (b) Channel cross section showing the dual, stacked-gate configuration with 0.2-μm-period W grating.

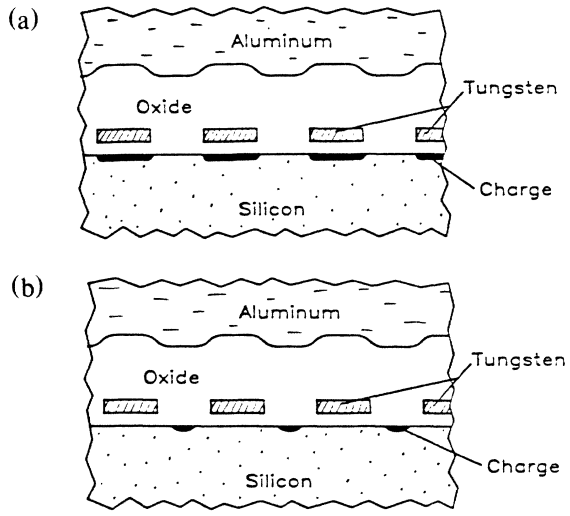

FIG. 2. Q1D charge-confinement schemes. (a) Subgrating confinement, where the upper gate is fixed and the grating controls the electron density. (b) Gap confinement, where the upper electrode is the control.

tration in the narrow lines. The two electrodes are interchangeable in this respect so that the devices can be operated in either a subgrating-confinement mode where the grating is the control electrode, or in a gap-confinement mode where the continuous upper gate is the control electrode, as illustrated in Fig. 2. As suggested by this figure, the inversion lines will typically be narrower for the gap confinement and this has been verified both by electrical measurements and by 2D computer simulation.[10]

Test structures and planar FET's were used to verify device structural integrity. From these planar FET's maximum mobilities of ~ 800 cm^2/V-sec at room temperature and 7000 to 8000 cm^2/V-sec at 4.2 K were obtained. Q1D devices were checked initially at room temperature, and those having gate oxides free of electrical shorts were bonded for testing at low temperature.

To produce subgrating confinement [Fig. 2(a)], the upper gate's bias was fixed at a level below threshold so that the Si region between grating lines would not invert. For all measurements, longitudinal electric fields were kept below ~ 0.1 V/cm to prevent electron heating. Operated in this manner, Q1D devices were observed to have "normal" transistor characteristics over the entire temperature range explored here (295–1.2 K). Dependence on the upper (confinement) gate bias was also examined, and while a threshold variation was observed, very little change in the maximum slope occurred. This indicates that the width of the inversion region under the grating lines was relatively independent of the upper gate bias, in agreement with 2D simulation of the device structure.[10] Of primary significance here is the fact that in channels having 250 inversion lines with nominal widths of 0.1 μm, *no oscillations in the transconductance were observed.*

To produce gap inversion [Fig. 2(b)], the grating bias was fixed below threshold to produce the confining potential wells, while the upper gate controlled the inversion electron concentration in the gaps. Typical I_{DS}-V_{UGS} (source-drain current versus upper gate bias) data at 1.2 K are shown in Fig. 3(a), and it can be seen that there is no *strong* modulation. Differentiation, however, reveals a regular, weak oscillation of the transconductance with gate voltage [Fig. 3(b)] having a "period" of 1–1.5 V. Of the three devices tested at low temperature, the two higher-mobility samples showed oscillations with approximately equal spacing (though with different thresholds) while the lowest-mobility sample (~ 2000 cm^2/V-sec) showed none. To determine whether this oscillation was due to a Q1D density of states, the dependence of the I_{DS}-V_{UGS} characteristics on confinement gate bias was studied again, and, similar to the subgrating-confinement case, a strong variation in the threshold voltage was observed, but the maximum slope varied only weakly. In addition, no variation of spacing between adjacent peaks that was indicative of quantum-well width variations was observed. The tem-

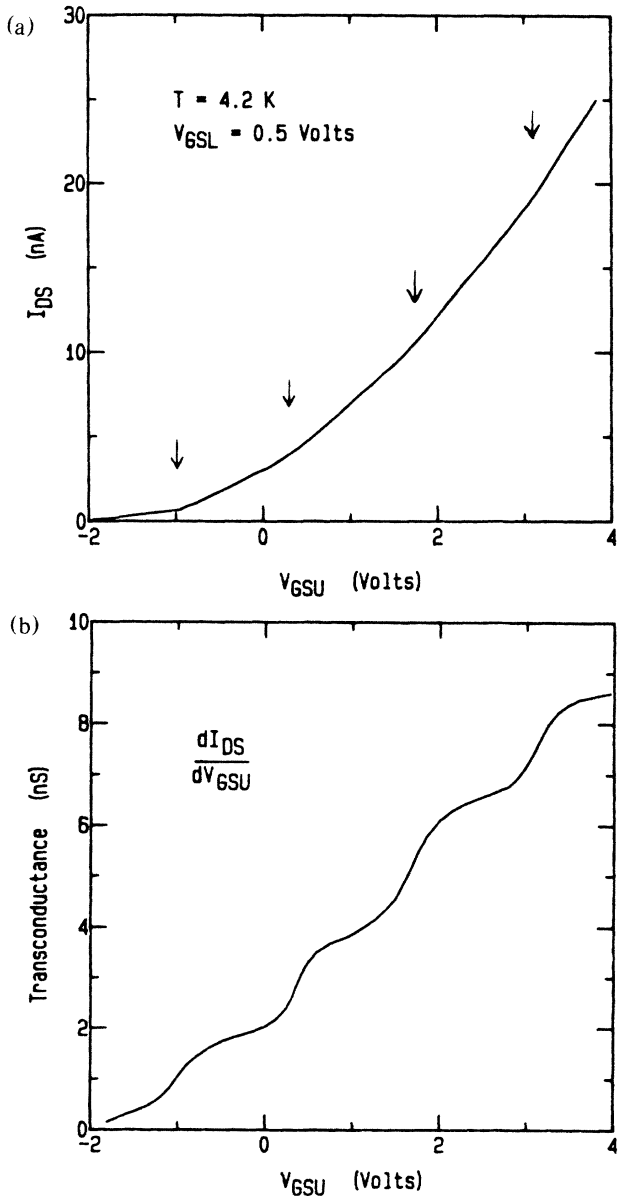

FIG. 3. I_{DS}-V_{UGS} (source-drain current vs upper gate bias) data for a Q1D device operated in the gap inversion mode at 1.2 K. (a) Normal I_{DS} vs V_{UGS}, and (b) derivative $(\partial I_{DS}/\partial V_{UGS})$ vs V_{UGS}.

perature dependence was also examined and it was found that the modulation could be observed at 4.2 K and (very weakly) at temperatures approaching 10 K. It is also significant that, unlike single-inversion-line devices, no strong *random* structure in the conductance was observed at 1.2 K.

Modulation of the conductance with gate voltage in a quasi one-dimensional conductor is a predictable consequence of the nonuniform density of states. In an ideal 1D system (i.e., single subband) the density of states varies as $E_F^{-1/2}$. Figure 4 shows density-of-states calculations for several 1D subbands (i.e.,

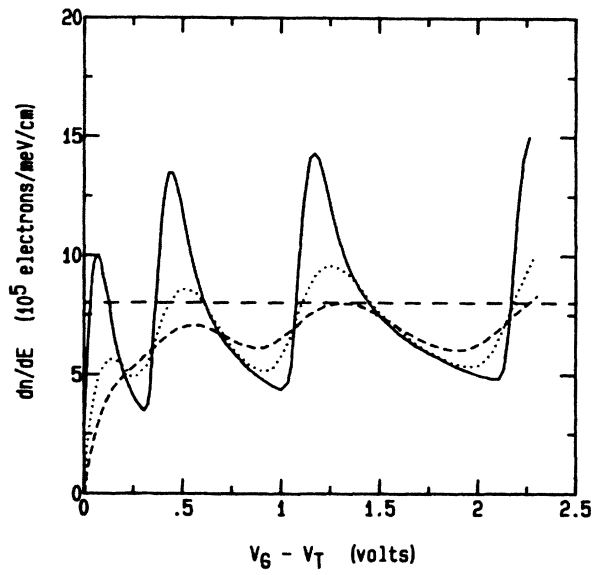

FIG. 4. Plots of the effective density of states, $\bar{g}_1$, in a Q1D conductor showing the decrease in modulation amplitude with increasing temperature. System modeled is a square well of width 50 nm at $T = 1.2$, 4.2, and 8 K. Dashed line is the equivalent 2D approximation for the same channel width (i.e., $g_2 W$).

Q1D), and includes the effect of thermal broadening.[10] Although the data and simulation indicate a fairly constant level spacing indicative of a harmonic-oscillator potential well, a square-well approximation has been used in this analysis for simplicity. If one assumes a well width, W, of 50 nm (from simulation), the expected lowest subband separation, ΔE, from the square-well approximation $(3\hbar^2\pi^2/2m^*W^2)$ is ~ 2 meV. This can be compared with the experimental data by relating the difference between successive transconductance peaks in gate voltage, ΔV_{UGS}, to the shift in the Fermi level at the interface. With approximation of the inversion line as a narrow 2D electron gas (see Fig. 4), a ΔV_{UGS} of 1.3 V and a capacitance of 1.7×10^{-8} F/cm^2 (from 0.2 μm of SiO_2) gives an electron-density difference, Δn_s, of 1.4×10^{11}/cm^2. Dividing this by the 2D density of states ($\sim 1.6 \times 10^{11}$/cm^2-meV), one obtains a level spacing of 0.9 meV. At this point, it is unclear whether the discrepancy between this and the theoretical value of 2 meV is due to the 2D approximation used here, or to a difference in the actual width of the narrow inversion lines. A width of ~ 70 nm would account for the difference, and such a width (resulting from a grating line-to-space ratio of less than 1) is not out of the question. The experimental level spacing and the oscillation weakness are consistent with level broadening of $\simeq 1$ meV from elastic scattering $(\hbar/2\tau_e)$. This is also consistent with the absence of oscillation in the

subgrating case since the wider inversion lines result in smaller level spacings so that $\hbar/2\tau_e > \Delta E$.

Finally, it should be noted that the expectation of strong signal-to-noise improvement appears to be verified. This improvement relies on two conditions: (a) that the random features in different narrow inversion lines are uncorrelated, and (b) that the Q1D modulation in different lines should sum coherently. The first assumption is consistent with the present model for the random modulation, since the associated potential fluctuations are short range (relative to channel dimensions). The second assumption requires that the threshold for inversion and the inversion-line width in different lines fall within a predictable range. Calculations for this structure have been performed,[10] and they indicate that the threshold requirement is not restrictive, but that the width requirement imposes severe lithography constraints on the fabrication of the narrow lines. For these dimensions, the requirement is that the inversion-line width tolerance is roughly $\pm 5\%$, and while the grating-line variation is observed to be about 10%, it is uncertain exactly how much smoother the narrow inversion lines are. It is therefore possible that such variations also contributed to the observed broadening.

In summary, we report the fabrication of grating-gate FET's which have been used to study electronic transport in narrow inversion lines. A parallel-channel scheme has been employed to increase the Q1D signal relative to that arising from localization, resulting in what we believe to be a clear observation of a quasi one-dimensional density of states.

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