

Universal Parity Quantum Computing

Michael Fellner^{1,2,*}, Anette Messinger², Kilian Ender^{1,2}, and Wolfgang Lechner^{1,2,†}

¹*Institute for Theoretical Physics, University of Innsbruck, A-6020 Innsbruck, Austria*

²*Parity Quantum Computing GmbH, A-6020 Innsbruck, Austria*



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We propose a universal gate set for quantum computing with all-to-all connectivity and intrinsic robustness to bit-flip errors based on parity encoding. We show that logical controlled phase gate and R_z rotations can be implemented in parity encoding with single-qubit operations. Together with logical R_x rotations, implemented via nearest-neighbor controlled-NOT gates and an R_x rotation, these form a universal gate set. As the controlled phase gate requires only single-qubit rotations, the proposed scheme has advantages for several cornerstone quantum algorithms, e.g., the quantum Fourier transform. We present a method to switch between different encoding variants via partial on-the-fly encoding and decoding.

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Designing quantum computers [1–17] and quantum algorithms [18–26] is a current grand challenge in science and engineering, motivated by the prospect of solving certain problems exponentially faster than any known classical algorithms [21]. However, the fundamental rules of quantum mechanics that make this new paradigm possible also impose fundamental restrictions. In contrast to classical information, quantum information cannot be copied, which is known as the no-cloning theorem, but only propagated [27]. Thus, quantum computers will not be able to follow the von Neumann architecture [28] with separated memory and computational unit. As the quantum CPU serves as memory and computational unit at the same time, connectivity between any quantum bits on the chip is required. In current standard approaches to gate-based quantum computers, either these long-range interactions are implemented as physical interactions, which limits scalability, or quantum information is moved on the chip via SWAP sequences, which requires a large overhead in gates. Although there are recent approaches toward qubit routing that address this issue [29,30], exchanging information between qubits remains a challenging problem.

In this Letter, we propose a novel universal quantum computing approach based on the Lechner-Hauke-Zoller (LHZ) architecture [31], which was originally designed for quantum annealing. In this parity-based paradigm, each physical qubit represents the parity of multiple logical qubits. We extend the LHZ architecture, up to now only

used for solving combinatorial optimization problems, to a universal quantum computing approach by providing a universal gate set on parity-encoded states and with that, open up new possibilities for universal quantum computation. These extensions include an additional row of *data qubits* added to the original LHZ layout to enable control of single logical qubits. We introduce logical operations, in particular R_x rotations, to establish a universal gate set in the logical space. As the parity constraints no longer need to be enforced throughout the computation, they can be utilized for error correction.

As it only requires nearest-neighbor interactions between qubits on a square lattice chip, our proposal can be implemented on state-of-the-art quantum devices, independent of the qubit platform. Suitable platforms are for example superconducting qubits [15,32–36], neutral atoms [37–39], or trapped ions [40–43]. We show that the parity transformation renders diagonal multiqubit operators between arbitrary logical qubits into single-qubit physical gates and, in turn, nondiagonal logical operators into sequences of physical gates. The transformation eliminates the need for long-range interactions and thus SWAP gates as illustrated in Fig. 1. Furthermore, redundant encoding offers the potential for intrinsic tolerance against bit-flip errors. We additionally present a possibility to choose and switch between different variants of the parity mapping, containing subsets of parity qubits tailored to the algorithmic requirements. This allows for further reduction of computational resources.

The gate set presented here contains operations that correspond to R_x and R_z rotations and controlled phase gates acting on logical qubits. Because of the absence of any connectivity limitations, we expect this approach to have an impact on the design of next generation quantum devices [44]. The scheme allows for an efficient

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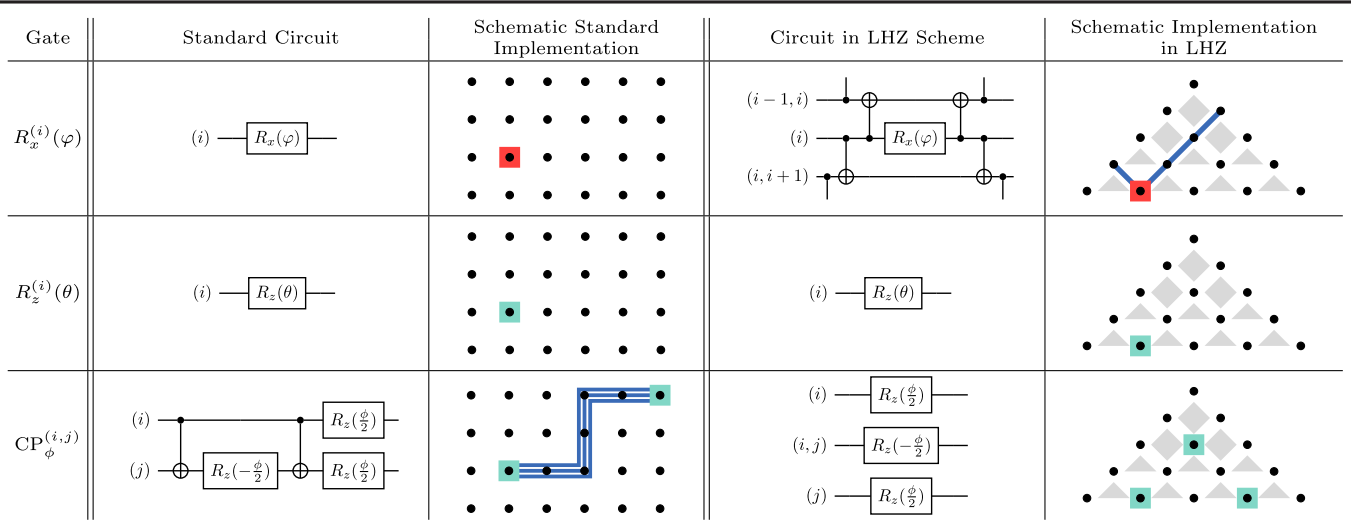


FIG. 1. Overview over the implementation of a universal gate set in the LHZ scheme. All operations have been decomposed to CNOT gates and local rotations. Blue lines represent a chain of CNOT gates, while red (darker) and green (lighter) squares depict local R_x and R_z rotations, respectively. Triple lines correspond to SWAP gates, consisting of 3 CNOT gates each.

implementation of controlled rotations around the z axis and is thus advantageous for the quantum Fourier transform [45] which is the basis of Shor's factoring algorithm [21] as well as quantum addition [46]. Implementations of well-known quantum algorithms in the parity architecture are shown in detail in the associated publication Ref. [47].

Parity mapping.—The LHZ architecture [31] expands the Hilbert space of n logical qubits to a Hilbert space of $K = n(n-1)/2$ physical qubits (parity qubits, with operators σ), encoding the parity of pairs of logical qubits (with operators $\tilde{\sigma}$) such that for any state $|\psi\rangle$ in the code space,

$$\tilde{\sigma}_z^{(i)} \tilde{\sigma}_z^{(j)} |\psi\rangle = \sigma_z^{(ij)} |\psi\rangle, \quad (1)$$

where the superscripts correspond to qubit labels. The code space is restricted to configurations corresponding to valid logical states $|\psi\rangle$ by $K-n+1$ parity constraints of the form

$$C_l |\psi\rangle := \sigma_z^{(l_1)} \sigma_z^{(l_2)} \sigma_z^{(l_3)} [\sigma_z^{(l_4)}] |\psi\rangle = |\psi\rangle \quad (2)$$

where the indices l_i correspond to pairs of logical indices, such that in every constraint, each logical index appears an even number of times. The brackets around $\sigma_z^{(l_4)}$ indicate that a constraint can contain either 3 or 4 qubits. Here, we use a slightly modified layout compared with the original LHZ layout, shown in Fig. 2, with an additional row of physical qubits which have a direct correspondence to single logical qubits,

$$\tilde{\sigma}_z^{(i)} = \sigma_z^{(i)}. \quad (3)$$

In the following, these additional qubits are referred to as *data qubits*. As depicted in Fig. 2, n all-to-all connected logical qubits are represented by $K = n(n+1)/2$ physical

qubits and $K-n$ constraints. The parity constraints generate the stabilizer of the code space [48], additionally allowing for detection of bit-flip errors and thus an intrinsic fault tolerance of the encoding.

Logical qubits and operators.—Next, we introduce the concept of *logical lines* denoted as Q_i , which have been identified in a different context in Ref. [49]. A logical line Q_i is defined as the set of all parity qubits containing the logical index i . In the LHZ architecture, qubits that contain a particular index are arranged along lines, which are indicated as solid lines in Fig. 2 to guide the eye. The red line for example extends from the data qubit (3) to all parity qubits that contain the index 3, and thus contain all relative parity information with respect to the logical qubit (3). For each logical line Q_i we define an operator

$$\tilde{\sigma}_x^{(i)} = \sigma_x^{(i)} \prod_{j<i} \sigma_x^{(ji)} \prod_{j>i} \sigma_x^{(ij)} \quad (4)$$

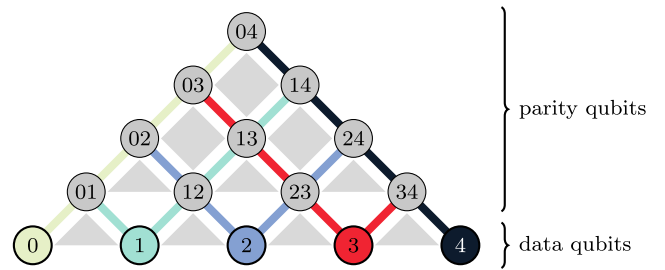


FIG. 2. Illustration of the modified LHZ architecture with logical lines. Three- and four-body constraints are represented by light gray triangles and squares between corresponding qubits. Data qubits with single logical indices are added as an additional row at the bottom of the architecture to allow direct access to logical R_z rotations. Colored lines connect all qubits whose labels contain the same logical index. Logical R_x rotations can be realized with chains of CNOT gates along the corresponding line.

acting on every qubit in the respective line. The operators $\tilde{\sigma}_x^{(i)}$ and $\tilde{\sigma}_z^{(i)}$ commute with all parity constraints and fulfill the (anti-) commutation relations for Pauli operators

$$\{\tilde{\sigma}_x^{(i)}, \tilde{\sigma}_z^{(i)}\} = [\tilde{\sigma}_x^{(i)}, \tilde{\sigma}_z^{(j)}] = 0 \quad (5)$$

for $i \neq j$. We can therefore identify the operators with Pauli operators acting on logical qubits, and build arbitrary logical rotations as

$$\tilde{R}_x(\alpha) = \exp\left(-i\frac{\alpha}{2}\tilde{\sigma}_x^{(i)}\right) \quad (6)$$

and

$$\tilde{R}_z(\alpha) = \exp\left(-i\frac{\alpha}{2}\tilde{\sigma}_z^{(i)}\right). \quad (7)$$

Throughout this Letter, tildes are used to denote operators with the corresponding action on logical qubits. While a logical \tilde{R}_z rotation can be directly implemented using the respective physical operator on the data qubit, the \tilde{R}_x operator on logical qubit (i) given by expression (6) can be implemented via physical controlled-NOT (CNOT) gates along the logical line Q_i and a physical single-body R_x rotation, as depicted in Fig. 1 (also see Ref. [50] for details on efficient implementations of exponentials of multiqubit Pauli operators). The chosen layout further ensures that all operators associated with the logical lines can be implemented with local operations and nearest-neighbor CNOT gates on a square lattice.

Encoding and decoding.—In the following we discuss the encoding and decoding of arbitrary states from and to the data qubits. Let us first consider the trivial logical state $|0\rangle^{\otimes n}$ which can be encoded in the LHZ scheme by preparing all physical qubits in the product state $|0\rangle^{\otimes K}$. This state fulfills all constraints, and is the joint eigenstate of the logical $\tilde{\sigma}_z$ operators with eigenvalue +1. Encoding an arbitrary, unknown quantum state into the LHZ scheme is less straightforward. Classically, the states of the data qubits are identical to the corresponding logical qubits (by definition, a measurement of these qubits in the z basis corresponds to a measurement of the logical state). However, they are typically highly entangled with the other qubits, and simply tracing out the parity qubits would cause a loss of coherence and therefore phase information.

We thus introduce an encoding and decoding strategy to add or remove an arbitrary number of parity qubits to or from the code. Suppose we start with the logical qubits, each of them encoded in a data qubit. We can now add a physical qubit (ij) corresponding to the parity of qubits (i) and (j), by initializing this qubit in the state $|0\rangle$ and then imposing the parity on it with two CNOT gates controlled by qubits (i) and (j), as shown in Fig. 3(b). This procedure adds an additional parity qubit to the code and guarantees

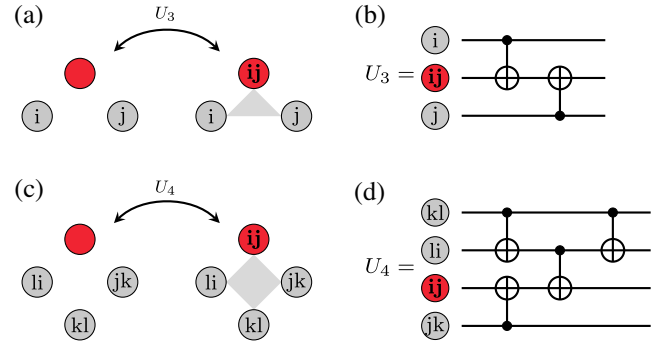


FIG. 3. Encoding and decoding circuits to add or remove a qubit and the corresponding constraint to or from the code. (a) Qubit (ij) is directly encoded via the adjacent data qubits (i) and (j) in a three-body constraint, with the circuit (b). (c) Qubit (ij) is encoded using other parity qubits in a four-body constraint, with the circuit (d). A qubit without a label indicates a qubit without any parity information, being in the state $|0\rangle$.

that the corresponding constraint $C = \sigma_z^{(i)} \sigma_z^{(j)} \sigma_z^{(ij)}$ is satisfied.

Following this procedure, it is possible to add parity qubits and constraints by applying this strategy iteratively. Instead of directly obtaining the parity information from the data qubits, one can also use the parity qubits included in local constraints, as for example the plaquettes shown in Fig. 2: By definition, the parity of all but one qubit of a constraint is always encoded in the state of the remaining qubit, i.e.,

$$\begin{aligned} \sigma_z^{(ij)} \sigma_z^{(jk)} \sigma_z^{(kl)} \sigma_z^{(li)} |\psi\rangle &= |\psi\rangle \\ \Rightarrow \sigma_z^{(ij)} |\psi\rangle &= \sigma_z^{(jk)} \sigma_z^{(kl)} \sigma_z^{(li)} |\psi\rangle. \end{aligned}$$

This transition and the encoding circuits are shown in Figs. 3(c)–3(d).

Conversely, applying the same gate sequence to a parity-encoded set of qubits removes the targeted qubit from the code and projects it to the state of the corresponding constraint. If the constraint was fulfilled, this is the state $|0\rangle$. For a layout as depicted in Fig. 2 with n logical qubits, this procedure allows encoding and decoding circuits with an overall circuit depth of $n + 1$. The exact circuit is given in the Supplemental Material [51].

The described procedure does not only offer a way to build up or collapse the all-to-all connected LHZ scheme, but also holds the possibility to switch between different variants of the parity mapping and adapt the number of parity qubits to the algorithmic requirements during computation. For example, if some interactions are not needed for a certain algorithm, it is not always necessary to have the corresponding parity qubits in the code. A reduction in the number of parity qubits results in shorter logical lines and thus fewer physical gates. In addition to the two-body parities as introduced in Eq. (1), it is also possible to encode

higher-order k -body parity qubits in the same manner, when using suitable layouts (see Ref. [47] for more details). As an example, a three-body parity qubit can be used to enable a nontrivial interaction between three logical qubits.

Universal gate set.—Single-qubit operations on logical qubits can be constructed from the operators introduced in Eqs. (6)–(7) using the decomposition

$$U = R_z(\alpha)R_x(\beta)R_z(\gamma). \quad (8)$$

To obtain a universal gate set, an additional two-qubit entangling gate is necessary. In the LHZ encoding, a native logical two-qubit operation is obtained by performing a single R_z rotation on a physical parity qubit,

$$R_z^{(ij)}(\alpha) = \exp\left(-i\frac{\alpha}{2}\sigma_z^{(ij)}\right), \quad (9)$$

which is stabilizer equivalent (i.e., the same up to the application of a constraint operator $C = \sigma_z^{(i)}\sigma_z^{(j)}\sigma_z^{(ij)}$) to the operator

$$\exp\left(-i\frac{\alpha}{2}\sigma_z^{(i)}\sigma_z^{(j)}\right) \quad (10)$$

and thus effectively performs the two-body operation $\exp[-i(\alpha/2)\tilde{\sigma}_z^{(i)}\tilde{\sigma}_z^{(j)}]$ on the logical qubits, as is obvious from Eq. (1). This operation can be transformed to a logical controlled phase gate CP_ϕ with local R_z rotations only, as shown in the following. For the sake of simplicity, qubit indices are omitted. We start from an operation

$$e^{-i\frac{\phi}{2}\sigma_z \otimes \sigma_z} = \text{diag}(e^{-i\frac{\phi}{2}}, e^{i\frac{\phi}{2}}, e^{i\frac{\phi}{2}}, e^{-i\frac{\phi}{2}}) \quad (11)$$

and the single-body R_z rotation,

$$R_z(\theta) = e^{-i\frac{\theta}{2}\sigma_z} = \text{diag}(e^{-i\frac{\theta}{2}}, e^{i\frac{\theta}{2}}), \quad (12)$$

and define

$$U_R := [\mathbb{1} \otimes R_z(\beta)]e^{-i\frac{\phi}{2}\sigma_z \otimes \sigma_z}[R_z(\gamma) \otimes \mathbb{1}]. \quad (13)$$

Evaluating Eq. (13) for $-\alpha = \beta = \gamma = (\phi/2)$ yields

$$U_R = e^{-i\frac{\phi}{4}} \cdot \text{diag}(1, 1, 1, e^{i\phi}) = e^{-i\frac{\phi}{4}} \cdot \text{CP}_\phi,$$

which corresponds, up to a global phase, to the controlled phase gate CP_ϕ . Using the identities defined above, this can be implemented in our scheme with local operations on the physical parity qubits and data qubits as

$$\tilde{\text{CP}}_\phi^{(i,j)} = R_z^{(i)}\left(\frac{\phi}{2}\right)R_z^{(ij)}\left(-\frac{\phi}{2}\right)R_z^{(j)}\left(\frac{\phi}{2}\right). \quad (14)$$

Here, i and j are the indices of the involved logical qubits, and R_z indicates the rotation on the corresponding data or

TABLE I. The number of physical operations needed to perform logical gates in the parity encoding for $n > 4$. All operations were decomposed into CNOT gates and local R_x and R_z rotations. The spin-flip operator σ_x is a special case of the R_x rotation, for which the logical implementation reduces to a product of single-qubit spin flips which can be performed in parallel. The unitary U represents an arbitrary nondiagonal single-qubit operation. A detailed derivation of the given numbers can be found in Ref. [47].

Logic gate	Required gates in LHZ		
	Single qubit	2 Qubit	Depth
R_x	1	$2(n-1)$	$2\lceil n/2 \rceil + 1$
σ_x	n	0	1
R_z	1	0	1
U	3	$2(n-1)$	$2\lceil n/2 \rceil + 1^a$
CP	3	0	1
$\text{CNOT}^{(c,t)}$	7	$2(n-1 + c-t)$	$\leq 4\lceil n/2 \rceil + 3^b$
$\prod_{i=1}^m U_i^{(n_i)c}$	$3m$	$2n(n-1)$	$2n+3$

^aFor $n \leq 4$, the depth increases by two steps because the R_z rotations cannot be performed parallel to other operations.

^bCan be further optimized depending on the control qubit and target qubit. For a detailed discussion, see Ref. [47].

^c $n_i \leq n$ denotes the qubit on which U_i acts, and $m \leq n$ is the number of qubits involved. We count consecutive single-qubit operations as a single time step.

parity qubit. In particular, for $\phi = \pi$, we obtain the CZ gate (controlled Z gate). This can in turn be transformed to a CNOT gate, by applying logical Hadamard gates before and after the CZ gate on the desired target qubit. The operations \tilde{R}_x , \tilde{R}_z , and $\tilde{\text{CP}}_\phi$ form a *universal gate set* in the LHZ scheme, and we can not only build arbitrary quantum circuits by applying CNOT gates and controlling local fields (parameters only occur in single-qubit operations), but also exploit the comparably simple implementation of a controlled phase gate. The standard gate model requires two CNOT- and three single-qubit gates to implement a controlled phase gate, as depicted in Fig. 1. Platforms with limited connectivity typically need a large number of SWAP gates in addition. In contrast, a logical controlled phase gate in our approach only requires three parallel single-body rotations. The required resources for implementing common gates and gate sequences in our scheme are listed in Table I. The depth and the gate count for nondiagonal single-body operations result from the CNOT chains involved. The main advantage of the encoding clearly comes from the depth-1 implementation of diagonal gates. Note that while nondiagonal operations have a higher cost, their increased weight allows for intrinsic tolerance to bit-flip errors as an additional advantage.

Following Eq. (8), any local unitary operation U on a logical qubit (i) can be performed in the LHZ scheme by performing it on the data qubit (i) and surrounding it by the CNOT chains as in the logical \tilde{R}_x rotation,

$$\begin{aligned}
 \tilde{U} &= \underbrace{R_z^{(i)}(\alpha) \dots \text{CNOT}^{(ij)}}_{\tilde{R}_z} \underbrace{R_x^{(i)}(\beta) \text{CNOT}^{(ij)}}_{\tilde{R}_x} \dots \underbrace{R_z^{(i)}(\gamma)}_{\tilde{R}_z} \\
 &= \dots \text{CNOT}^{(ij)} R_z^{(i)}(\alpha) R_x^{(i)}(\beta) R_z^{(i)}(\gamma) \text{CNOT}^{(ij)} \dots \\
 &= \dots \text{CNOT}^{(ij)} U^{(i)} \text{CNOT}^{(ij)} \dots
 \end{aligned}$$

The circuit depth for this construction is given in Table I. Fixing the qubit on which the R_x rotations are performed to the respective data qubit reduces hardware requirements such that R_x rotations are only ever necessary on the data qubits, while for the parity qubits, local R_z rotations and CNOT gates between them are sufficient.

Note that a circuit implementing a product of $m \leq n$ logical single-qubit operators can be realized by applying the decoding circuit, performing the single-body operations on the data qubits and encoding again with an overall circuit depth of $2n + 3$ and a CNOT-gate count of $2n(n - 1)$.

Error correction.—The redundancy of the parity encoding allows for the correction or mitigation of bit-flip errors. Because all parity constraints commute with any logical operator, measuring their value does not disturb the logical state of the system. Constraint measurements can be performed either with the help of ancillary measurement qubits in the center of each plaquette [45,52], or by applying the decoding circuit as in Figs. 3(b) and 3(d) to each constraint, measuring the decoded qubit, and encoding it again.

As the transition from one logical basis state to another flips n physical qubits, it is in principle possible to correct for multiple errors at a time. For different encoding variants, for example with a reduced number of parity qubits, the number of simultaneously correctable errors depends on the number of qubits in the shortest logical line. F. Pastawski and J. Preskill successfully demonstrated error correction via belief propagation on a LHZ chip [53], and showed that the LHZ encoding is robust against weakly correlated bit-flip noise. An analysis of the bit-flip error-correction capability of the LHZ architecture is provided in the Supplemental Material [51].

To ideally complement the bit-flip tolerance of the LHZ encoding, it is advisable to use physical qubits which are intrinsically robust against phase errors [54–57].

Conclusion and outlook.—In conclusion, we have demonstrated a universal gate set implemented in the LHZ encoding, opening up a new strategy for universal quantum computation. All gates can be implemented on state-of-the-art quantum devices that fulfill the comparably low requirement of nearest-neighbor connectivity on a square lattice. Furthermore, the encoding can be dynamically adjusted by adding or removing parity qubits tailored to the requirements of different algorithms. The introduced decoding scheme can be used to decode the output of optimization algorithms run in the parity scheme as for example proposed in Refs. [58–60], in order to further work with

the resulting quantum states. With its availability of nonlocal and multiqubit operations and the intrinsic error-correction capability, we expect our work to be a step toward the next generation of quantum computers.

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*m.fellner@parityqc.com

†wolfgang.lechner@uibk.ac.at

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