Extended Charge Layers in Metal-Oxide-Semiconductor Nanocapacitors Revealed by *Operando* Electron Holography

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The metal-oxide-semiconductor (MOS) capacitor is one of the fundamental electrical components used in integrated circuits. While much effort is currently being made to integrate new dielectric or ferroelectric materials, capacitors of silicon dioxide on silicon remain the most prevalent. It is perhaps surprising therefore that the electric field within such a capacitor has never been measured, or mapped out, at the nanoscale. Here we present results from *operando* electron holography experiments showing the electric potential across a working MOS nanocapacitor with unprecedented sensitivity and reveal unexpected charging of the dielectric material bordering the electrodes.

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Introduction.—Metal-oxide-semiconductor (MOS) capacitors are widely used in many advanced devices whose performance is dependent on their miniaturization and operation [1]. They can be employed individually or as an element of more elaborate components such as the field-effect transistor, flash memory, dynamic random-access memory, and active regions of image sensors. A MOS capacitor is composed of a thin oxide layer sandwiched between a top metal electrode and a bottom electrode of semiconductor substrate [2]. While new materials for the dielectric are constantly being explored from high-K materials [3] to ferroelectrics [4] and negative capacitance ferroelectric stacks [5], silicon dioxide is still the most widely used dielectric material and is featured prominently in textbooks on semiconductor physics. By applying bias across the two electrodes, charge is stored at the two interfaces. In reality, the physics is rich and complex, ranging from band-bending, depletion regions and inversion layers in the semiconductor substrate to charge trapping in the dielectric oxide and at the interfaces. It is the latter phenomenon that is of particular interest here.

Charge trapping changes the capacitance and performance of real devices by modifying the threshold voltage and frequency response [6] and is a major concern for dielectric breakdown [7]. Some traps are expected to be stable over time and others occupied dynamically as a function of the applied bias. Much discussion has been made of the nature of the traps and where they occur: at the interface, in immediate vicinity to the interface, or within the bulk of the dielectric [8]. Others refer to border traps, being near the interface but within the dielectric layer [9]. Interest in the topic has recently been revived since interface and border traps have been linked to reliability issues [10,11]. The uncertainty concerning their location arises from the fact that the majority of the characterization techniques are based on indirect measurements. Electrical characterization by Fermi-probe techniques, thermal activation, photoemission, x-ray photoelectron spectroscopy, and electron spin-based methods measure the global response of a device or lack the spatial resolution to probe the distribution of traps at the nanometer length scale [12]. We have therefore explored whether transmission electron microscopy, and in particular electron holography, can be used as a new way of studying these systems.

Electron holography is a powerful technique for measuring local fields in materials, from electric and magnetic [13–15] to mechanical strain [16]. Indeed, the phase of the electron hologram can be directly related to the electrostatic potential encountered by the fast electron along its trajectory:

$$\phi^E(x,y) = C_E \int V(x,y,z)dz, \tag{1}$$

where C_E depends only on universal constants and the accelerating voltage of the microscope. While it was shown early on that electric fields could be measured in semiconductor devices in such a way [17,18], the development of *operando* experiments has been a long one.

The p-n junction was the first object of study, since there is a built-in electric field requiring no external applied bias. After pioneering *in situ* observations [19], an important breakthrough was achieved when the projected potential across a junction was measured for the first time by applying contact clamps to the wafer [20]. This led to the identification of key issues such as specimen preparation, surface damage layers, stray fields, and electron radiation [21–23]. Rare, however, has been the study of biased devices even with dedicated probe-based

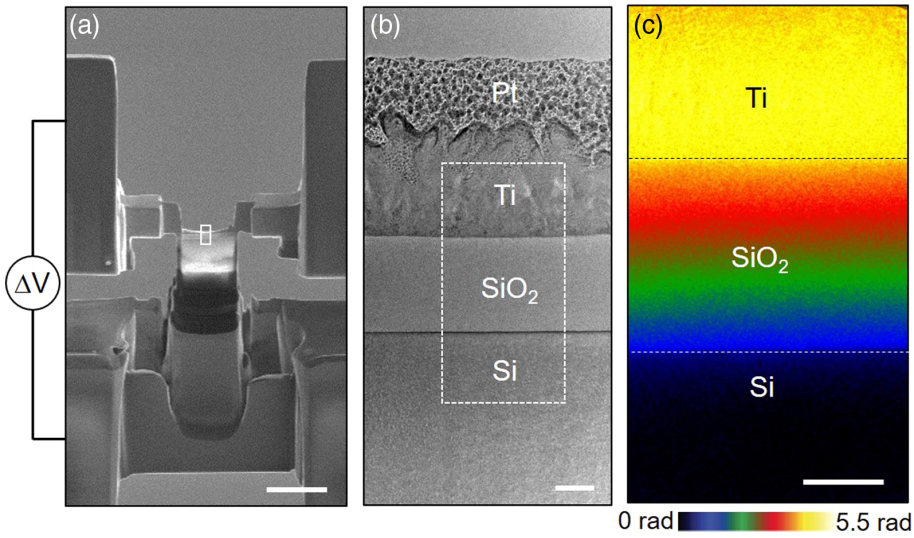

FIG. 1. *Operando* electron holography of nanocapacitor. (a) Scanning electron microscopy (SEM) image of specimen device within the FIB showing Pt deposited contacts to chip gold electrodes. (b) TEM image of active region showing substrate highly doped silicon, dielectric layer of silicon-dioxide (120 nm), top electrode of Ti, and Pt contact layer. (c) Phase map of projected electric potential obtained by electron holography [dotted region in (b)]. Scale bars are 5 μm for (a) and 50 nm for (b) and (c).

holders [24]. The main problem is that the stray field around the nanoprobe is significant, perturbing the reference area of the hologram [25] and the potential applied to the active area [26]. In addition, the contact resistance between nanoprobe and sample is unknown, poorly controllable, and causes mechanical instabilities. To make the quantitative measurement of electric field feasible in devices such as a nanocapacitor, a different approach is needed.

Result.—Specimen device adapted to *operando* electron holography: To this end, along with other groups [26–31], we have been developing the fabrication of what we call "specimen devices" (Fig. 1): an operational device that is both electron transparent and contacted on a chip for biasing *in situ* without the need of a nanoprobe [32]. First, a thin lamella is extracted directly from thin film wafers or devices by focused-ion beam (FIB). Second, the lamella is placed across the electrodes of a specially designed chip with patterned electrodes and contacts made between the lamella and electrodes by depositing metal with the gas-injection system of the FIB. Final polishing for electron transparency is performed at low energy to limit the surface contamination and damage layers (for more details, see Supplemental Material [33]). The chip can then be inserted into a dedicated biasing holder of the TEM [34].

This chip-based technology and sample geometry avoids the problems associated with a nanoprobe contact, the bias being applied in a very similar way to the real device. Furthermore, the top electrode naturally shields the vacuum area above the specimen from the electric field in the active area, making other shielding schemes unnecessary [28,32,35]. These specimen devices are, however, extremely fragile and electrically sensitive. For example, the MOS nanocapacitor studied here has a nominal capacitance of the order of 80 aF. The shielding and electrical protection of the connections from the sample holder to external power supply were therefore an essential part of the instrument development.

One of the other major reasons that local charge distributions have rarely been studied is that the signal is extremely weak. Elementary charges on nanoparticles can indeed be counted using electron holography because the field can be measured in the surrounding vacuum and the exact specimen geometry is known [36]. A working device made by FIB is much more challenging [37]. The methodology for the electron holography experiments also needed to be improved. Part of the solution was achieved by relying on the inherent advantage of *operando* experiments: the device is observed during operation and at rest. Here, operation means applying a constant (dc) bias across the two electrodes to create an electric field across the dielectric capacitor. By grounding the two electrodes, a reference hologram can be recorded that contains all the experimental artifacts: variable lamella thickness, damage layers, diffraction contrast, and electron-beam-induced charging [38,39]. By subtracting the reference signal from the holograms acquired during device operation, the artifacts are removed and the remaining signal can be attributed to the applied electrical biasing. For the experimental data presented in this Letter, this was not sufficient, however. We also needed to profit from the extremely long exposure times made possible by dynamic automation of the electron microscope [40] and smart acquisition routines [41]. Only then can the signal-to-noise ratio in the holograms be at an acceptable level for analysis of the local charges.

The sample device of study [Fig. 1(a)] fashioned by FIB is a thin film of 120-nm-thick thermally grown silicon dioxide on a highly p-doped silicon wafer (10^{18} atom $\cdot$ cm^{-3}) and topped with an electrode of titanium (see Supplemental Material [33]). The lamella thickness was measured to be 55 ± 5 nm. Once connected to the chip with locally deposited platinum and inserted into a dedicated TEM biasing holder, the substrate was grounded while positive, negative, or zero biases were applied *in situ* to the top electrode. Electron holography experiments were carried out in Lorentz mode on an HF3300-C (Hitachi) equipped with a BCOR aberration corrector [42] from CEOS and using two post-specimen biprisms to allow flexibility in the holographic configurations and to eliminate the Fresnel fringe artifacts [43]. Holograms were acquired in the region shown in Fig. 1(b) and the phase calculated. The phase has been corrected for the phase at zero bias, and a region within the silicon substrate was used as an internal reference (see electron holography and hologram analysis in Supplemental Material for experimental details and data analysis [33]). The resulting phase map for a positive bias of 5 V is shown in Fig. 1(c), where we can see the change in phase across the capacitor due to the applied bias.

Phase profiles analysis: In order to improve the signal-to-noise ratio further, phase profiles were averaged over 100 nm parallel to the interface and the results shown in Fig. 2. The phase noise is now less than 10 mrad for a spatial resolution of 0.8 nm. The phase change across the capacitor can be seen clearly and increases linearly with applied bias, as expected from Eq. (1). However, the phase is not constant in the regions corresponding to the electrodes, whereas we would expect the electrodes to be at a uniform potential. This is due to the fact that the phase is also sensitive to the stray field above and below the sample [27]. To interpret the profiles quantitatively, it is therefore necessary to carry out modeling of the electric potential in and around the thin sample.

A feature of particular interest to the analysis is the pronounced step in the phase occurring at both interfaces. The enlargement in Fig. 2 shows that here are two points of inflection, one at the interface plane and another at least 5 nm deep into the dielectric layer. This feature was unexpected and required much exploration to understand its origin.

We therefore carried out extensive finite element method simulations to understand the phase profiles. Our models took into account the specimen geometry, in particular, the lamella thickness and the width of the electrodes, but also the possibility of charge layers in the dielectric. Corresponding phase profiles were obtained by applying Eq. (1) to the simulated electrical potential and internal reference applied as for the experimental case.

The best fit for the 5 V phase profile is shown in Fig. 3. Simulations confirm that the global phase change between the two electrodes (5.5 rad) corresponds exactly to an applied voltage of 5 V measured on the power supply, assuming the measured sample thickness to be correct. From a methodological point of view, this is highly encouraging and suggests that macroscopically applied bias is transmitted to the nanometer-sized active area of the device (the dielectric layer in this case). A large surface damage layer created by FIB would favor a leakage current and a voltage drop through the contact resistances between the sample and the grid. In addition, this means that the

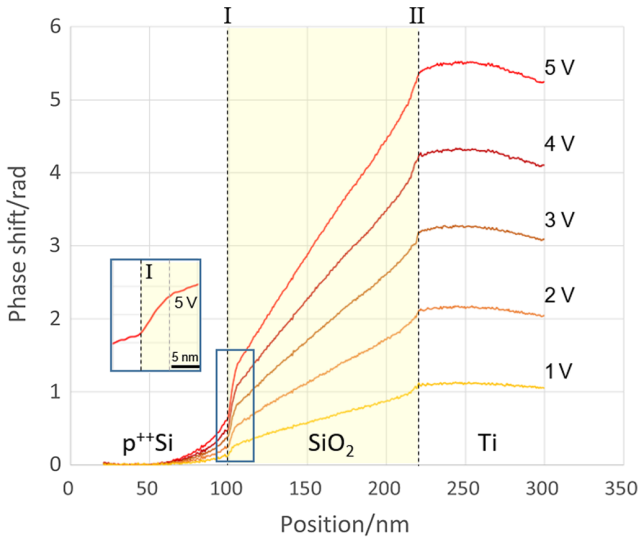

FIG. 2. Phase profiles as function of applied bias (1–5 V). Note the curvature of the phase within the electrodes (highly doped Si and Ti) and the phase jumps at the electrode-dielectric interfaces extending more than 5 nm inside the SiO_2 layer (see enlargement for 5 V bias).

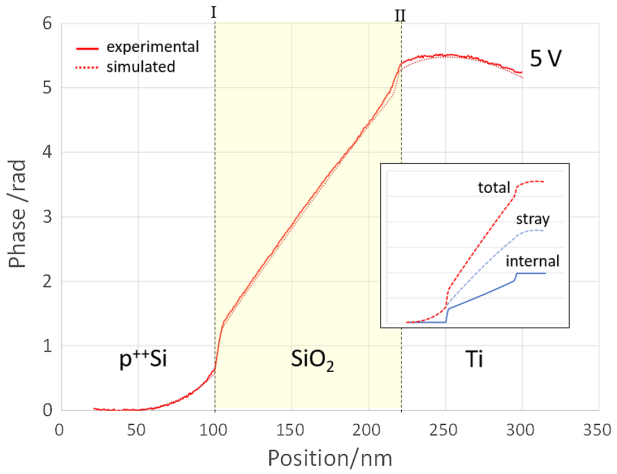

FIG. 3. Finite element method modeling of electric potential in sample device. Experimental phase profile for 5 V bias (red line), best fitting simulation (red dotted line). Inset: simulated phase contributions from internal potential (blue line), stray field (blue dotted line), and total (red dotted line). Potential steps at interfaces caused by dielectric charge layers.

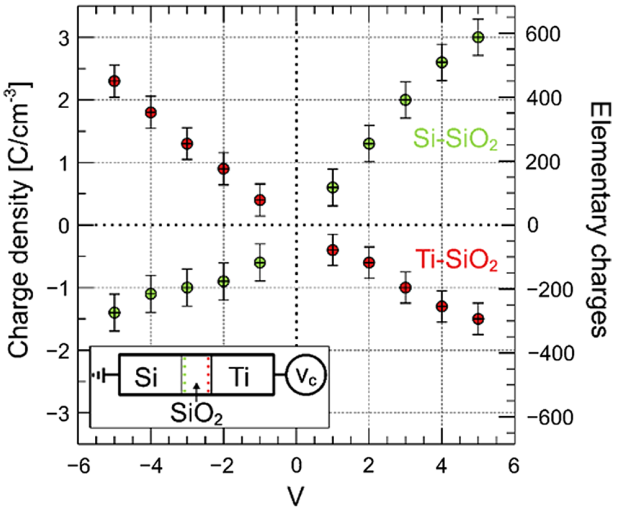

FIG. 4. Dielectric charge as a function of applied bias at Si-SiO_2 and SiO_2-Ti interfaces. Left-hand axis in charges per unit volume. Right-hand axis in number of elementary charges contained in the analyzed region in the experimental specimen device.

phase sensitivity of 10 mrad is equivalent to only 9 mV of applied bias.

Quantification of volume charge densities within the dielectric layer: Analysis also shows that the curvature of the phase in the region corresponding to the electrodes is indeed caused by the stray fields around the thin specimen (see inset in Fig. 3). We see no evidence of a depletion layer in the silicon for a positive bias, which is expected for the high doping level with a thin depletion width (<10 nm for 5 V of applied bias) and a low surface potential (0.1 V). The only way the step in phase at the interface could be modeled successfully, however, was to include a layer of charge within the dielectric layer, similar to double charge layers observed in solid-state batteries [27]. We modeled this as a layer of uniform volume charge over 5.5 nm for both interfaces. Using this model, and by only changing the charge density, we were able to nicely reproduce the experimental profiles for the complete biasing experiment as depicted in Fig. 3.

The charge densities required to fit the experimental data are summarized in Fig. 4, including the negative biasing results. We have also indicated (right-hand scale) the number of elementary charges this represents in the region analyzed and represented by the phase profiles (i.e., 100 nm of interface in the 55-nm-thick lamella) to highlight the sensitivity of the measurements. The error bars reflect the experimental uncertainties, for example, the exact thickness of the lamella, much larger than the effect of the depletion layer for a positive bias. The resolution of the phase profiles is also limited giving our estimate for the width of the charge layers of 5.5 ± 0.5 nm, which in turn introduces a certain interplay between the width of the charge layers and the charge density therein. Nevertheless, given the detailed form of the profiles and the signal-to-noise ratio of the phase, the resulting error bars are contained (Fig. 4), representing sometimes as little as 50 elementary charges in the region analyzed.

Discussion.—It is well known that charges can be trapped in dielectric capacitors. However, it is generally considered that traps are in the immediate vicinity of the interface, that is, within a tunneling distance of 1–2 nm. It is therefore highly surprising that a homogeneous charge layer extends to a distance of over 5 nm from the interface. Furthermore, this distance is much larger than the structural or chemical width of the interface, as verified by high-resolution TEM and electron energy-loss spectroscopy (see Supplemental Material [33]). The second interesting feature is that, contrary to an origin by quantum tunneling, the charge density varies monotonically with the applied bias, with an almost linear dependence, and follows the sign of the applied bias with an opposite sign to the charges on the nearby electrodes. Both negative and positive charges are therefore created on biasing. Overall, more positive charges are created than negative, particularly for the Si-SiO_2 interface. Finally, the density of charge does not depend on the history of the biasing. This was tested experimentally by returning from time to time to previous values of bias within a cycle. In addition, the hologram phase was stable over the acquisition time for each particular bias. All this suggests that the charges within the sample are in thermal equilibrium. Furthermore, the phase profiles are observed to change almost instantaneously on applying bias, suggesting that the equilibrium is attained very quickly.

To explore the implications for a full device, we have developed an analytical description of a capacitor having infinite parallel electrodes but including uniform dielectric charge layers at the interfaces using parameters measured by electron holography. The model also allows us to compare capacitors with and without dielectric charging and gives the electric potential, capacitance, and the electrostatic energy stored in the capacitor. We find a capacitance of 17 nF cm^{-2} compared with an ideal capacitor (without the dielectric charge layers) of 29 nF cm^{-2}, a significant reduction.

The slope of the electric potential corresponds to the electric field and is smaller in the capacitor due to the potential steps created by the charge layers (cf. inset Fig. 3). Indeed, from Gauss's law, the overall charge on the electrode plus the charge layer is reduced with respect to the ideal capacitor. Counterintuitively, the charge on the electrode is in fact much higher, over 10 times that of the ideal capacitor, being compensated by the charges in the dielectric. For example, there are 590 positive charges in the dielectric layer near the interface with silicon for 5 V of bias (cf. Fig. 4). From the model, we can calculate that there are 620 negative charges on the silicon electrode, producing a net charge of only 30 negative charges. In the absence of

dielectric charge, the capacitor would have had 50 negative charges on the silicon electrode.

From a purely electrostatic point of view, the creation of charge layers in the dielectric costs energy. The electrostatic energy stored can thus be calculated as 1.2 μJ cm^{-2} compared with 0.36 μJ cm^{-2} for the ideal capacitor. If we assume that this energy difference is compensated by the charge trapping, this corresponds to 340 meV per trap.

These experiments show the extreme sensitivity of electron holography for the study of charge distributions in operating devices, down to a handful of elementary charges in the region analyzed and 9 mV of applied bias, and opens possibilities for the study of many other types of device. We have shown that the measured capacitance is much less than expected for a capacitor based on SiO_2, the most widely used dielectric. Macroscopic characterization might have attributed a reduction to poor quality of the interfaces or a larger than expected oxide thickness, contrary to what we observed. It should also be noted that our experiments are carried out for dc bias: other techniques are usually carried out at high frequency. The consequences are important however. While the electric field in the bulk of the dielectric layer is lower than expected, the electric field at the interface can be 10 times higher than for the ideal capacitor, with implications for the reliability. A very unexpected finding is that the charge layer extends to over 5 nm from the interface. Our results suggest that the charge trapping mechanisms and charge transfer at interfaces over long timescales needs to be reevaluated.

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