Constant-Overhead Quantum Error Correction with Thin Planar Connectivity

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Quantum low density parity check (LDPC) codes may provide a path to build low-overhead fault-tolerant quantum computers. However, as general LDPC codes lack geometric constraints, naïve layouts couple many distant qubits with crossing connections which could be hard to build in hardware and could result in performance-degrading crosstalk. We propose a 2D layout for quantum LDPC codes by decomposing their Tanner graphs into a small number of planar layers. Each layer contains long-range connections which do not cross. For any Calderbank-Shor-Steane code with a degree-δ Tanner graph, we design stabilizer measurement circuits with depth at most $(2\delta + 2)$ using at most $\lceil \delta/2 \rceil$ layers. We observe a circuit-noise threshold of 0.28% for a positive-rate code family using 49 physical qubits per logical qubit. For a physical error rate of 10^{-4}, this family reaches a logical error rate of 10^{-15} using fourteen times fewer physical qubits than the surface code.

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Quantum error correction (QEC) is typically implemented by measuring Pauli operators called *stabilizer generators* of a QEC code to detect faults. In quantum low density parity check (LDPC) codes, the stabilizer generators have low weight, making them easier to implement than general codes. Some quantum LDPC codes also have positive-rate, allowing them to achieve arbitrarily low logical error rates with a constant ratio of tens of physical qubits per logical qubit. For large computations, this can correspond to more than 1 order of magnitude lower qubit overhead than alternative codes with vanishing rate such as the surface code. However, these positive-rate LDPC codes have nonlocal stabilizer generators [1,2] making them somewhat daunting to implement in hardware. In this Letter, we seek a practical implementation of positive-rate quantum LDPC codes which performs well in a full circuit-level noise analysis.

To clarify our discussion, we define the *connectivity graph* of a quantum circuit, with vertices corresponding to qubits and edges connecting qubits coupled by circuit operations. We can further define a *layout* as a specification of the physical locations of the connectivity graph's qubits and connections. In this Letter, we are interested in circuits which measure the stabilizer generators of a QEC code. Given a family of codes, we focus on constant-depth stabilizer measurement circuits to avoid a buildup of errors which could spoil any fault-tolerance threshold.

A natural first question is if the nonlocal stabilizer generators of positive-rate quantum LDPC codes can be measured using a circuit with local connectivity in a 2D qubit layout. In recent work [3], we show that although a single nonlocal stabilizer can be measured in constant depth, the full set of stabilizer generators cannot be collectively measured in constant depth without the ratio of logical to physical qubits vanishing.

Given that a 2D qubit layout with local connectivity is excluded for positive-rate quantum LDPC codes, we consider quantum hardware equipped with some set of long-range connections. With unrestricted connections, one could simply lay out the code qubits in a 2D grid along with an ancilla for each stabilizer generator that has connections to the code qubits in that stabilizer's support. However, this typically results in an unbounded number of crossing

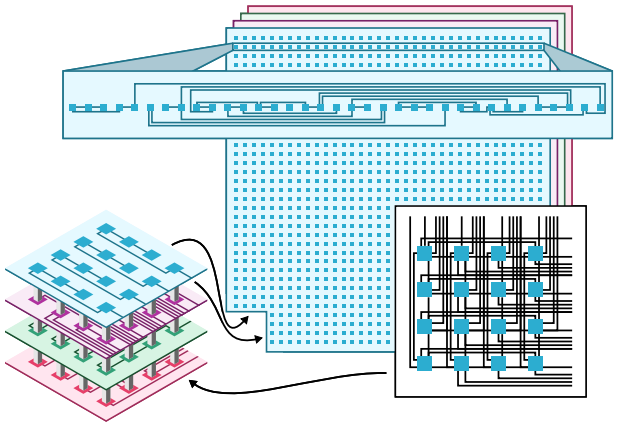

FIG. 1. A crossing-free planar layout for hypergraph product codes with four layers. Stabilizer generators are measured using circuits built from single-qubit operations and CNOT gates between qubits connected by an edge. The top two layers have edges connecting qubits in the same row as shown in the enlargement, while the lower two layers have edges connecting qubits in the same column. Each layer is planar, such that no pair of edges cross. For comparison, the lower right box shows the nonplanar connections passing through the lower-left corner before the decomposition, which exhibits many crossings.

connections [4,5]; see Fig. 1. In many hardware platforms, in addition to being challenging to implement, crossing connections can spread error through crosstalk [6–9]. This raises the following question:

Can we construct high-threshold constant-depth stabilizer measurement circuits for positive-rate quantum LDPC codes in a 2D qubit layout without crossings in the two-qubit gate connectivity?

In this Letter, we provide a positive answer to this question through the design of an l-planar layout, consisting of qubits placed in a 2D grid, with edges separated into $l = \mathrm{O}(1)$ planar layers, with no crossings in each layer; see Fig. 1. Furthermore, we provide a circuit construction consistent with this layered planar architecture to measure the stabilizer generators of any Calderbank-Shor-Steane (CSS)-type [10,11] quantum LDPC code in constant depth.

Theorem 1.—Let Q be a CSS code such that each stabilizer generator has weight at most δ and each qubit is involved in at most δ stabilizer generators. Then, one can implement the measurement of all the stabilizer generators of Q with a circuit with depth $2\delta + 2$ using a $\lceil \delta/2 \rceil$-planar layout.

Below, after proving this theorem, we refine these results by specializing to a family of quantum codes known as hypergraph product (HGP) codes [12] which are constructed from a pair of input graphs. In this case, we find a low-depth stabilizer measurement circuit which reduces to the standard circuit in the case of surface codes (Surface codes are HGP codes formed when the input graphs are the Tanner graphs of a pair of repetition codes) [13]. Moreover, we prove in Lemma 1 that the circuit depth can be reduced to $\delta + 2$ when the vertices of the input graphs of the HGP code admit a balanced ordering.

Lastly, we numerically explore the performance of these circuits for a family of HGP codes using the decoding routine of Grospellier and Krishna [14], but replacing their idealized noise model with circuit noise. Using our layered planar connectivity, we obtain a circuit-noise threshold of $2.8(2) \times 10^{-3}$, providing strong evidence that these codes can offer a significant advantage over surface codes which have a comparable threshold.

Quantum LDPC codes.—All the quantum codes we consider in this work are CSS codes [10,11]. Recall that a CSS code with length n is defined by a set of commuting stabilizer generators $s_{X,1}, \ldots, s_{X,r_X}, s_{Z,1}, \ldots, s_{Z,r_Z}$ with $s_{X,i} \in \{I, X\}^n$ and $s_{Z,j} \in \{I, Z\}^n$. The *X Tanner graph* is the bipartite graph $T_X = (V, E)$ whose vertex set is $V = V_q \cup V_X$ where $V_q = \{q_1, \ldots, q_n\}$ is the qubit set and $V_X = \{s_{X,1}, \ldots, s_{X,r_X}\}$. There is an edge between q_i and $s_{X,j}$ if and only if $s_{X,j}$ acts nontrivially on qubit q_i. The Z Tanner graph T_Z is defined similarly from the Z stabilizer generators, and the overall Tanner graph is their union $T = T_X \cup T_Z$. The code is a quantum LDPC code if the Tanner graph has bounded degree. Quantum error correction works by measuring all the stabilizer generators and applying a correction based on the outcomes observed. Our goal is to design practical stabilizer measurement circuits for quantum LDPC codes.

We first show that quantum circuits with a low-degree connectivity graph can be implemented with a layered planar connectivity using a small number of layers. This result applies to any quantum circuit (not just stabilizer measurement circuits) and in particular to all low-depth quantum circuits.

Proposition 1.—Let C be a circuit made with single-qubit and two-qubit operations whose connectivity graph has degree at most δ. Then, C can be implemented with a $\lceil \delta/2 \rceil$-planar layout.

Proof.—This follows directly from the fact that for any graph with degree at most δ, the smallest edge partition such that each subgraph is planar involves at most $\lceil \delta/2 \rceil$ subgraphs [15,16]. Furthermore, since any planar graph can be drawn with arbitrary vertex location [17], we can fix the position of each qubit across layers. ∎

We now introduce the *coloration circuit* associated with an edge coloration of a Tanner graph that can be used for any CSS code. (Reference [18] previously proposed a scheduling of gates based on a vertex coloring. The advantage of our approach is that the edge coloring we use can be computed efficiently while the vertex coloring problem of Ref. [18] is NP hard.) An *edge coloration* of a graph is a coloration of the edges such that incident edges support distinct colors. We will often consider a *minimum edge coloration*, that is, an edge coloration with a minimum number of colors.

Algorithm 1. Coloration circuit.

input : A minimum edge coloration $\mathcal{C}_X$ of T_X.
output: The measurement outcome of all X stabilizer generators.
1 Prepare an ancilla in $|+\rangle$ for each generator $s_{X,i}$.
2 **for** color $c \in \mathcal{C}_X$ **do**
3 Simultaneously apply all gates $\mathrm{CNOT}_{i \to j}$ from the ith ancilla to the jth data qubit supported on an edge $\{i, j\}$ with color c.
4 Measure each ancilla in the X basis.

Proposition 2.—Let Q be a CSS code with X Tanner graph T_X. Then, the coloration circuit measures all the X stabilizer generators of Q in depth $\deg(T_X) + 2$.

Proof.—The controlled-not (CNOT) applied in step 3 can be applied simultaneously because they correspond to edges with the same color, guaranteeing they have disjoint support. We see the circuit measures the X generators by rearranging the CNOTs, which commute, to form a sequence of single-generator measurement circuits. Each such circuit prepares an ancilla in $|+\rangle$, applies CNOTs from the ancilla to the generator's support, and then measures the ancilla in the X basis. The depth of the coloration circuit is $\deg(T_X) + 2$ because the Tanner graph, which is bipartite, admits an edge coloration with $\deg(T_X)$ colors [19]. ∎

Swapping X and Z provides a Z stabilizer measurement circuit with depth $\deg(T_Z)+2$. We now prove Theorem 1.

Proof of Theorem 1.—By Proposition 1, a circuit extracting both X and Z syndromes with depth $\deg(T_X)+\deg(T_Z)+2$ is formed by running the X and then the Z circuit with two overlapping time steps. The connectivity graph of the cardinal circuit has degree $\deg(T)$. Therefore, Proposition 1 proves the existence of a $\lceil \deg(T)/2 \rceil$-planar layout. ∎

This depth may be further reduced by compressing the circuit, interleaving X and Z stabilizer measurements. However, the design of such a compression is nontrivial because the CNOT gates involved in X and Z measurements do not commute. Now we specialize to HGP codes for which we provide an interleaved X/Z stabilizer measurement circuit.

Hypergraph product codes.—The HGP code $HGP(G_1, G_2)$ [12] is defined from the Cartesian product $G_1 \times G_2$ of two bipartite graphs [Fig. 2(a)]. For $m \in \{1,2\}$, let $V_m = B_m \cup C_m$ be the vertex set of G_m and E_m be its edge set. The edges of E_m connect a vertex of B_m with a vertex of C_m. We assume that each vertex of G_m is given by a label $i = 1, \ldots, |V_m|$. Each pair $(i,j) \in B_1 \times B_2 \cup C_1 \times C_2$ represents a data qubit of the HGP code while each pair (i,j) in $B_1 \times C_2$ (resp. $C_1 \times B_2$) corresponds to an X (respectively Z) stabilizer generator. The stabilizer generator with label (i,j), denoted $S_{(i,j)}$ is supported on the qubits with label (i',j) where $\{i',i\} \in E_1$ and (i,j') with $\{j,j'\} \in E_2$. To avoid confusion with the coordinates introduced later which specify the physical locations of qubits in a 2D layout, we refer to the pair (i,j) as a data qubit label or stabilizer generator label.

We associate a direction **N**, **S**, **E**, **W** with each edge. An edge between stabilizer vertex (i,j) and qubit vertex (i,j') with $j' = j + \ell \pmod{|V_1|}$ has direction **N** if $0 < \ell \leq |V_1|/2$ and direction **S** otherwise. We define the directions **E** and **W** similarly for edges between stabilizer and qubit vertices (i,j) and (i',j). For each direction $\mathbf{D} \in \{\mathbf{N},\mathbf{S},\mathbf{E},\mathbf{W}\}$, we consider the subgraph $T_{\mathbf{D}}$ of the Tanner graph T induced by the edges with direction **D**.

The following circuit interleaves X and Z measurements and can achieve a depth lower than the coloration circuit.

Algorithm 2. Cardinal circuit.

input : A minimum edge coloration $\mathcal{C}_{\mathbf{D}}$ of $T_{\mathbf{D}}$.
output: The outcome of the measurement of all the X and Z stabilizer generators.

1 Prepare an ancilla in $|+\rangle$ for each X stabilizer generator and an ancilla in $|0\rangle$ for each X stabilizer generator.
2 **for** *direction* $\mathbf{D} \in \{\mathbf{E},\mathbf{N},\mathbf{S},\mathbf{W}\}$ **do**
3 **for** *color* $c \in \mathcal{C}_{\mathbf{D}}$
4 Simultaneously apply all CNOT gates supported on an edge of $T_{\mathbf{D}}$ with color c.
5 Measure each X and Z ancilla in the X and Z basis respectively.

Note that the CNOT is either aligned or antialigned with an edge depending on the type of the stabilizer. The control qubit of the CNOT is the ancilla for X stabilizers, and it is the data qubit for Z stabilizers.

Proposition 3.—Let Q be a hypergraph product code with Tanner graph T. Then, the cardinal circuit implements the measurement of all the stabilizer generators of Q in depth $\deg(T_{\mathbf{N}}) + \deg(T_{\mathbf{S}}) + \deg(T_{\mathbf{E}}) + \deg(T_{\mathbf{W}}) + 2$.

Proof.—It is easy to check that the depth of the cardinal circuit is $\deg(T_{\mathbf{N}}) + \deg(T_{\mathbf{S}}) + \deg(T_{\mathbf{E}}) + \deg(T_{\mathbf{W}}) + 2$. This is because the bipartite graph $T_{\mathbf{D}}$ admits an edge coloration with $\deg(T_{\mathbf{D}})$ colors [19].

We now prove by induction that the cardinal circuit measures the stabilizer generators. Denote by C_m the circuit obtained by applying the cardinal circuit construction to the subset of stabilizer generators $s_1, \ldots, s_m$. Clearly, for $m = 1$, the circuit $C(s_1)$ measures the stabilizer generator s_1. We will show that the concatenation of C_m and $C(s_{m+1})$, that we denote $C_m C(s_{m+1})$, has the same action as C_{m+1}.

If all the CNOT gates of $C(s_{m+1})$ commute with all the CNOTs of C_m, we can simply reorder the CNOTs of the circuit $C_m C(s_{m+1})$ to obtain the cardinal circuit C_{m+1}. Assume now that some CNOT gates of $C(s_{m+1})$ do not commute with the gates of C_m. Again, we would like to put the CNOT of $C_m C(s_{m+1})$ in the cardinal order, but swapping these CNOTs produces extra CNOTs as one can see in Fig. 2(d). We will show that these extra CNOTs cancel out.

If s_{m+1} is a Z stabilizer, the corresponding CNOTs only fail to commute with CNOTs associated with the previous X stabilizer generators s_i that overlap with s_{m+1}. Swapping these CNOTs produces an extra gate $\mathrm{CNOT}_{s_i \to s_{m+1}}$ as shown in Fig. 2(c). By the hypergraph product construction, if

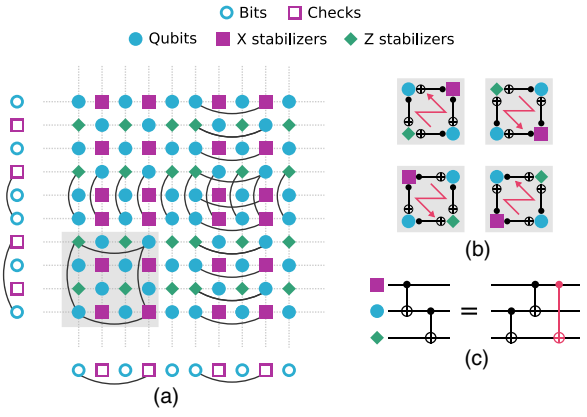

FIG. 2. (a) The Tanner graph of an HGP code is the Cartesian product of two bipartite input graphs. Here qubits are displayed according to their label, which does not correspond to their physical location in the 2D layout. (b) The four possible configurations in which an X and a Z stabilizer can overlap. Red arrows show the cardinal circuit ordering. (c) The commutation of a pair of CNOT gates.

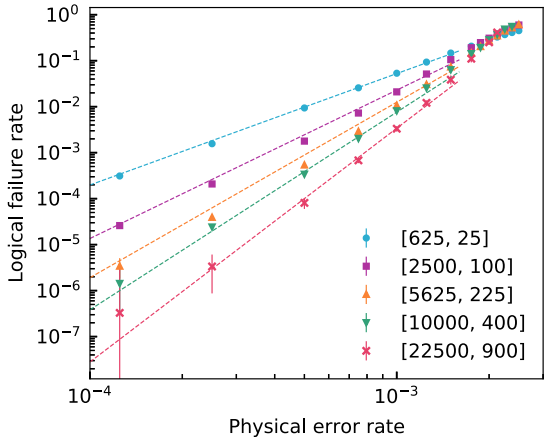

FIG. 3. The failure rate per round averaged over ten successive rounds of error correction. The dashed lines are obtained using $P_L(p,k) = c_1(p/p_t)^{c_2 k^{c_3}}$ finding fitting constants $c_1 = 0.64$, $c_2 = 1.3$, $c_3 = 0.21$ and the threshold $p_t = 2.8(2) \times 10^{-3}$.

s_{m+1} overlaps with an X stabilizer generator s_i, their overlap contains exactly two qubits, in one of the four possible configurations of Fig. 2(b). To bring the CNOTs into cardinal order, we need to perform either 0 or 2 swaps between the CNOTs of s_{m+1} and s_i. This results in two consecutive CNOT gates $\mathrm{CNOT}(s_i, s_{m+1})$ which cancel out. Thus, reordering the CNOT gates in $C_m C(s_{m+1})$ to produce C_{m+1} preserves the action of the circuit. A similar argument applies when s_{m+1} is an X stabilizer generator. Applying this inductively starting with a single stabilizer generator, we reach the cardinally ordered circuit proving that it has the same action as the initial stabilizer measurement circuit. ∎

From Proposition 3 we see that the cardinal circuit only has a lower depth than the coloration circuit if the Tanner subgraphs T_D have sufficiently low degree. To ensure this, we must order the vertices (i,j) of the Tanner graph to distribute the edges more equally between the four directions around each vertex. This motivates the notion of balanced ordering that we introduce now.

A *balanced ordering* for a graph $G = (V, E)$ is a labeling of the vertices by integers $i = 1, \ldots, |V|$ such that for each vertex i we have $\delta_+(i) - \delta_-(i) = [\delta(i) \bmod 2]$ where $\delta_+(i)$ is the number of vertices connected to i of the form $(i + \ell) \pmod{|V|}$ with $0 < \ell \leq |V|/2$ and $\delta_-(i) = \delta(i) - \delta_+(i)$. When the graph is not clear from the context, we will use the notation $\delta_\pm(G, i) = \delta_\pm(i)$. The following lemma is proven in the Supplemental Material [20].

Lemma 1.—Let $Q = \mathrm{HGP}(G_1, G_2)$ be a hypergraph product code. Then, we have

$$\deg(T) \leq \sum_{\mathbf{D}=\mathbf{N},\mathbf{S},\mathbf{E},\mathbf{W}} \deg(T_{\mathbf{D}}) \leq 2\ \deg(T).$$

TABLE I. Total number of data and ancilla qubits required to achieve specific logical failure rates with a physical error rate of 10^{-4} using surface codes and HGP codes. The HGP code data are found from an extrapolation of the fits in Fig. 3, while the surface code data are estimated using the formula $P'_L(p,k,d) = ak(p/p'_t)^{(d+1)/2}$ with optimistic values of $p'_t = 0.011$ and $a = 0.03$ from Ref. [13] and Ref. [25].

Logical failure rate	10^{-9}	10^{-12}	10^{-15}
Logical qubits	1600	6400	18 496
Surface code physical qubits	387 200	2 880 000	13 354 112
HGP code physical qubits	78 400	313 600	906 304
Improvement using HGP codes	4.94×	9.18×	14.73×

Moreover, if G_1 and G_2 have only even degree vertices and admit a balanced ordering, then the lower bound is tight.

For HGP codes based on even, balanced graphs, this lemma, combined with Proposition 3, proves that the depth of the cardinal circuit is about half that of the coloration circuit.

Numerical results.—We use the standard circuit noise model to simulate the performance of a family of HGP codes with parameters $[[25s^2, s^2]]$, i.e., encoding $k = s^2$ logical qubits into $n = 25s^2$ physical qubits; see Fig. 3. This code family has stabilizer generators of weight 7, and each qubit is contained in the support of either six or eight stabilizer generators. The syndrome extraction is performed with the cardinal circuit using $24s^2$ ancilla qubits.

We use a simple extrapolation of the data to estimate a threshold of $p_t = 2.8(2) \times 10^{-3}$ and compare the qubit overhead with that of the surface code in Table I. Based on our simulation, we propose the heuristic formula

$$P_L(p,k) = c_1(p/p_t)^{c_2 k^{c_3}} \tag{1}$$

where $c_1 = 0.64$, $c_2 = 1.3$, $c_3 = 0.21$, and $k = 24s^2$ to provide an estimate of the logical failure rate per round with physical error rate $p < p_t$. Further details on our numerical approach including the code construction [21], the noise model, belief propagation [22,23], and small set flip decoding [24] can be found in the Supplemental Material [20].

Outlook and hardware challenges.—We have shown that syndrome extraction can be implemented in constant depth using a planar layout for any CSS quantum LDPC code, including HGP codes, but also many other families of interest including hyperbolic codes [26] and homological product codes [27]. Our design simultaneously seeks to minimize the depth of the stabilizer measurement circuit which achieves faster quantum error correction and reduces the time allowed for error buildup, while also avoiding crossings of the connections that couple qubits which is expected to improve fabrication and reduce crosstalk. Further improvements could come from optimizing the

circuit to minimize the spreading of errors [28] using better decoders [29–32], or by leveraging improved planar graph algorithms. Moreover, it would be interesting to further study logical operations for quantum LDPC codes [33–36].

We hope that these significant quantum error-correction advantages will motivate experimental teams to overcome the challenges to build quantum hardware in planar layouts. We foresee two major obstacles. Firstly, our design requires a number of long-range links within each layer. Significant experimental progress has been made in that direction using for instance photonic couplings to establish long-range connections [37–44] but it is unclear which of these approaches could be scaled to larger systems. Secondly, there is a tension between the need for insulation between the layers to reduce crosstalk and the fact that data qubits must participate in all layers.

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