Supercompact Photonic Quantum Logic Gate on a Silicon Chip

Ming Zhang,[1,*] Lantian Feng,[2,3,*] Ming Li,[1] Yang Chen,[2,3] Long Zhang,[1] Deyong He,[2,3] Guoping Guo,[2,3] Guangcan Guo,[2,3] Xifeng Ren,[2,3,†] and Daoxin Dai[1,‡]

[1]*State Key Laboratory for Modern Optical Instrumentation, College of Optical Science and Engineering, Ningbo Research Institute, International Research Center for Advanced Photonics, Zhejiang University, Hangzhou 310058, China*

[2]*Key Laboratory of Quantum Information, CAS, University of Science and Technology of China, Hefei, Anhui 230026, China*

[3]*Synergetic Innovation Center of Quantum Information and Quantum Physics, University of Science and Technology of China, Hefei, Anhui 230026, China*

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To build universal quantum computers, an essential step is to realize the so-called controlled-NOT (CNOT) gate. Quantum photonic integrated circuits are well recognized as an attractive technology offering great promise for achieving large-scale quantum information processing, due to the potential for high fidelity, high efficiency, and compact footprints. Here, we demonstrate a supercompact integrated quantum CNOT gate on silicon by using the concept of symmetry breaking of a six-channel waveguide superlattice. The present path-encoded quantum CNOT gate is implemented with a footprint of $4.8 \times 4.45\ \mu m^2$ ($\sim 3\lambda \times 3\lambda$) as well as a high-process fidelity of ~ 0.925 and a low excess loss of <0.2 dB. The footprint is shrunk significantly by $\sim 10\,000$ times compared to those previous results based on dielectric waveguides. This offers the possibility of realizing practical large-scale quantum information processes and paving the way to the applications across fundamental science and quantum technologies.

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The quantum controlled-NOT (CNOT) gate is one of the most important quantum elements and lies at the heart of quantum information [1–4]. It flips the state of the target qubit conditioned on the state of the control qubit. Together with single-qubit quantum operations, it is possible to form all set of gates for the universal quantum computation [2]. In 2001, Knill *et al.* proposed a nondeterministic CNOT gate scheme, which only requires single photons and beam splitters, as well as interferometers, and thus is very suitable for linear optical systems [5]. The first demonstration of this kind of CNOT gate was given by using bulk optical devices in 2003 [6], and it has subsequently been extended [7,8]. However, these bulky gates suffer from poor scalability, instability, and noncompactness. For example, the footprints of bulky CNOT gates are usually in the scale of decimeters [6]. In contrast, photonic integrated circuits (PICs) provide a practical platform for implementing quantum photonic devices and circuits (including CNOT gates) with the natural advantages on scalability, stability, and cheapness [9–17]. Currently this attractive and feasible technology has been utilized for many complicated quantum photonic chips [18–22]. In particular, on-chip CNOT gates have been realized with SiO_2 buried waveguides [3], laser-written glass waveguides [12], and silicon-on-insulator (SOI) nanophotonic waveguides [23] for path- or polarization-encoded photons since 2008.

One should note that the footprint of quantum PICs (QPICs) grows rapidly with the number of quantum gates and the complexity of quantum tasks, which are indispensable for large-scale quantum information processing [24]. To simulate an arbitrary n qubit quantum information process, the theoretical lower bound for the number of CNOT gates needed is given by $N = (4^n - 3n - 1)/4$ [25], which shows that the number N increases exponentially with the quantum-state complexity. This requires one to integrate many photonic components on an ultracompact chip, and thus it is extremely important to reduce the size of photonic components. However, for those reported quantum logic gates based on dielectric waveguides, the footprints are still on the scale of $\sim 10^5\ \mu m^2$ due to the long coupling region, wide decoupling regions, and large bending radii. The noncompactness of quantum logic gates strongly prevents further realization of large-scale QPICs. For example, even for an arbitrary 2-qubit quantum gate, which includes three CNOT gates and many single-qubit gates [26], the QPIC occupies a footprint of several square centimeters. When one tries to realize more complicated quantum algorithms, the QPIC might be even as large as hundreds of square centimeters, which challenges the current fabrication technology. A possible way to reduce the QPIC footprint is to utilize plasmonic waveguides, which enables nanoscale mode confinement [10,27]. As presented in Refs. [10,27], the single-photon quantum interference and on-chip CNOT gates have been experimentally demonstrated with a footprint of about, e.g., $14 \times 14\ \mu m^2$ by introducing plasmonic nanostructures. However, the light coupling to and from the plasmonic chip is inconvenient and lossy. Additionally, the inherent loss of

plasmonic nanostructures limits not only the efficiency but also the fidelity of quantum gates [28]. A summarization of the representative results of quantum photonic CNOT gates is given by Fig. S1 in the Supplemental Material [29].

In this Letter, we report an integrated supercompact quantum CNOT gate on silicon with a footprint as small as $4.8 \times 4.45\ \mu m^2$ ($\sim 3\lambda \times 3\lambda$), which is $\sim 10\,000$ times smaller than those previous integrated quantum CNOT gates based on dielectric waveguides. Our CNOT gate is even 10 times smaller than the plasmonic quantum CNOT gate in Ref. [10], while the latter bears intrinsically high losses, low fidelity (e.g., ~0.638), and difficulty for scaling. The present supercompact quantum CNOT gate is realized by breaking the symmetry of an ultradense waveguide superlattice. In this way, one can flexibly manipulate the coupling and decoupling processes occurring in a six-channel silicon photonic waveguide array. The separation between the waveguide in the array is less than 800 nm, which helps achieve supercompact CNOT gates. Our scheme does not require any special fabrication process and is fully compatible with SOI waveguide structures used commonly. To characterize the present CNOT gate, we measured the truth table and demonstrate on-chip generation of all the four Bell states. The on-chip excess loss of the CNOT gate is <0.2 dB in theory. Furthermore, the quantum process tomography was obtained with a fidelity result of 0.925 by using on-chip Mach-Zehnder interferometers (MZIs) and thermal-tuning phase shifters. Our protocol can be generalized to realize other quantum information processes, such as quantum photon sources preparation, quantum boson sampling, and quantum random walk, and thus plays an important role to step forward in photonic quantum information processing.

Figure 1(a) shows the working principle of a quantum CNOT gate. In this Letter, we use path-encoded photons and exploit the quantum interference between photons to build up the CNOT gate [11], as shown in Fig. 1(b). Here a special target bit encoding method was used. The kernel of the CNOT gate is mainly formed by the power splitters, in which the state of the target photon is flipped depending on whether there is quantum interference between the control and target photons. The quantum states $|0\rangle_c$ and $|1\rangle_c$ of the control photon are encoded to the path mode in the optical waveguides labeled by C_0 and C_1, respectively. The quantum states $|0\rangle_T$ and $|1\rangle_T$ of the target photon are encoded to the superposition path modes $1/\sqrt{2}(T_0 + T_1)$ and $1/\sqrt{2}(T_0 - T_1)$ in the optical waveguides labeled by T_0 and T_1, respectively. For simplicity, the subscripts are dropped in the following part and, for example, the presence of each photon in waveguides C_0 and $1/\sqrt{2}(T_0 - T_1)$ is labeled by the state $|01\rangle$. In this scheme, the gate is operating as an unheralded type of CNOT gate. Only when there is detection of a photon in both control and target outputs, the operation of the gate is logically meaningful and the successful probability of the gate operation is $P = 1/9$. A postselected method was adopted after the quantum interference in the beam splitters, on the event that only one photon appears in the control qubit waveguides (C_0, C_1) and one photon in the target qubit waveguides (T_0, T_1) [31]. Note that the present waveguide-superlattice-based gate operation can be further extended to a heralded type of CNOT gate by using additional beam splitters and two more ancilla photons [22].

For this type of CNOT gate, there are six input-output ports and three optical couplers with a power splitting ratio of $1/3:2/3$ between the through and cross ports. The two input-output ports located at the top and bottom edges are auxiliary, as shown in Fig. 1(b). The desired power splitting

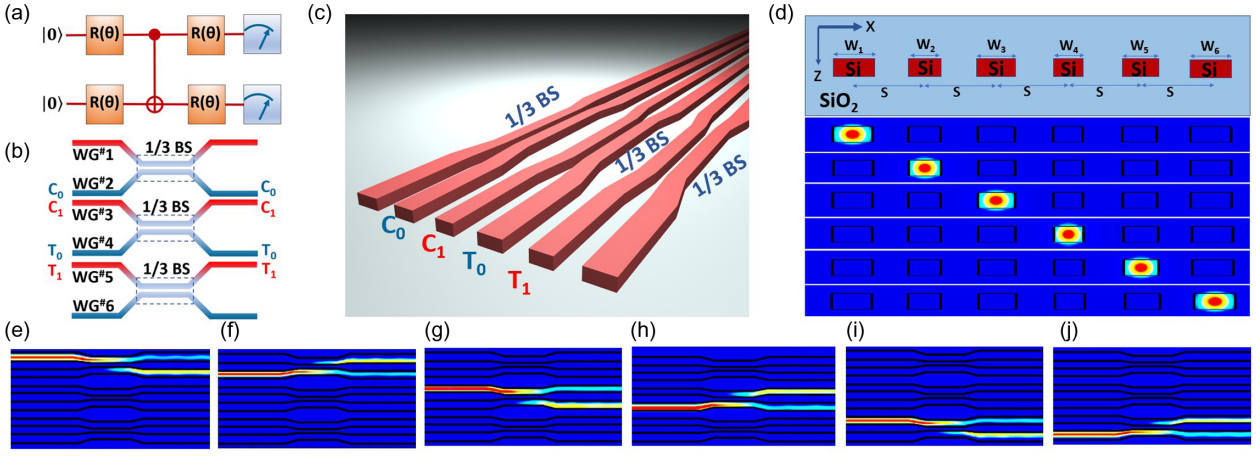

FIG. 1. The proposed quantum CNOT gates. (a) Principle of a quantum CNOT gate. (b) Diagram of the CNOT gate for path-encoded photons, including three beam splitters (BS) with a power splitting ratio of $1/3:2/3$. (c) Configuration of the present CNOT gate. (d) Cross section of the superlattice waveguides in the input-output section and the corresponding localized supermodes. (e)–(j) Simulated light propagation in the designed superlattice waveguides (WGs) when light is, respectively, launched from waveguide Nos. 1–6.

ratio can be realized by choosing the length L_c of the coupling region optimally for the directional couplers used. In order to obtain the desired mode coupling and minimize the footprint, the width of the gaps in the coupling regions should be reduced. On the other hand, the input-output ports should be separated with a sufficiently large separation D to avoid undesired mode coupling in the decoupling regions. For example, the separation D is usually as large as several microns (or even tens of microns). The coupling and decoupling sections of the waveguide array are usually connected by introducing some S bends. Thus, traditionally the CNOT gate has a large footprint, as shown in previous works.

In order to realize supercompact on-chip CNOT gates, here we propose a novel structure design with silicon superlattice waveguides, as shown in Fig. 1(c). In particular, the mode coupling in the silicon superlattice waveguides are manipulated effectively by the symmetry-breaking strategy. When the symmetry-breaking is introduced by choosing different core widths for the silicon superlattice waveguides, significant mode localization happens due to the strong phase mismatch. As a result, these superlattice waveguides become decoupled even when they are arranged very densely [32–34]. For example, the separation between adjacent waveguides in the decoupling regions can be as small as the half-wavelength scale (e.g., $\sim 0.8\ \mu$m at $\lambda = 1.55\ \mu$m). This is very promising for the realization of high-density integration of optical waveguides. On the other hand, it is still effective to achieve some coupling between some adjacent waveguides as desired for CNOT gates. In our case the power splitting ratio between the adjacent waveguides Nos. (1, 2), (3, 4), (5, 6) is required to be $1/3:2/3$. In order to realize this, it is necessary to reduce the mode localization and enhance the mode coupling, which can be obtained by modulating the core widths of the adjacent waveguides to be identical or similar according to the phase matching condition.

According to this rule, the present supercompact on-chip CNOT gate is designed with six silicon photonic waveguides, consisting of the coupling regions and the input-output sections based on superlattice waveguides, as shown in Fig. 1(c). The core widths and gap widths for these waveguides in the input-output sections and the coupling regions are designed carefully to achieve the mode localization (decoupling) and the mode coupling, respectively. At the input-output sections, the silicon superlattice waveguides are nonuniform by carefully choosing different core widths, i.e., w_1, w_2, w_3, w_4, w_5, and $w_6 = 450$, 390, 330, 420, 360, and 450 nm. With this design, there is significant phase mismatching among them. As a result, strong mode localization happens and thus the evanescent coupling between the adjacent and nonadjacent optical waveguides are depressed greatly even when the adjacent waveguides separation is as small as 0.8 μm [see Fig. 1(d)]. To characterize the cross talk performance of superlattice waveguides, we fabricated a group of superlattice waveguides with 100-μm-long distance, and the maximal coupling cross talk is less than -28 dB in the wavelength range from 1530 to 1600 nm (see Fig. S2 in the Supplemental Material [29]). This indicates these superlattice waveguides enable excellent mode localization (decoupling) as the theoretical analysis predicted.

In contrast, the core widths for these six waveguides in the coupling region are chosen to be the same, so that there is no phase mismatching and sufficient coupling can be achieved. Here we set the core width as $w = 330$ nm in order to avoid high scattering losses at the sidewalls. Meanwhile, the width for the gaps is chosen to be as small as 200 nm, which is the minimal value allowed in our fabrication process. In this way, it is helpful to enhance the evanescent coupling and minimize the length of the coupling region. In order to connect the six nonuniform superlattice waveguides in the input-output sections and the six waveguides in the coupling region, asymmetric linear tapers are introduced for achieving low-loss mode conversion between them. According to the 3D finite-difference time domain (FDTD) simulation (see Fig. S3), the length of the tapers is chosen as short as 1.0 μm and the corresponding excess loss is negligible in a broadband.

In this design, the length of the coupling region is optimized according to 3D-FDTD simulation. It can be seen that the optimal coupling length L is about 2.8 μm for achieving the desired power splitting ratio of $1/3:2/3$ (see Fig. S4). For the designed CNOT gate, the total footprint is as small as $4.8 \times 4.45\ \mu\text{m}^2$. The light propagation in the designed structure consisting of the superlattice waveguides and the coupling regions is then simulated when light is, respectively, launched from the left side of waveguide Nos. 1–6, as shown in Figs. 1(e)–1(j).

In order to characterize the performance of the CNOT gates, a silicon QPIC was designed with the part for the state preparation, as well as the part for the state analysis on the same chip, as shown in Fig. 2(a). Here the configurations of these two parts are similar. Each of them consists of two thermally tuned phase shifters and two MZIs. Each MZI is composed of a phase shifter and two 2×2 3 dB multimode-interference couplers, so that any unitary transformation in SU(2) can be realized (l). Such an architecture enables reconfigurable single-qubit unitary operations, and one can characterize arbitrary 2-qubit quantum states when working together with projection measurement. The designed PIC consisting of the CNOT gate was fabricated with very simple processes. Figure 2(b) shows the microscope picture of the whole chip and Fig. 2(c) shows the SEM image for the supercompact CNOT gate with a supercompact footprint of $4.8 \times 4.45\ \mu\text{m}^2$.

Figure 2(f) shows the experimental setup consisting of the silicon QPIC and some off-chip components. The off-chip components include the quantum photon pair source, the single-photon detectors, and the coincidence measurement devices. The quantum photon pair source was produced from type-II spontaneous parametric down-

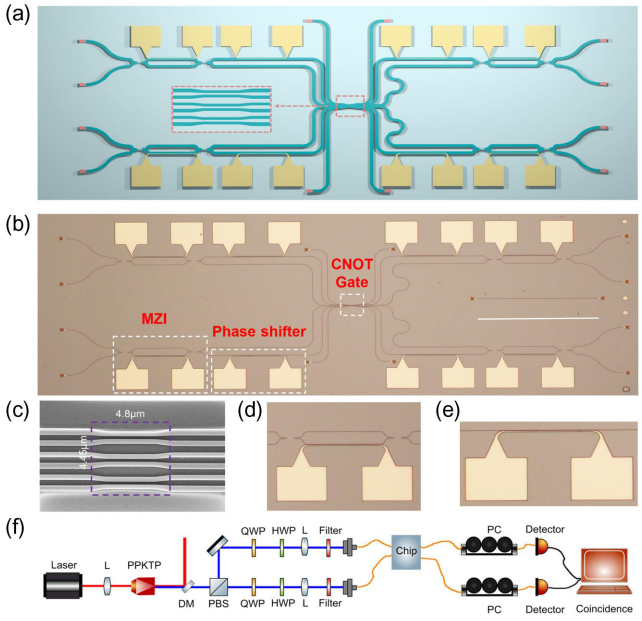

FIG. 2. Silicon QPIC with CNOT gates and the experimental setup. (a) Schematic of the silicon quantum CNOT gate chip. (b) Microscope picture for the fabricated silicon QPIC. (c) SEM image of the fabricated CNOT gate $4.8 \times 4.45\ \mu m^2$. Microscope pictures of the (d) MZI and (e) the phase shifter. (f) Experimental setup.

conversion, which was generated by pumping a 3-cm-long PPKTP crystal with a continuous 775 nm laser of 80 mW. Degenerate 1550 nm orthogonally polarized daughter photon pairs were generated and divided by one polarization beam splitter. The second-order correlation function of this source was tested with a result of $g^2(0) = 0.0228 \pm 0.001$ without background correction, indicating that an excellent single-photon source was realized. The photon pairs were then coupled into two single-mode fibers through aspheric lenses. Pump light was blocked by a dichroic mirror (DM). The half wave plates (HWPs) and quarter wave plates (QWPs) before the lenses were controlled carefully, so that the polarization states of the two photons were both aligned to the horizontal axis and then coupled to the transverse electric (TE) mode of the optical waveguides by using TE-type grating couplers and a single-mode fiber array. The coupling efficiency of the used TE-type grating couplers is about 30%. After going through the silicon QPIC, the photons were detected by superconducting-nanowire single-photon detectors. The electrical signals from the detectors were collected and analyzed through a time-correlated single-photon counting system. The coincidence window was set as 0.8 ns for the two-photon state characterization. The phase shifters on the chip are controlled by one homemade multichannel direct-current power supply. More details about the characterization of the phase shifters can be found in the Supplemental Material [29].

As a preliminary characterization of a CNOT gate [35], the truth table was measured experimentally (see Fig. S5). In this situation, the four logical basis states ($|0\rangle_C|0\rangle_T$, $|0\rangle_C|1\rangle_T$, $|1\rangle_C|0\rangle_T$, $|1\rangle_C|1\rangle_T$) were injected. The probability for each of them at the output was measured, and the average transformation fidelity was $F = 0.944$. The discrepancy between the measured and expected fidelities is mainly attributed to the partial distinguishability of on-chip MZIs and the imperfect power splitting ratio (see Supplemental Material [29]).

The basic function of a CNOT gate is entangling two separate qubits or unentangling the entangled ones. Here we show the entanglement preparation with our silicon QPIC, which is the fundamental operation in quantum information processing and represents the most nonclassical implication of the quantum mechanics [36,37]. Here four maximally entangled Bell states were prepared with the CNOT gate and analyzed accordingly. By using the part of the state preparation, one can generate any of the states $|\pm\rangle_C|0\rangle_T$ and $|\pm\rangle_C|1\rangle_T$ to be input to the CNOT gate, where one has $|\pm\rangle \equiv (|0\rangle \pm |1\rangle)/\sqrt{2}$. Correspondingly, the four Bell states were all produced in the form of $|\Phi^{\pm}\rangle = 1/\sqrt{2}(|0\rangle_C|0\rangle_T \pm |1\rangle_C|1\rangle_T)$, and $|\Psi^{\pm}\rangle = 1/\sqrt{2}(|0\rangle_C|1\rangle_T \pm |1\rangle_C|0\rangle_T)$. Then we used the arbitrary single-qubit measurement capability of the state-analysis QPIC to perform the quantum-state tomography on these four states [36–39]. The phase shifters were used to implement all the 16 measurements needed to reconstruct the density operator of the state. Figure 3 shows the measured density of the Bell states with fidelities of 0.88 ± 0.02, 0.91 ± 0.02, 0.93 ± 0.03, and 0.92 ± 0.02, respectively, which were obtained from $F = (\mathrm{Tr}\sqrt{\sqrt{\rho_{\mathrm{th}}}\rho_{\mathrm{exp}}\sqrt{\rho_{\mathrm{th}}}})$. Here, ρ_{exp} is the density matrix reconstructed from the raw experimental data, and ρ_{th} represents the density matrix of the ideal state. To further characterize the quality of the entangled state, we measured the S parameter of the Clauser-Horne-Shimony-Holt (CHSH) inequality, which is a well-known validation technique for the presence of entanglement [35]. For any local hidden variable model, the CHSH inequality value S should satisfy the condition of $-2 \le S \le 2$. We set the phases

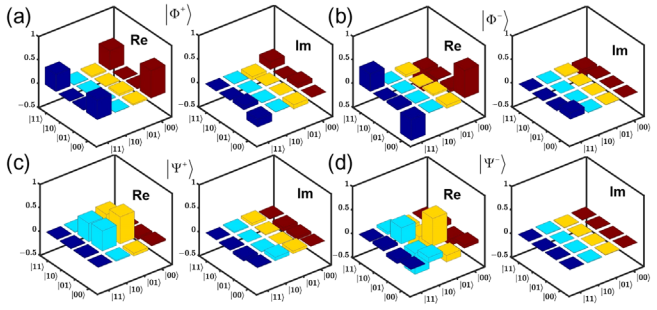

FIG. 3. Quantum states tomography. (a)–(d) The density matrices for the four Bell states; the fidelities are 0.88 ± 0.02, 0.91 ± 0.02, 0.93 ± 0.03 and 0.92 ± 0.02, respectively.

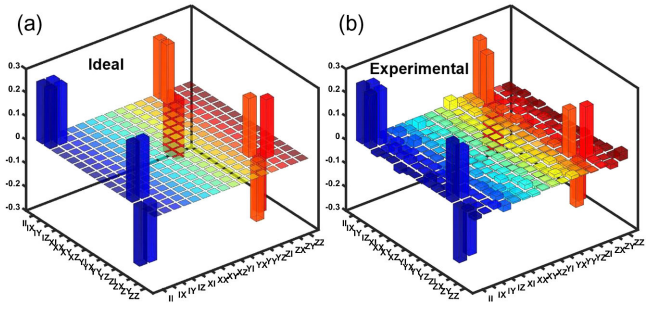

FIG. 4. Real part of the results for the 16×16 matrix χ_{exp} for the CNOT gate. (a) The ideal result. (b) The experimental result reconstructed from the test raw data. The process fidelity is 0.925 ± 0.008.

in two MZIs in the part of state analysis as $\theta_1 = \pi/8, 3\pi/8, 5\pi/8, 7\pi/8$ and $\theta_2 = 0, \pi/4, \pi/2, 3\pi/4$, respectively. According to these 16 two-qubit measurements on each state emerging from the CNOT gate, i.e., the Bell states $|\Phi^{\pm}\rangle$ and $|\Psi^{\pm}\rangle$, the S parameter is estimated as 2.47 ± 0.05, 2.60 ± 0.05, 2.65 ± 0.05, and 2.43 ± 0.06, respectively, which evidently violates the inequality. Here the errors were calculated by using a Monte Carlo method with Poissonian statistics [35].

To fully characterize the CNOT gate, the quantum process tomography [38] was also carried out. As required, one should prepare the input state of photons in a complete set of basis states and perform the quantum-state tomography on each output state [34]. For a generic quantum process ε acting on a 2-qubit density matrix ρ, one has $\varepsilon(\rho) = \sum_{m,n=0}^{15} \chi_{mn} \Gamma_m \rho \Gamma_n^{\dagger}$, where the operator Γ_m is defined as the tensor products of Pauli matrices $\{\Gamma_m \equiv \sigma_i \otimes \sigma_j\}, i, j = 0, \ldots, 3, m = 0, \ldots, 15$, and thus the matrix χ_{mn} contains all the information of the process. Figures 4(a) and 4(b) show the real part of the ideal state and the experimental result reconstructed from the test raw data for the 16×16 matrix χ_{exp}, respectively. The process fidelity of the CNOT gate is 0.925 ± 0.008, which is much higher than the result ($\sim$0.638) for the 14×14 $\mu\mathrm{m}^2$ plasmonic CNOT gate reported recently [10].

In summary, we have demonstrated a supercompact path-encoded quantum CNOT gate on silicon, which has been fully characterized by applying the quantum-state and process tomography technique. The present supercompact CNOT gate was realized by introducing a six-channel superlattice waveguide, and the footprint is as small as 4.8×4.45 $\mu\mathrm{m}^2$ ($\sim 3\lambda \times 3\lambda$). For the present supercompact CNOT gate, which is the smallest one reported until now, the footprint is shrunk very significantly by $\sim$10 000 times compared to those previous on-chip quantum CNOT gates based on dielectric waveguides. Meanwhile, the fidelity is still as high as 0.925 ± 0.008. This supercompact CNOT gate shows great potential for developing high-density silicon quantum PICs. Furthermore, the design with the waveguide superlattice can also be extended to other complex QPICs. This work provides a novel basic element for quantum information processing and paves the way to realize large-scale QPICs.

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*These authors contributed equally to this work.
†renxf@ustc.edu.cn
‡dxdai@zju.edu.cn

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