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Nanowire Transistors with Bound-Charge Engineering

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Low-dimensional electronic systems such as silicon nanowires exhibit weak screening which is detrimental to the performance and scalability of nanodevices, e.g., tunnel field-effect transistors. By atomistic quantum transport simulations, we show how bound charges can be engineered at interfaces of Si and low-κ oxides to strengthen screening. To avoid compromising gate control, low-κ and high-κ oxides are used in conjunction. In Si nanowire tunnel field-effect transistors, we demonstrate that bound charge engineering increases the on-state current by orders of magnitude, and the combination of oxides yields minimal subthreshold swing. We conclude that the proposed bound-charge engineering paves a way toward improved low-power transistors.

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Introduction.—Power dissipations in transistors are a major cause [1] for much of the recent downfall in the scaling laws suggested by Moore [2] and Dennard [3]. Since these power dissipations scale with the inverse of a transistor's gate capacitance [4], two of the most significant developments in the semiconductor industry over the last two decades have been (1) the substitution of silicon dioxide by high-κ (i.e., high permittivity) dielectrics [5], such as hafnium-based oxides [6,7], as the gate dielectric, and (2) the multiplication of the number of gates [8], starting from single-gate, to double-gate [9], to fin [10], and finally to gate-all-around (GAA) [11] field-effect transistors (FETs). Semiconductor nanowires (NWs)—especially silicon NWs—are ideal complementary-metal-oxide-semiconductor-compatible materials for GAA transistors [12,13]. When combined with high-κ gate dielectrics, GAA Si NW metal-oxide-semiconductor field-effect transistors (MOSFETs) display excellent gate control and performance [14,15]. A relevant figure of merit directly related to power dissipation is the subthreshold swing (SS)

$$S = \left(\frac{\partial \log_{10} I_{DS}}{\partial V_{GS}}\right)^{-1}, \tag{1}$$

namely the increment in gate-to-source voltage V_{GS} required for a decade increase in drain current I_{DS}. For MOSFETs, thermodynamics dictate that $S \geq 60$ mV dec^{-1} at room temperature. This fundamental limit—known as Boltzmann tyranny—sets a practical limit on the power supply voltage V_{DD} at which CPUs can be run and on power dissipations in the switching process $P \propto V_{DD}^2$ [1]. A critical task is thus to develop devices employing physics beyond that of the MOSFET. To this end, the tunnel FET (TFET), which operates on band-to-band quantum tunneling, can reach sub-60 mV dec^{-1} SS, leading to significantly lower power dissipations [16,17].

The most basic TFET has a p-type-intrinsic-n-type chemical doping profile. Tunneling occurs at the p-type-intrinsic junction and is severely limited by the width of the tunneling barrier, which is commensurate to the sharpness of the electrostatic potential profile at the junction. Problematically, in low-dimensional electronic materials such as Si NWs [18,19], few-layers black phosphorus [20–23], few-layers transition metal dichalcogenides [24], graphene nanoribbons [25], and carbon nanotubes [26], electrostatic charge screening is rather poor, which leads to diffuse potential profiles across junctions. This presents a major problem to the performance and scalability of any nanodevice requiring sharp potential interfaces, e.g., TFETs, small-diameter short-channel GAA FETs, and possibly novel memory devices containing many interfaces. Experimentally, sharp potential interfaces may be realized by heavy doping, which shortens the screening length. However, one is already at a limit of how much one can dope semiconductors in nanoscale FETs without affecting material integrity and electronic properties. Theoretically, in simulations, one often uses doping levels higher than what is feasible experimentally in order to generate sharp potential profiles across junctions.

In this work, we propose and theoretically investigate the idea of bound-charge engineering (BCE) to solve the electrostatic charge screening problem. In BCE, a high-κ oxide inside the gated region is combined with a low-κ oxide outside to achieve strong screening. We show that BCE significantly improves charge screening in low-dimensional nanodevices without compromise to gate control. Furthermore, using a quantum transport formalism, we show that applying BCE to Si NW TFETs can greatly increase the overall device performance—the on-state

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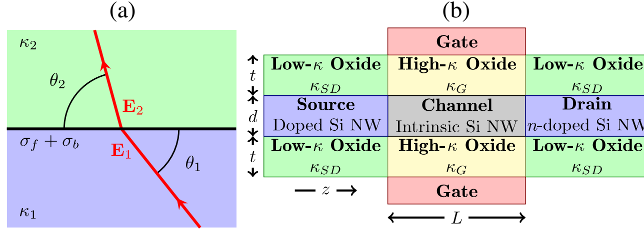

FIG. 1. (a) Illustration of BCE. When an electric field $\mathbf{E}_1$ (red arrow) is incident to the interface (black line) between two distinct linear dielectric media (green and blue regions) with relative permittivities $\kappa_{1,2}$, a bound charge σ_b forms on the interface. (b) Schematic of the GAA Si NW transistors investigated in this work. Cross sections through the NWs' axis of rotational symmetry are shown. MOSFETs have an n-doped source and TFETs have a p-doped source; the surrounding oxide thickness is set to $t = 2$ nm and the channel length is set to $L = 9.98$ nm. The gate metal's work function is taken to be 0.5 eV greater than the Si NW's electron affinity.

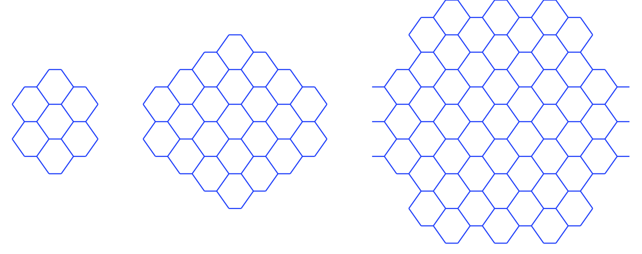

FIG. 2. Atomic structures (in the wire-frame model) of the unit cells of the three Si NWs investigated in this work, all of which are grown in [110]. Their diameters are (from left to right) $d = 1.16$ nm, $d = 2.07$ nm, and $d = 2.95$ nm. Their numbers of atoms per unit cell are (from left to right) 24, 64, and 136. The interatomic distance is 2.35 Å. In this figure, the z axis [defined in Fig. 1(b)] is normal to the page.

current in particular—thanks to the sharp band-to-band tunneling junctions that BCE provides.

Bound-charge engineering.—To explain BCE, consider the interface between a semiconductor with relative permittivity κ_1 and an oxide with relative permittivity κ_2 as shown in Fig. 1(a). By Gauss's law,

$$(\kappa_2 \mathbf{E}_2 - \kappa_1 \mathbf{E}_1) \cdot \hat{n} = \frac{\sigma_f}{\epsilon_0}$$
$$\Rightarrow \kappa_1 E_1 \sin\theta_1 + \frac{\sigma_f}{\epsilon_0} = \kappa_2 E_2 \sin\theta_2, \quad (2)$$

where $\hat{n}$ is the normal unit vector from the semiconductor to the oxide, σ_f is the surface free charge on the interface between the two media, ϵ_0 is the permittivity of free space, $\mathbf{E}_{1,2}$ are the electric fields in the two media, and $\theta_{1,2}$ are the angles they make with the interface. From electrostatics [27], the polarization density in medium i near the interface is $\mathbf{P}_i = (\kappa_i - 1)\epsilon_0 \mathbf{E}_i$, and the surface bound charge at the interface is $\sigma_b = \mathbf{P}_1 \cdot \hat{n} - \mathbf{P}_2 \cdot \hat{n}$. It follows from Eq. (2) that the total surface charge on the interface is

$$\sigma_f + \sigma_b = \epsilon_0 E_1 \frac{\kappa_1 - \kappa_2}{\kappa_2} \sin\theta_1 + \frac{\sigma_f}{\kappa_2}. \quad (3)$$

Equation (3) suggests that, under an external electric field, the surface bound charge σ_b—hence the total surface charge $\sigma_f + \sigma_b$—on a semiconductor can be modulated by the permittivities $\kappa_{1,2}$. In an n-type FET biased such that the gate potential is lower than the source and drain potentials (i.e., in the off state), since some electric field lines must flow from the source and drain to the gate, positive charges accumulate over a depletion length ℓ in the source and drain near the interfaces with the channel to screen the negative channel charge. If the oxide surrounding the source and drain has a relative permittivity κ_{SD} smaller than that of the semiconductor source and drain (for Si, the relative permittivity is $\kappa_{\mathrm{Si}} = 11.7$), then, by Eq. (3), the surface charge on the oxide-semiconductor interface is positive and maximized in the limit of small κ_{SD}, and thereby enhances the screening of the channel charge (i.e., ℓ is lower). This effect is expected to be stronger in FETs with larger surface-area-to-volume ratio, such as in thin Si NW FETs. Similar arguments can be applied for p-type FETs. High-κ oxides are needed and used in modern FETs for gate control. The above analysis thus suggests to combine two oxides: a high-κ one around the channel of the FET and a low-κ one around the source and drain for strong screening of the channel charge. This BCE realizes a FET structure whose cross section is shown in Fig. 1(b), which has much sharper potential profiles at the source-channel and channel-drain interfaces.

Atomistic simulations of BCE.—Having established the general physics of BCE, we concretely test its potential benefit to charge screening, using as an example the Si NWs shown Fig. 2, within the atomistic quantum transport package Nanoskim 2.0 [28]. This simulation method combines the Slater-Koster tight-binding (TB) method [29] and the nonequilibrium Green's functions (NEGF) formalism [30–33] self-consistently, and is described in more detail in Sec. S.I of the Supplemental Material [34]. We note that oxides are treated in a continuum approximation, being described solely by their permittivities. We justify this approximation by the very large band gaps of oxides and their resulting inertness in charge transport. Furthermore, experimental reports show that given proper device fabrication, the permittivities of nanometric thin-film oxides are close to the bulk permittivities [37,38], indicating that such thin-film oxides can be treated in a continuum approximation.

Figure 3(a) shows the calculated electrostatic potential profiles at equilibrium of n-channel GAA Si NW MOSFETs with HfO_2 gate oxide ($\kappa_G = 30$) and various source and drain oxides; the calculated electric fields are shown in Fig. S.3 of the Supplemental Material [34].

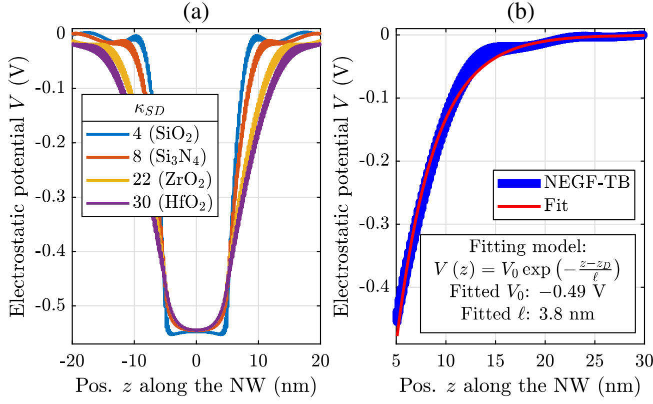

FIG. 3. (a) Electrostatic potential V as a function of the position z along the NW from the channel center in $d = 1$-nm-wide GAA Si NW n-channel MOSFETs with structures shown in Fig. 1(b), as obtained from NEGF-TB simulations. The source and drain doping concentration N_D is set to 2×10^{20} cm^{-3} and the gate oxide is HfO_2 ($\kappa_G = 30$). Several source and drain oxides (with different relative permittivities κ_{SD}) are compared. The drain and gate voltages are, respectively, set to $V_{DS} = 0$ V and $V_{GS} = 0.5$ V. (b) Illustration of the extraction of the depletion length ℓ in the case of $\kappa_{SD} = 22$. The term $z_D = 4.99$ nm refers to the position of the channel-drain interface.

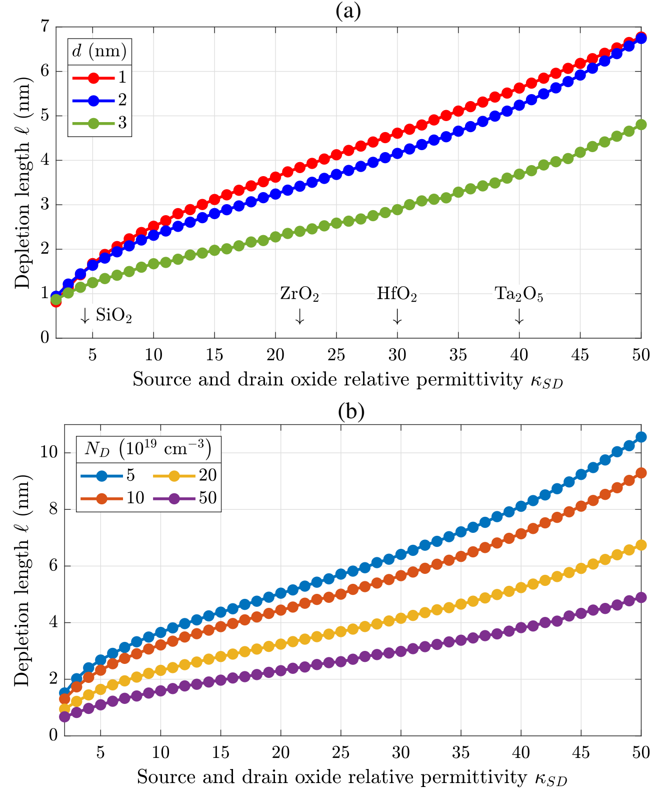

FIG. 4. Depletion length ℓ as a function of source and drain oxide permittivity κ_{SD} in GAA Si NW n-channel MOSFETs with structures shown in Fig. 1(b), as obtained from the method of Fig. 3(b). The gate oxide is HfO_2 ($\kappa_G = 30$). The applied voltages are set to $V_{DS} = 0$ V and $V_{GS} = 0.5$ V. In (a), the source and drain doping concentration N_D is set to 2×10^{20} cm^{-3}, and several NW diameters d are investigated. In (b), d is set to 2 nm, and several N_D are investigated.

Specifically, the structure of these devices is shown in Fig. 1(b); in particular, the channel length is $L = 10$ nm and the surrounding oxide thickness is $t = 2$ nm. A clear trend is seen: NWs with BCE, namely those with lower κ_{SD}, exhibit sharper potential junctions at the interfaces between the channel and the source or drain. The sharpness of the potential profile is described by a lengthscale ℓ over which the potential decays to 0; it can be quantified using an exponential fit, as illustrated in Fig. 3(b). The potential decay lengthscale ℓ can be interpreted to be the depletion length of the source-channel or channel-drain interface. In Fig. 4, the extracted ℓ as a function of κ_{SD} are shown. The depletion length is seen to increase monotonically with the permittivity of the source and drain oxide, as expected from Eq. (3). Furthermore, $\ell \to 0$ as $\kappa_{SD} \to 0$; this is a consequence of the $1/\kappa_2$ singularity in Eq. (3).

In Fig. 4(a), the ℓ-κ_{SD} relationship is calculated for NW diameters d ranging from 1 nm to 3 nm (Fig. 2). Broadly speaking, thicker NWs display stronger screening as expected from their larger density of free charge. Furthermore, BCE provides greater improvement to screening in thinner NWs—for which the relative contribution of surface bound charges is higher—as expected from their larger surface-area-to-volume ratio. Indeed, consider a "BCE device" with SiO_2 as the source and drain oxide ($\kappa_{SD} \approx 4$) and a "standard device" with HfO_2 as the source and drain oxide ($\kappa_{SD} = 30$). Comparing these devices in the case of $d = 3$ nm, BCE reduces the depletion length by a factor of $\ell(\kappa_{SD}=30)/\ell(\kappa_{SD}=4)=2.53$ (Fig. 4). On the other hand, for $d = 2$ nm ($d = 1$ nm), this ratio is 2.87 (3.19).

In Fig. 4(b), BCE is benchmarked for various source and drain doping concentrations N_D. Expectedly, devices with higher N_D have smaller depletion lengths. However, by similar arguments as before, BCE is found to be more effective at lower doping concentrations. Correspondingly, for thinner NWs with lower doping, the ratio of total bound charge to total free charge is higher (Fig. S.4 of the Supplemental Material [34]). BCE thereby provides an alternative to achieve stronger charge screening in applications where higher chemical doping is infeasible. Overall, the NEGF-TB simulation results quantitatively substantiate the BCE picture. Furthermore, BCE is found to be more effective in thinner NWs with lower doping concentrations. Therefore, BCE would be especially useful to future generations of industry Si NW transistors, for which d is expected to shrink to a few nanometers.

BCE in TFETs.—Having understood the effect of BCE on electrostatic screening, we investigate its benefits to devices using Si NW TFETs as examples. Charge transport in TFETs involves band-to-band quantum tunneling from the source to the channel; the tunneling probability decays

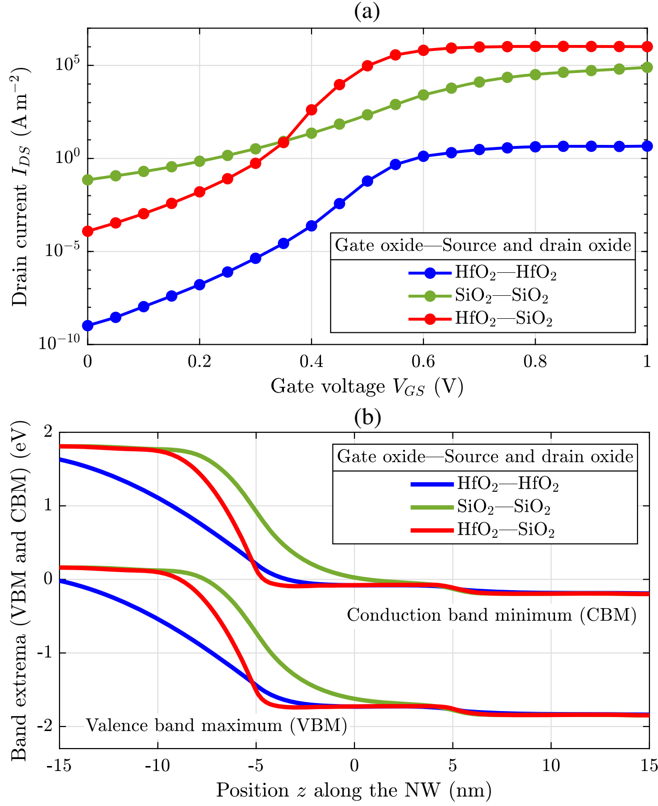

FIG. 5. (a) Transfer characteristics of $d = 2$-nm-wide GAA Si NW n-channel TFETs with structures shown in Fig. 1(b) as obtained for NEGF-TB simulations at a temperature of $T = 300$ K. The drain voltage is set to $V_{DS} = 50$ mV. The current is normalized by the NW cross-sectional area. (b) Band diagrams of the TFETs for gate voltage $V_{GS} = 0.6$ V and drain voltage $V_{DS} = 50$ mV as obtained from NEGF-TB simulations.

exponentially with the tunneling length [39]. TFETs with sharper junctions thus exhibit higher on-state current which enables their practical applications at higher frequency.

Three different $d = 2$-nm-wide GAA Si NW n-channel TFETs [structure shown in Fig. 1(b)] are simulated by NEGF-TB (Fig. 5). In the first TFET, the Si NW is entirely surrounded by the high-κ oxide HfO_2 ($\kappa_G = \kappa_{SD} = 30$). In the second TFET, the Si NW is entirely surrounded by the low-κ oxide SiO_2 ($\kappa_G = \kappa_{SD} = 3.8$). The third is a BCE TFET: the Si NW is surrounded by HfO_2 and SiO_2 as in Fig. 1(b) ($\kappa_G = 30$ and $\kappa_{SD} = 3.8$). In the NEGF-TB simulations, the devices are naturally partitioned into three regions: source, channel, and drain. The source and drain extend to $\pm\infty$; their contributions are included in the self-energy (see Eq. S.4 in the Supplemental Material [34]). The channel of the devices is 9.98 nm long and includes 1664 Si atoms. The entire simulation box (source and drain buffers and channel) is 117 nm long and includes up to 19456 Si atoms.

The calculated transfer characteristics of these devices are shown in Fig. 5(a) for $V_{DS} = 50$ mV. Several observations are in order. First, overall, the best performing device is the BCE TFET (red curves). Its low-κ source and

TABLE I. On-state current I_{on} and average subthreshold swing S_{av} of the three TFETs investigated in this work. The on state (off state) is defined to be reached when the gate voltage is $V_{GS} = 0.6$ V ($V_{GS} = 0.2$ V) and the drain voltage is $V_{DS} = 50$ mV. The average of the subthreshold swing is taken between the off state and the on state.

Gate oxide	Source and drain oxide	I_{on} (A m^{-2})	S_{av} (mV dec^{-1})
HfO_2	HfO_2	1.3×10^0	58.0
SiO_2	SiO_2	2.6×10^3	112
HfO_2	SiO_2	6.5×10^5	52.6

drain oxide significantly sharpens the potential profile at the source-channel and channel-drain interfaces [see Fig. 5(b)], which reduces tunneling length, thus increasing the on-state current by orders of magnitude compared to the HfO_2-only TFET (blue curves). Second, the SiO_2-only TFET (green curves) has an on-state current orders of magnitude higher than that of the HfO_2-only TFET (blue curves), although it is smaller than that of the BCE TFET, which has greater gate control due to HfO_2 surrounding the channel. Third, the calculated band diagram in Fig. 5(b) shows that the tunneling length in the BCE TFET is ~4.3 nm (red curves), to be compared to ~11.9 nm for the HfO_2-only TFET (blue curves). This is the physical reason for the much higher on-state current in the BCE TFET. Fourth, devices employing HfO_2 as the gate oxide (red and green curves) have much lower SS than that which employs SiO_2 (blue curves). The much-improved SS is due to a stronger gate control and a lower body factor that a high-κ gate oxide confers [4]. The values of SS and on-state current for the three devices are reported in Table I.

Conclusion.—In this work, we introduce a novel and simple bound-charge engineering where oxides of different permittivities are combined to greatly sharpen potential profiles in NW transistors at interfaces along the transport direction with no compromise to gate control. As an example, when BCE is applied to Si NW TFETs, it very effectively reduces tunneling length while maintaining high gate control, leading to much-improved device characteristics regarding the on-state current, the subthreshold swing, and the on-to-off current ratio. Since both the high-κ HfO_2 and low-κ SiO_2 are well-known, industry-standard oxides (and there are many other material choices, as shown in Fig. 4), BCE-assisted FETs should be realizable experimentally. Recent reports of ultralow-κ dielectrics, e.g., amorphous boron nitride with $\kappa \approx 1.5$ [40], offer especially promising prospects. BCE may thereby offer significant performance gains with relatively few changes to processes and assembly. The principle of BCE is general; it could also be applied to other low-dimensional materials, notably 2D semiconductors as well as semiconducting NWs and nanotubes. BCE could also be applied to scale down low-dimensional nanodevices, especially systems with a large

number of junctions such as NAND memory and the cold source FET [41]. Finally, given the very general physics underlying BCE, it could find applications in areas of research beyond nanoelectronics in which strong charge screening might be desired, e.g., molecular electronics, electrochemistry, and material sciences.

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[34] See Supplemental Material at http://link.aps.org/supplemental/10.1103/PhysRevLett.125.247704 for a description of the NEGF-TB simulation method, sensitivity tests, visualizations of the electric field in investigated devices, and investigation of the bound-to-free charge ratio, which includes Refs. [35,36].

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