

Limits to Metallic Conduction in Atomic-Scale Quasi-One-Dimensional Silicon Wires

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(Received 5 May 2014; revised manuscript received 18 September 2014; published 10 December 2014)

The recent observation of ultralow resistivity in highly doped, atomic-scale silicon wires has sparked interest in what limits conduction in these quasi-1D systems. Here we present electron transport measurements of gated Si:P wires of widths 4.6 and 1.5 nm. At 4.6 nm we find an electron mobility, $\mu_{\text{el}} \approx 60 \text{ cm}^2/\text{Vs}$, in excellent agreement with that of macroscopic Hall bars. Metallic conduction persists to millikelvin temperatures where we observe Gaussian conductance fluctuations of order $\delta G \sim e^2/h$. In thinner wires (1.5 nm), metallic conduction breaks down at $G \lesssim e^2/h$, where localization of carriers leads to Coulomb blockade. Metallic behavior is explained by the large carrier densities in Si:P δ -doped systems, allowing the occupation of all six valleys of the silicon conduction band, enhancing the number of 1D channels and hence the localization length.

DOI: 10.1103/PhysRevLett.113.246802

PACS numbers: 73.63.Nm, 71.23.An, 73.23.Hk, 85.35.-p

Individual dopants in semiconductors are emerging as active components in device applications due to their electrical [1–3], spintronic [4,5], or optoelectronic [6] properties. Combined with the ability to encode quantum information [5] within their spin or charge degrees of freedom, individual dopants can be regarded as the fundamental limit in semiconductor device scaling. However, the construction of complex devices [7–9] and scalable architectures [10,11] requires low-resistive electrodes and interconnects of comparable scale as the dopants themselves.

Recently, we reported the fabrication of atomic-scale wires in silicon, using STM hydrogen lithography, phosphorus δ doping, and low-temperature molecular beam epitaxy [1]. In contrast to other silicon nanowires [12] these highly doped systems were found to maintain a diameter-independent bulklike resistivity as low as $\rho_{3D} = (0.3 \pm 0.2) \text{ m}\Omega \text{ cm}$ at $T = 4.2 \text{ K}$. These results implied Ohmic scaling down to diameters comparable to the donor Bohr radius ($a_B \sim 2.5 \text{ nm}$), raising the question whether these wires could be regarded as metallic.

Indeed, atomistic tight-binding (TB) calculations confirm a metallic band structure with Fermi energies as much as $E_F \approx 135 \text{ meV}$ above the local conduction band edge [1,13]. These calculations, however, assume “ideal” wires with periodic repetitions of doped supercells and do not capture potential disorder in the wire arising from the disordered placement of donors. Understanding this disorder is crucial since it can lead to spatial localization of electronic wave functions [14] and ultimately imposes a limit on the observation of metallic conduction in low-dimensional nanostructures.

In strictly one-dimensional (1D) systems (those with a *single* quantum channel), disorder causes localization over

a length scale as short as the carrier mean free path, l [15]. With $l \approx 5\text{--}10 \text{ nm}$ Si:P δ -doped systems [16], no appreciable length scale would exist over which metallic conduction and Ohm’s law could be maintained [17]. However, the localization length, $\xi \sim Nl$, in *quasi*-1D systems (those with *multiple* quantum channels N), increases due to an enhanced number of final states for scattering [18,19]. Correspondingly, it has been shown that a *single* parameter—the conductance G —determines whether a conductor of length L is regarded as *metallic* or *insulating* with a universal crossover at a conductance $G_0 \sim e^2/h$, where $\xi \sim L$ [18,20].

Here, we investigate this metal-insulator transition in highly doped Si:P wires. Using STM as an atomic-precision fabrication tool to scale the wire width, we access both metallic and insulating regimes and study electron conduction down to millikelvin temperatures and in the presence of gate-induced electric fields. Unique to Si:P wires, extremely high carrier sheet densities ($\approx 2 \times 10^{14} \text{ cm}^{-2}$) allow the occupation of all six equivalent valleys of the silicon conduction band, leading to a sixfold enhancement of 1D channels at the quantum limit. Consequently, this allows metallic conduction over tens of nanometers in Si:P wires, despite their atomic-scale diameters.

STM images of two wire templates (W1) and (W2) [21] are shown in Fig. 1 [1,3,22] with high-resolution closeups in Figs. 1(c) and 1(d) recorded after hydrogen lithography on Si(001) – (2 × 1) substrates (*n*-type, 1–10 m Ω cm). Both wires are aligned along $\langle 110 \rangle$, parallel to the dimer rows of the surface reconstruction. Compared to earlier work on STM-patterned wires [23,24], improved tip biasing conditions ($\sim 2.5 \text{ V}$, $\sim 25 \text{ nA}$) were used for complete removal of the hydrogen resist and clean definition of the

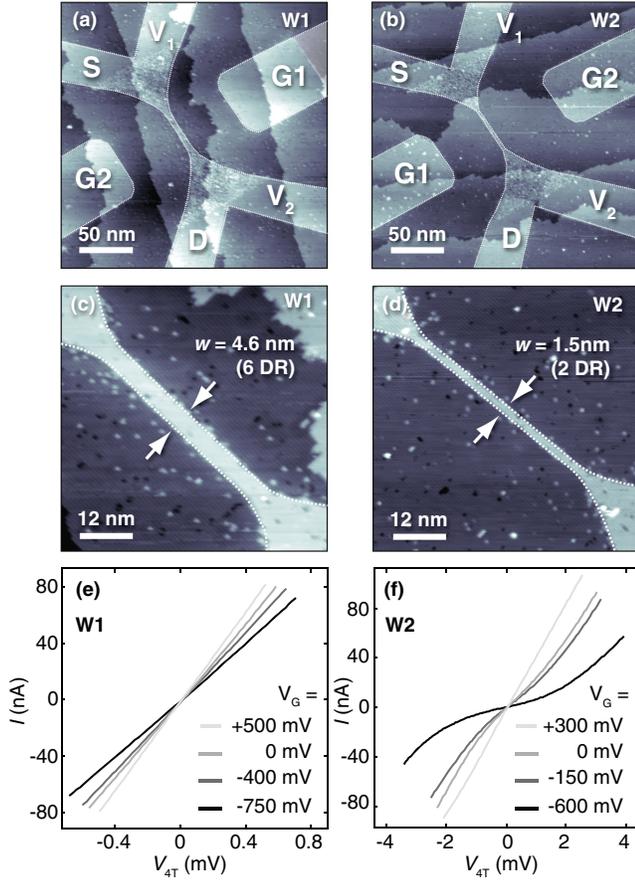


FIG. 1 (color online). (a) and (b) Overview STM images (-2.0 V, 100 pA) of two atomic-scale wires ($W1$) and ($W2$) with two contacts (S , V_1) and (D , V_2) on either end, allowing four-terminal ($4T$) resistance measurements. In-plane gates, G_1 and G_2 , allow us to tune the electron density. (c),(d) Atomic resolution images show the alignment along $\langle 110 \rangle$. The lithographic widths, $w = 4.6$ ($W1$) and $w = 1.5$ nm ($W2$), correspond to six and two dimer rows (DR) of the $\text{Si}(001) - (2 \times 1)$ surface reconstruction. (e),(f) $4T$ IV characteristics at $T = 4.2$ K and for varying gate bias, V_G .

wire edges. We extract the lithographic widths, $w = 4.6$ and $w = 1.5$ nm, corresponding to approximately six and two atomic dimer rows (DR) of the surface reconstruction. The wires span lengths, $L = 47$ and $L = 49$ nm, between the contacts, making them nominally identical except for their width.

Immediately after STM lithography of the wires, each template is exposed to phosphine (PH_3) gas (5×10^{-8} mbar, 6 min), passivating the reactive silicon dangling bonds, thereby effectively protecting the wire against contaminants during patterning of electrodes (S , D , $V_{1,2}$), gates ($G1, 2$), and micrometer-scale contact arms [1]. The PH_3 -dosed parts of the central part of the pattern can be observed in Figs. 1(a) and 1(b). A second exposure to PH_3 , followed by annealing (350°C , 1 min) and low-temperature silicon homoepitaxy (≈ 25 nm), selectively dopes the completed

pattern to $1/4$ ML density ($N_{2D} \approx 2 \times 10^{14} \text{ cm}^{-2}$) [16,25]. Optimized conditions during dopant incorporation and crystal growth [25], compared to earlier studies [23,24], minimize segregation and diffusion of donors and allows for atomically sharp doping profiles with equivalent bulk density $\sqrt{N_{2D}^3} \sim 10^{21} \text{ cm}^{-3}$ —three orders of magnitude higher than the density ($\approx 3 \times 10^{18} \text{ cm}^{-3}$) at the Mott transition [15].

Four-terminal IV characteristics at $T = 4.2$ K are shown in Figs. 1(e) and 1(f). In the 4.6 nm wide wire ($W1$), linear IV s and a weak dependence on gate voltage indicate metallic conduction with the large carrier density effectively screening the gate-induced electric fields. In contrast, the 1.5 nm wide wire ($W2$) shows a strong dependence on gate voltage, allowing us to tune the device from Ohmic (linear) to non-Ohmic, and indicates incomplete screening of the disorder potential and carrier localization. Integrity of the doping pattern in both wires is confirmed by the existence of a low-Ohmic transport channel along $S - D$ while several hundred millivolt can be applied to the gates.

In Figs. 2(a) and 2(b), we plot conductance G_W corrected for series resistances R_δ arising within the contact triangles at either end of the wires [26]. The lower panel in each figure shows conductance at $V_{4T} = 0$ V, with respect to $G_0 \sim e^2/h$ (black dashed lines).

In the 4.6 nm wide wire ($W1$) the absence of conductance features resembles the characteristics of an Ohmic resistor with $G_W > e^2/h$ at all gate voltages. Metallic conduction is confirmed by the approximately linear slope allowing us to extract electron mobility, μ_{el} . In quasi-1D systems the conductance can be expressed using Boltzmann theory [27,28],

$$G = g_s g_v \frac{e^2 k_F l}{h} \left(\frac{w}{L} \right) = \frac{2e^2}{h} N_{\text{eff}} \frac{\pi l}{2L}, \quad (1)$$

where $g_s = 2$ and $g_v = 6$ are the spin and valley multiplicity, respectively, and $k_F = \sqrt{4\pi n_s / g_s g_v}$ is the Fermi wave vector. The last identity connects to a Landauer-type expression of the conductance [27] where $\pi l / 2L$ can be regarded as an average transmission coefficient per 1D mode and $N_{\text{eff}} = g_v (k_F w / \pi)$ denotes the total number of modes [29].

From a linear fit [dashed blue line in Fig. 2(a)],

$$G = 4.8 \frac{e^2}{h} \left(1 + \frac{V_G}{3V} \right), \quad (2)$$

we extract,

$$\mu_e = \left(\frac{L^2}{C_G} \right) \left(\frac{dG}{dV_G} \right) \approx 60 \text{ cm}^2/\text{V s}, \quad (3)$$

in excellent agreement with previous estimates in 2D δ -doped Hall bars (35 – $120 \text{ cm}^2/\text{V s}$) [16,25]. In the above estimate L is the sample length and $C_G = e(dN_{el}/dV_G) \approx 23$ aF is the combined gate capacitance. The latter has been

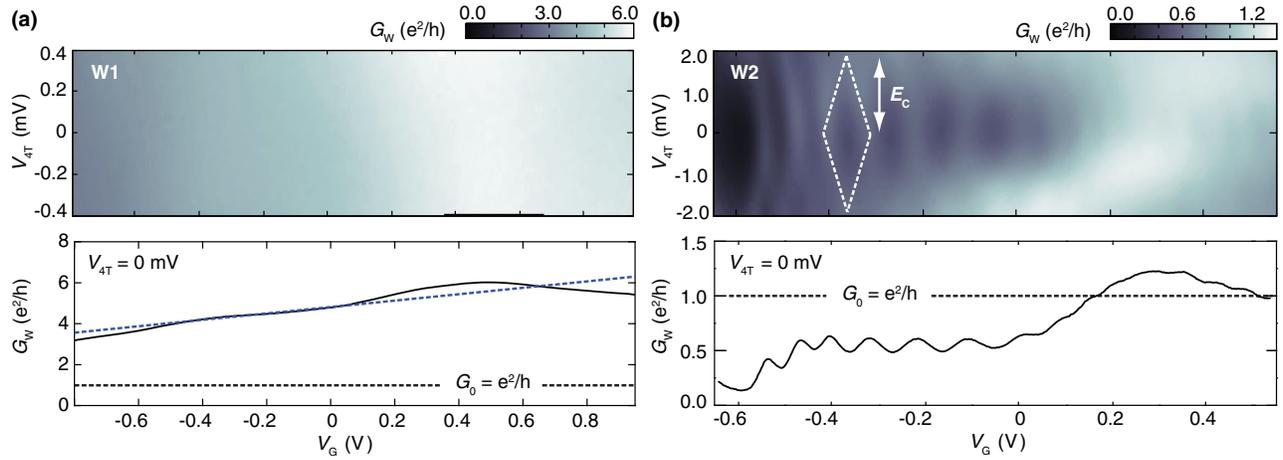


FIG. 2 (color online). $4T$ differential conductance G_W of two atomic-scale wires W1 (a) and W2 (b). Upper panel: G_W as a function of gate voltage V_G , and $4T$ voltage drop, V_{4T} . Lower panel: Conductance, $G_W(V_{4T} = 0$ V) with respect to $G_0 \sim e^2/h$ (black dashed lines). The dashed blue line in (a) shows a linear fit to extract electron mobility. Coulomb blockade oscillations (b) are observed in the 1.5 nm wide wire (W2).

obtained, assuming that the wire is fully depleted at $V_G = -3$ V, allowing us to estimate the number of carriers in the wire, $N_{el} \approx 430(1 + (V_G/3 \text{ V}))$, based on the electron sheet density at $V_G = 0$ V ($\approx 2 \times 10^{14} \text{ cm}^{-2}$) and the lithographic area of the wire, $(w \times L) \approx 215 \text{ nm}^2$. From the mobility we extract the electron mean free path, $l = (\hbar k_F \mu_{el}/e) \approx 6$ nm. This now allows us to extract the Ioffe-Regel (disorder) parameter, $k_F l$. With $k_F l \gg 1$ for metallic systems and $k_F l \ll 1$ in insulators [17], we find $k_F l \approx 9$, in our Si:P wires.

In the 1.5 nm wide wire (W2) [Fig. 2(b)] we observe regions of reduced differential conductance around zero bias and at negative gate voltage. These result in regular oscillations in the linear conductance at $G_W < e^2/h$, and arise from Coulomb blockade of strongly localized carriers [20,30,31]. From the height of the Coulomb “diamonds” (white dashed lines), we extract an approximate charging energy, $E_C \approx 2$ meV. Towards positive gate bias, the Coulomb oscillations subside, coinciding with an increase in conductance just above $G_W \sim e^2/h$.

To understand metallic conduction and its limits in Si:P wires, it is important to realize that they are multimode quasi-1D systems such that the number of conducting channels N_{eff} and the carrier mean free path l determine the length over which electronic wave functions are localized, $\xi \sim N_{eff} l$ [19]. Unique to Si:P nanostructures are extremely high carrier sheet densities ($\approx 2 \times 10^{14} \text{ cm}^{-2}$), allowing the occupation of all six equivalent valleys of the silicon conduction band ($g_v = 6$) with effective masses close to those in bulk [13,32–35]. Importantly, this distinguishes Si:P wires from other silicon devices with dilute or semidilute doping ($\lesssim 10^{19} \text{ cm}^{-2}$) [36], in which tunneling occurs through discrete donor states or within Hubbard impurity bands [36].

The number of channels N_{eff} obtained by atomistic TB calculations [1,13] is plotted in Fig. 3(a) as a function

of width. Here, we observe an approximately linear drop in N_{eff} with decreasing width down to $w \approx 2$ nm, where N_{eff} saturates at the valley multiplicity, $g_v = 6$. A single 1D mode in each valley, $N_{eff} = 6$, consequently defines the 1D quantum limit for Si:P wires. The black dashed line in Fig. 3 corresponds to a simple analytical estimate, $N_{eff} = g_v(k_F w/\pi)$, previously employed in the expression

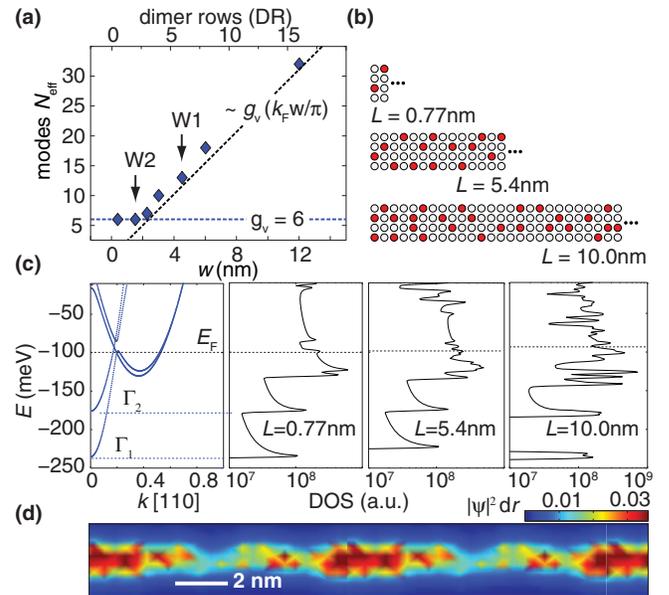


FIG. 3 (color online). Atomistic modeling of the electronic structure at $T = 4.2$ K. (a) Number of conducting modes N_{eff} (diamonds) as a function of wire width, compared to a simple analytical estimate (black dashed line, see text). (b)–(d) Modeling of electron localization due to dopant disorder. (b) Example supercell configurations used to calculate (c) band structure and density of states. (d) Charge density $|\psi|^2 dr$ [1] based on a repetition of the $L = 10$ nm cell in (b).

of the Boltzmann conductance [Eq. (1)]. With as many as $N_{\text{eff}} = 13$ (W1) and $N_{\text{eff}} = 6$ (W2) channels (black arrows) based on the TB calculations, we estimate $\xi_{W1} \sim 78$ nm and $\xi_{W2} \sim 36$ nm, using $l \sim 6$ nm. Consequently, at a length, $L \approx 50$ nm, both wires are close to the metal-insulator transition with W1 in the metallic ($\xi > L$) and W2 in the insulating regime ($\xi < L$).

The influence of dopant disorder on electronic structure is explored in Figs. 3(b)–3(d). Examples of supercell configurations with 0.25 ML, representing a 1.5 nm wide wire of varying length ($L = 0.77$, $L = 5.4$, and $L = 10$ nm), are shown in Fig. 3(b) [1,13]. Infinite repetitions of such cells in the transport direction are used to calculate the band structure and density of states (DOS), Fig. 3(c). The shortest cell ($L = 0.77$ nm) represents an ordered wire [1,13] and yields the quasi-1D metallic band structure and DOS of Si:P systems [13]. Including doping randomness requires an increase of the supercell length to $L = 5.4$ nm, leaving the DOS essentially unchanged. Initial indications of carrier localization is observed at $L = 10$ nm, where we find a prominent gap in the DOS between the lowest bands, labeled Γ_1 and Γ_2 . This is substantiated by plotting the charge density for a repetition of this cell in Fig. 3(d), where we observe clear fluctuations and the emergence of charge “puddles.”

Importantly, however, despite initial indications for carrier localization, a $L = 10$ nm wire must still be regarded metallic [13] as an appreciable density of states exists at E_F [black dashed lines in Fig. 3(c)]. The demonstration of carrier localization for bands at E_F will require modeling of supercells with lengths approaching the localization length ($L \approx 36$ nm). These calculations, however, containing more than half a million atoms, are computationally too exhaustive and are currently not feasible.

Further insight into metallic conduction and its limits in these wires is gained through measurements at millikelvin temperatures. In Fig. 4(a), we compare the conductance G_W of both wires recorded at $T_{\text{el}} \lesssim 200$ mK. Both wires show characteristic conductance fluctuations with key differences observed in the conductance distributions, $P(G_W)$ [Figs. 4(b) and 4(c)]. These histograms have been obtained by plotting statistically independent values of the conductance within the correlation voltage, $V_C \approx 50$ mV (obtained via analysis of the autocorrelation function), and are in agreement with a Thouless energy, $E_{\text{Th}} \approx 1$ meV, at a gate lever of 0.02. According to scaling theory [19,37,38], conductance in the metallic regime follows a *normal* distribution [19,20,37–39],

$$P(G_W) \propto \exp\left[-\frac{(G_W - \langle G_W \rangle)^2}{2\delta G_W^2}\right], \quad (4)$$

centered around a mean conductance, $\langle G_W \rangle > e^2/h$. A standard deviation, $\delta G_W \sim e^2/h$, corresponding to the amplitude of universal conductance fluctuations (UCF) [19,40,41] is a fundamental manifestation of quantum

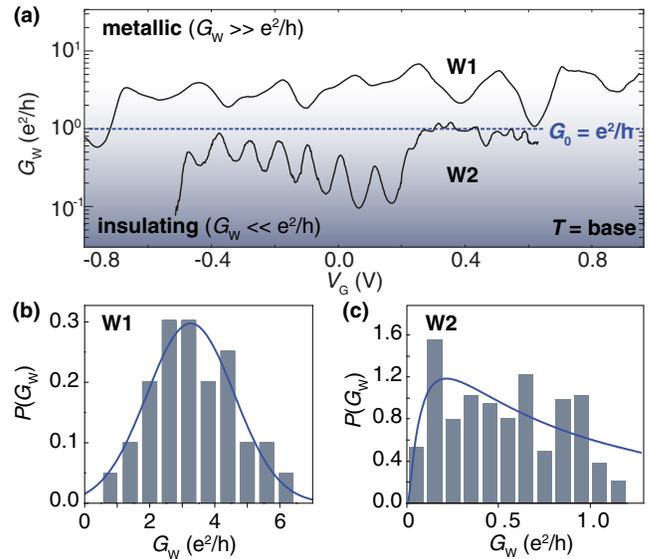


FIG. 4 (color online). (a) Differential conductance at millikelvin temperatures, comparing the 4.6 nm (W1) and the 1.5 nm (W2) wide wires. (b) and (c) Conductance histograms, $P(G_W)$, of both wires, indicating metallic and insulating behavior, respectively. The solid blue lines are fits to a normal [Eq. (4)] and a log-normal [Eq. (5)] distribution, expected in the metallic and insulating regimes, respectively.

interference effects in quasi-1D metals. Fitting the conductance distribution of the 4.6 nm wide wire (W1) (solid blue line), we find $\langle G_W \rangle = 3.3e^2/h$ and $\delta G_W = 1.3e^2/h$, confirming metallic conduction at millikelvin temperatures. The transition into the insulating regime is observed in the 1.5 nm wide wire (W2) [Fig. 4(c)]. Here, $P(G_W)$ is asymmetrically biased towards $G_W = 0$ with a slight tail towards larger conductance. Both characteristics are indicative of a *log-normal* distribution in the insulating regime ($\langle G_W \rangle < e^2/h$) [19,28,38,42],

$$P[\ln(G_W)] \propto \exp\left[-\frac{[\ln(G_W) - \langle \ln(G_W) \rangle]^2}{2[\delta \ln(G_W)]^2}\right]. \quad (5)$$

The characteristics of the conductance distribution combined with the magnitude of the mean conductance and estimates of the localization length, consequently provide a consistent indicator of metallic conduction in atomic-scale Si:P wires.

In summary, we have explored metallic conduction and its limits in atomic-scale Si:P wires, patterned by STM hydrogen lithography. Uniquely, here the valley multiplicity of the silicon conduction band provides a sixfold enhancement of the number of conducting modes at the Fermi energy. This allows quasi-1D metallic conduction over tens of nanometers with an electron mobility comparable to that measured in the corresponding 2D system. Towards the application of Si:P wires in donor-based quantum computing architectures [10,11], this implies that

STM-patterned Si:P δ -doped wires remain highly conductive, despite their atomic-scale diameters, allowing us to use them as low-resistive leads, electrostatic gates, and electron reservoirs in scalable architectures.

We acknowledge G. Scappucci for helpful discussions. This research was conducted by the Australian Research Council Centre of Excellence for Quantum Computation and Communication Technology (Project No. CE110001027) and the U.S. National Security Agency and the U.S. Army Research Office under Contract No. W911NF-08-1-0527. M. Y. S. acknowledges an ARC Laureate Fellowship.

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