Two-Dimensional Charge Transport in Disordered Organic Semiconductors

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We analyze the effect of carrier confinement on the charge-transport properties of organic field-effect transistors. Confinement is achieved experimentally by the use of semiconductors of which the active layer is only one molecule thick. The two-dimensional confinement of charge carriers provides access to a previously unexplored charge-transport regime and is reflected by a reduced temperature dependence of the transfer curves of organic monolayer transistors.

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In Si metal-oxide-semiconductor field-effect transistors, the application of a sufficiently strong positive voltage V_G on the gate electrostatically induces a two-dimensional electron gas in the p-type Si just under the SiO_2 gate dielectric [1]. Because of the large electric field at the Si-SiO_2 interface, an approximately triangular potential well is formed. The confinement in the potential well causes the three-dimensional (3D) conduction band to split into a series of two-dimensional subbands. A two-dimensional electron gas offers the possibility to study quantum transport in macroscopic systems, due to the combination of a large Fermi wavelength (40 nm) and large mean free path (exceeding 10 μm). Two-dimensional systems in a perpendicular magnetic field have the remarkable property of a quantized Hall resistance [2] which results from the quantization of the 2D subbands in a series of Landau levels.

Similar to charge carriers in Si-based metal-oxide-semiconductor field-effect transistors, carriers in organic semiconductors can also be confined in a field-effect transistor (OFET) at the semiconductor-dielectric interface [3]. In contrast to inorganic semiconductors, the charge transport occurs by hopping, which is phonon-assisted tunneling, between disorder-induced localized states at the Fermi level. The density of localized states (DOS) can be described by a Gaussian [4] or an exponential [5] distribution. With increasing carrier density, the tail states of the DOS get filled. The charge carriers have more transport states available at higher energy, and, therefore, the average mobility increases. For bulk conduction, a transport model has been derived based on variable range hopping and percolation by Vissenberg and Matters [5]. An exponential DOS is assumed, described by a characteristic temperature T_0. The model is valid for disordered systems, for temperatures well below T_0. This model gives an analytical description for the bulk conductivity as a function of carrier density and temperature. The typical hopping distance, which reflects the mean free path of a carrier in a disordered organic semiconductor, is typically 1–10 nm, depending on the carrier density.

The dependence of the measured field-effect mobility on semiconductor thickness has been reported for a number of organic compounds. For semiconductors deposited by vacuum sublimation, the determined mobility typically saturates after 2–6 monolayers [6–8] depending on the growth mode [8]. The fact that charge transport is observed even in a single organic monolayer [6] has opened the possibility of using a semiconducting self-assembled monolayer as an active component in an OFET. In a self-assembled monolayer field-effect transistor (SAMFET), the semiconductor is a single molecular layer formed spontaneously on the gate dielectric. Recently, the first SAMFETs were reported and combined into integrated circuits [9]. The demonstration of logic functionality makes self-assembly the ultimate technology for bottom-up mass production of organic electronics [10–13]. In a SAMFET the semiconductor layer thickness is comparable to that of the accumulation layer, i.e., 2 nm. The electrical transport is then by definition two-dimensional. However, the reported charge carrier mobilities in SAMFETs were similar to the corresponding bulk mobilities. In spite of the strong confinement within the single sheet of molecules, no special signatures of 2D charge transport have been observed in SAMFETs. The fundamental question is now whether 2D transport or confinement effects play a role in organic transistors. Intuitively, one could argue that because of the small mean free path of the charge carriers, typically equal to or slightly larger than the thickness of a monolayer, these effects will be small or absent. In the present study, we investigate the charge transport in monolayer OFETs and show that 2D carrier confinement is

reflected in the transfer characteristics. We demonstrate that the 2D confinement of charge carriers leads to a reduced temperature dependence of the transfer curves.

An OFET typically operates in accumulation mode, where the charges are electrostatically confined in the first few nanometers of the semiconductor near the dielectric interface [14]. The majority of the semiconductor is depleted and acts as an insulator. The current can be calculated by using the Vissenberg-Matters model [5], and an accurate description of the transport in an OFET as a function of temperature and gate bias has been demonstrated. The transport is characterized by a power-law relationship between the conductivity and the carrier concentration at the semiconductor-dielectric interface, due to the filling of the tail of the DOS. The power-law exponent is determined by the shape of the exponential DOS. In this Letter, we focus on p-type OFETs, where holes are mainly responsible for the conduction. In the Vissenberg-Matters model, the conductivity has been derived as a function of the carrier density and temperature:

$$\sigma(p) = A p^{T_0/T} \tag{1}$$

with

$$A = \sigma_0 \left(\frac{(\frac{T_0}{T})^4 \sin(\pi \frac{T}{T_0})}{(2\alpha)^3 B_c} \right)^{T_0/T}, \tag{2}$$

where p is the hole density, σ_0 is a conductivity prefactor, α^{-1} is the wave function overlap localization length, B_C is the critical number for the onset of percolation (~ 2.8 for 3D amorphous systems), and T is the temperature. This expression holds for disordered semiconductors where transport solely occurs through localized states and at temperatures T well below T_0.

To calculate the current, an expression for the hole density is required. For a semi-infinitely thick semiconductor with an exponential DOS, the distribution of holes in the accumulation layer perpendicular to the semiconductor-dielectric interface, z, is given by [15]

$$p(z) = \frac{2 k_B T_0 \varepsilon_0 \varepsilon_{sc}}{e^2 (z + z_0)^2} \tag{3}$$

with

$$z_0 = \frac{2 k_B T_0 \varepsilon_0 \varepsilon_{sc}}{e C_i V_x}, \tag{4}$$

where $k_B T_0$ is the width of the exponential DOS, k_B is the Boltzmann constant, ε_0 is the vacuum permittivity, ε_{sc} is the dielectric constant of the semiconductor, C_i is the gate capacitance per unit area, e is the electron charge, and V_x is the difference between the gate bias and the local channel potential at a point x in the channel. Equations (3) and (4) show that the carrier density quadratically decreases with distance from the interface, with an effective accumulation layer thickness z_0 of typically a few nanometers, as depicted in Fig. 1. In the linear regime, when the drain voltage $V_D \rightarrow 0$, the potential in the channel gradually changes between the source and drain. The sheet conductance is calculated by integrating the conductance over the semiconductor thickness, d_{SC}, as $G_{sh}(V_x) = \int_0^{d_{sc}} \sigma(p) dz$. The source-drain current can be derived by integrating the sheet conductance over the potential between the source and drain. When using the hole distribution of Eq. (3), the hole current for $|V_G - V_t| \geq |V_D|$ reads [16]

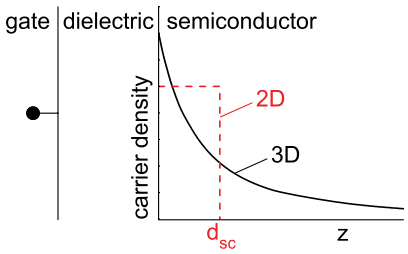

FIG. 1 (color online). Charge carrier density as a function of distance from the semiconductor-gate dielectric interface z in an OFET. In a semi-infinitely thick semiconductor, the charges distribute in 3D, resulting in a density that decreases with the square of the distance from the interface. In a monolayer semiconductor with a thickness d_{sc}, the carriers are confined in 2D, and a constant carrier density is expected.

$$I_D^{3D} = \frac{A}{e} \frac{W}{L} \left(\frac{1}{2 k_B T_0 \varepsilon_0 \varepsilon_{sc}} \right)^{T_0/T-1} C_i^{2T_0/T-1} \frac{T}{2T_0} \frac{T}{2T_0 - T} \times [(V_t - V_G)^{2T_0/T} - (V_t - V_G + V_D)^{2T_0/T}], \tag{5}$$

where W and L are the width and length of the transistor channel, respectively, and V_t is the threshold voltage, defined as the gate bias at the onset of accumulation. By using the Taylor expansion $(1 - r)^\alpha \approx 1 - \alpha r + \cdots$ for small r, with $\alpha = 2T_0/T$ and $r = -V_D/(V_t - V_G)$, the current I_D at high gate bias can be approximated by

$$I_D^{3D} \propto (V_t - V_G)^{2T_0/T-1}. \tag{6}$$

The validity of this model can easily be exemplified by studying the charge transport in organic transistors where charge carriers can distribute in 3D. As model compounds we used spin-coated, amorphous films of regio-random poly(3-hexylthiophene) (P3HT), poly(2, 5-thienylene vinylene) (PTV), or poly[2-methoxy-5-(3′, 7′-dimethyloctyloxy)-p-phenylene vinylene] (MDMO-PPV). Au source and drain contacts form an Ohmic contact for holes, yielding unipolar p-type transistors. The transistors were fabricated as described previously. Details are presented in the Supplemental Material [17]. We note that the film thickness was larger than 80 nm, much thicker than the hole accumulation layer. Transfer curves were measured as a function of temperature at low drain bias and are presented in Fig. 2(a) for P3HT. The current increases with increasing negative gate bias and with increasing temperature. As expected from Eq. (6), at high

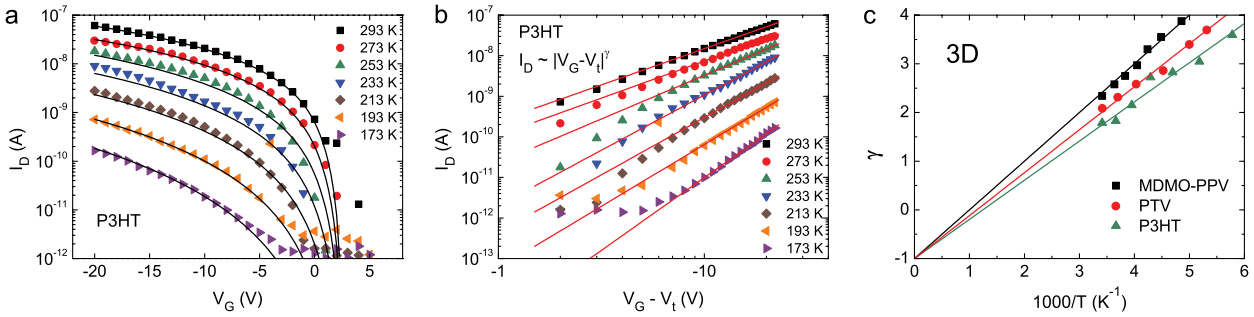

FIG. 2 (color online). (a) Experimental transfer curves of a P3HT field-effect transistor measured as a function of temperature, at a drain bias of $V_D = -2$ V. Curves calculated according to Eq. (5) are presented as black lines, using the following parameters: $T_0 = 402$ K, $\sigma_0 = 1.76 \times 10^6$ S/m, $\alpha^{-1} = 1.4$ Å, and $V_t = 2.5$ V. The semiconductor thickness was 80 nm, and the width and length of the channel were 2500 and 10 μm, respectively. (b) The same experimental data as in (a) plotted on a double logarithmic scale, corrected for a threshold voltage of 2.5 V. The red lines are a power-law fit at high gate bias, for each temperature. (c) The power-law exponent γ extracted from (b) versus inverse temperature. A similar analysis was performed on literature data reported for MDMO-PPV and PTV [18,19]. The solid lines are a guide to the eye.

gate bias a power-law dependence on the gate bias is observed [Fig. 2(b)]. For each temperature, the exponent of the observed power law was plotted versus $1/T$. A straight line was found, as shown in Fig. 2(c). The extrapolated line crosses the exponent axis at the value of -1, as predicted by Eq. (6) for $T \rightarrow \infty$. This agreement indicates indirectly that the charge carrier profile calculated for an infinite semiconductor thickness is indeed valid for the P3HT transistor. We performed similar analysis on data of OFETs based on PTV and MDMO-PPV [18,19]. In both cases a power-law dependence was observed. The extrapolated exponents cross at -1 in a $1/T$ plot, as shown in Fig. 2(c). From the slopes of Fig. 2(c), the values for T_0 can be found, the parameter that indicates the width of the exponential DOS. For P3HT, MDMO-PPV, and PTV we obtain $T_0 = 402$ K, $T_0 = 500$ K, and $T_0 = 441$ K, respectively. By using the determined T_0, the transfer curves as a function of bias and temperature can be fully described with Eq. (5), as presented by the solid lines in Fig. 2(a) for P3HT. The calculations for MDMO-PPV and PTV are presented in the Supplemental Material [17].

To study the charge transport in a transistor where charges are physically confined to a 2D semiconducting monolayer, we fabricated SAMFETs and transistors with an evaporated monolayer. The SAMFETs were fabricated by self-assembly of a monolayer of the conjugated molecule chloro[11-(5′′′′-ethyl- 2, 2:5′, 2′′:5′′, 2′′′:5′′′, 2′′′′-quinquethien-5-yl)undecyl] dimethylsilane between the source and drain electrodes. The evaporated monolayer transistors were fabricated from α-sexithiophene (T6). In both cases, Ohmic contacts for holes are formed with Au, yielding p-type transistors. Experimental details are presented in the Supplemental Material [17].

Linear transfer curves of a SAMFET were measured as a function of temperature and are presented in Fig. 3(a). Similar to the transistors with a thick semiconductor, the current decreases for lower temperatures. Furthermore, a power-law dependence of the current on gate bias is

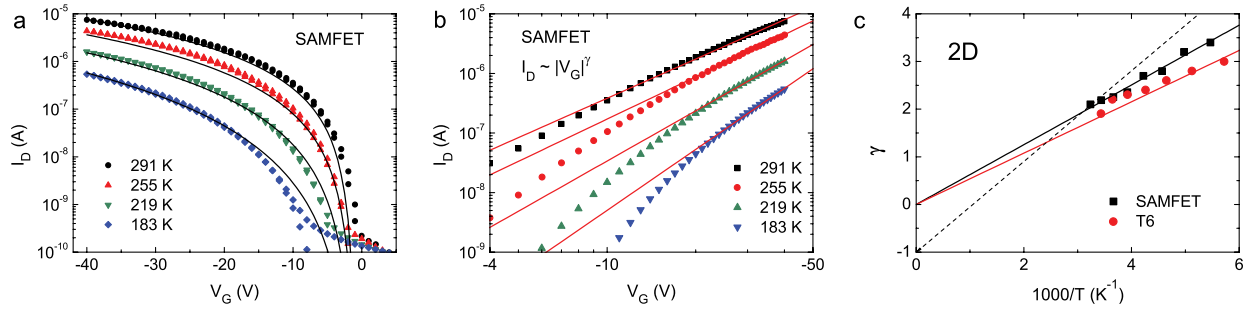

FIG. 3 (color online). (a) Experimental transfer curves of a SAMFET measured as a function of temperature, at a drain bias of $V_D = -2$ V. Curves calculated according to Eq. (8), based on a step-function carrier distribution, are presented as black lines. The following parameters were used: $T_0 = 627$ K, $\sigma_0 = 4 \times 10^6$ S/m, $\alpha^{-1} = 4.3$ Å, $V_t = -1$ V, and $W/L = 20\,000/20$. The semiconductor thickness was taken as 2 nm. (b) The same experimental data as in (a) plotted on a double logarithmic scale. The red lines are a power-law fit at high gate bias, for each temperature. (c) The exponent extracted from (b) versus inverse temperature. Similar analysis was done for a T6 monolayer transistor, as presented in the Supplemental Material [17]. The solid lines are a guide to the eye. Extrapolating the monolayer data to infinite temperature does not agree with Eq. (6), as indicated by the dashed line.

observed at high gate bias; see Fig. 3(b). The extracted exponent of the power law is plotted versus inverse temperature in Fig. 3(c). Again a straight line was found. However, the extrapolated line does not cross the exponent axis at a value of -1 but at a value close to 0. The temperature dependence of the power-law exponent of the SAMFET is weaker than that for the thick semiconductors. Transfer curves of T6 monolayer transistors show a similar temperature dependence as that of the SAMFETs. The exponent of the transfer curves as a function of inverse temperature are plotted in Fig. 3(c), also yielding a straight line crossing the exponent axis close to 0.

The question is whether the weaker temperature dependence in the monolayer transistors is related to the carrier distribution. To answer this question, we compare the carrier distribution in thick and thin semiconducting films, and we study the impact of the distribution on the charge transport. As shown above, in a thick semiconductor, the carrier density decreases with the square of the distance from the semiconductor-gate dielectric interface. However, for a monolayer semiconductor, the assumption of infinite thickness does not hold. The carriers accumulated by the gate bias are confined in the monolayer; there is no space to redistribute. Therefore, a density proportional to the gate bias but uniform in the semiconductor seems reasonable, as illustrated by the step function in Fig. 1. The local hole density then reads

$$p = \frac{C_i V_x}{e d_{\mathrm{sc}}}, \tag{7}$$

where d_{sc} is the semiconductor thickness. As the semiconductor thickness we take 2 nm, the length of the conjugated part of the molecule. By using this step-function carrier profile, an expression for the current can be derived. We start with the local conductivity relation of Eq. (3).

The source-drain current can again be derived by integrating the sheet conductance $G_{\mathrm{sh}}(V_x) = \int_0^{d_{\mathrm{sc}}} \sigma(p) dz$ over the potential between the source and drain. However, now we use the step function for the hole concentration of Eq. (7). The current then reads

$$I_D{}^{\mathrm{2D}} = A \frac{W}{L} (d_{\mathrm{sc}})^{1-(T_0/T)} \left(\frac{C_i}{e}\right)^{T_0/T} \frac{T}{T_0 + T} [(V_t - V_G)^{(T_0/T)+1} - (V_t - V_G + V_D)^{(T_0/T)+1}]. \tag{8}$$

By using again the Taylor expansion, the current at high gate bias can be approximated by

$$I_D{}^{\mathrm{2D}} \propto (V_t - V_G)^{T_0/T}. \tag{9}$$

The resulting equation for the current in a monolayer transistor at high gate bias, Eq. (9), is also a simple power law, similar to Eq. (6). The main difference is in the exponent: T_0/T versus $2T_0/T - 1$. The used hopping charge-transport description is the same for thick and thin films. However, the carrier confinement results in qualitatively different temperature dependence. From Eq. (9), it is clear that the extrapolated straight line in Fig. 3(c) should, for infinite T, cross the exponent axis at the value 0 instead of -1, which is indeed consistent with the data. From the slope of Fig. 3(c), the values for T_0 can be found. For the SAMFET, we obtain $T_0 = 627$ K and for the T6 monolayer $T_0 = 539$ K. By using the determined values for T_0, the transfer curves as a function of bias and temperature can be fully described with Eq. (8), as presented by the solid lines in Fig. 3(a) for the SAMFET. Correspondingly, the calculations of the current in transistors with a T6 monolayer are presented in the Supplemental Material [17]. This is the first observation of charge carrier confinement and 2D transport in organic semiconductors.

Experimentally, it is challenging to find a model system to demonstrate a transition from 2D to 3D transport. It has been shown that in multilayer small molecule transistors the electrical transport takes place in the first few monolayers. The charge carrier density follows from electrostatics, with the highest density in the first monolayer and then decreasing in the next layers. In contrast to the charge carrier distribution, however, it has been shown that a major part of the current is transported not in the first layer but in the second and third layers [7,8]. This clearly indicates that the mobility is higher in the second and third layers. The origin could be that electrostatic interactions with the gate dielectric affect especially the first monolayer, yielding a substantial broadening of the DOS. In the model, one would have to include a depth-dependent parameter T_0 in order to correctly describe the transition from 2D to 3D. As a consequence, the linear extrapolation to infinite temperature becomes meaningless for such multilayer transistors. Therefore, here we compare single monolayers with a single exponential DOS, with bulk organic polymers that are less affected by the dielectric induced disorder as their intrinsic disorder prevails.

In summary, we have analyzed the effect of carrier confinement on the charge-transport properties of organic field-effect transistors. Spatial confinement was achieved by the use of semiconductors of which the active layer is only one molecule thick, either by self-assembly or by thermal evaporation. Electrical measurements of the resulting monolayer transistors were compared to measurements of organic transistors with a thick semiconducting polymer as the active layer. We have demonstrated that the 2D transport in organic semiconductors is reflected in a reduced temperature dependence of the transfer characteristics.

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