Giant Piezoresistance Effects in Silicon Nanowires and Microwires

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(Received 13 October 2010; published 23 November 2010)

The giant piezoresistance (PZR) previously reported in silicon nanowires is experimentally investigated in a large number of depleted silicon nano- and microstructures. The resistance is shown to vary strongly with time due to electron and hole trapping at the sample surfaces independent of the applied stress. Importantly, this time-varying resistance manifests itself as an apparent giant PZR identical to that reported elsewhere. By modulating the applied stress in time, the true PZR of the structures is found to be comparable with that of bulk silicon.

DOI: 10.1103/PhysRevLett.105.226802 PACS numbers: 73.50.Dn, 73.50.Gr, 73.63.Nm

As the most well studied and commercially important semiconductor, reports of new physical phenomena in silicon receive much attention. A recent example is giant piezoresistance (PZR) [1], where the change in resistance of silicon nanowires due to an applied mechanical stress, X, was reported to be orders of magnitude larger than that of bulk silicon [2]. This report is highly cited [3–8] in part because it may represent another example of the effect of size on the physical properties of an otherwise well-characterized material [3,9,10]. Additionally, giant PZR is currently seen as a potential breakthrough means of detecting motion in nanoelectromechanical systems [5] since PZR sensitivity scales better than optical or capacitive techniques [4,11,12]. Moreover, since mechanical stress is a key element for performance enhancement of microelectronic devices [13], the physical mechanism behind giant PZR could prove important for the design of future nanoscale transistors. As yet there is no consensus concerning the origins of giant PZR, although two models have some support [14,15]. One [14] is based on a surface quantization effect predicted to occur in the first few silicon monolayers, while the other [15] is based on a stress-induced shift of the surface Fermi level in depleted structures resulting from a change in surface charge. The atomic length scale of the former seems to be in disaccord with the typical wire diameters reported in the literature, which are at least several tens of nanometers, whereas the characteristic length scale of the latter is the surface depletion layer width (1 nm to 10 μm, depending on the doping density). Tellingly, it was noted that the initially reported giant PZR occurred only in depleted nanowires [1,15] and subsequent claims of giant PZR involve depleted silicon [4,6,7].

Here we show that in depleted structures resistance changes are dominated by electron and hole trapping at the surface. Quite unexpectedly this dielectric relaxation (which is independent of X) results in apparent giant PZR identical to that initially reported in silicon nanowires [1]. The true PZR can only be measured by modulating the mechanical stress in time as outlined below. In all cases, independent of the sample dimensions, it is comparable with that of bulk silicon [2].

A variety of unreleased and released, n-type and p-type microwires, nanowires, and nanoribbons were fabricated using a top-down approach from silicon-on-insulator wafers of different device layer thicknesses (h) and background doping levels [see Fig. 1 and Table I]. The background doping density was chosen so that the surface

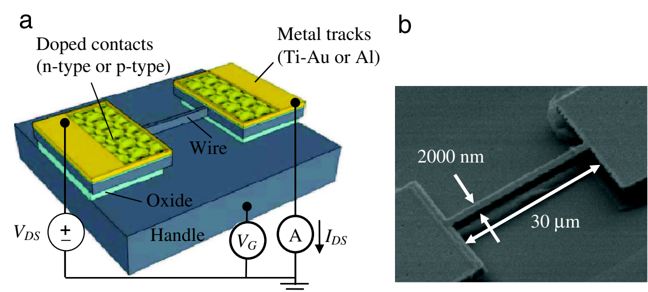

FIG. 1 (color online). (a) Typical layout of nanostructures, showing symbols used in the text and (b) SEM image of a released 2000 nm × 2000 nm × 30 μm microwire.

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TABLE I. True π_l measured on all samples.

h (nm)	w (nm)	l (μm)	W_D (nm)	Doping	Released?	π_l ($\times 10^{-11}$/Pa)
2000	2000	30	8000	p	no	96.6, 90, 102, 96.8, 101, 107, 87.5
2000	3000	30	8000	p	no	96.2, 102
2000	2000	30	8000	p	yes	205, 115, 125
2000	3000	30	8000	p	yes	116
100	50	1	800	p	no	58.5
75	50	1	800	p	no	74.6
50	50	1	800	p	no	76.9
200	2000	30	800	n	no	−76, −77.4, −99, −48.9, −60.8, −46.3
200	3000	30	800	n	no	−69.7, −50.4

depletion layer width [16] $W_D > h$, thereby ensuring that the device layer is depleted. All structures were etched using deep reactive ion etching and either thermally activated phosphorous (n-type) or boron (p-type) were used as dopants for the Ohmic contacts (1×10^{20} cm^{-3}). Ti/Au (A1) was used for the $n(p)$-type contacts. For released structures, the buried oxide was removed using a HF (50%) etch followed by supercritical CO_2 drying. All wires and ribbons are aligned with the $\langle 110 \rangle$ crystal direction along which the mechanical stress is applied using a three-point bending method. On wafer, large area strain gauges were also fabricated, thereby allowing X to be monitored *in situ*. The three-point bending setup, which uses a piezoelectric pusher, permits rapid and repeatable switching between zero-stress and X regimes; this experimental technique is different than the usual one where X is ramped or stepped monotonically with time [1,4,6,17]. The conductance, G, was measured by monitoring the current ($I_{\rm DS}$) induced by an applied voltage ($V_{\rm DS}$) while the silicon handle was held at a constant back-gate voltage, V_G [see Fig. 1].

The need to separate the time-varying and stress-induced resistance is illustrated with the experimental data shown in Fig. 2. At $t = 0$, $V_{\rm DS}$ is stepped from 0 V to 0.5 V across a 200 nm $\times$ 2000 nm $\times$ 30 μm nanoribbon with n-type contacts, while X was alternated between 0 MPa and −13.3 MPa. Over 8000 s, a stress-independent reduction in G by 27% followed by a slower increase is observed, similar in form to that observed optically during dielectric relaxation [18]. Using the stress modulation technique, sequential measurements of $I_{\rm DS}$ are made at zero stress (times t_1 and t_3) and with X (times t_2 and t_4) (see inset). The stress-induced change in conductance, $\Delta G/G_0 = I_{\rm DS}/I_{\rm DS,0}$, at t_3 is found by linear interpolation to be $[2I_{\rm DS}(t_3) - I_{\rm DS}(t_2) - I_{\rm DS}(t_4)]/[I_{\rm DS}(t_2) + I_{\rm DS}(t_4)]$ and remains at a constant −0.54% [see bottom panel, Fig. 2] over time. The longitudinal PZR coefficient, $\pi_l = -41 \times 10^{-11}$ Pa^{-1}, in excellent agreement with the bulk value for $\langle 110 \rangle$-oriented n-type silicon [2]. Here the usual definition is used; $\pi_1 = \hat{a}, 1/X \times \Delta G/G_0$ where G_0 is the zero-stress conductance. If the stress had been ramped linearly in time, the true PZR would have been masked by the nonstress-related drift of G which is 10–100 times larger. Indeed, the implicit assumption when using a linearly ramped stress technique is that the G_0 remains constant for the entire measurement; clearly not the case in depleted silicon that, as will be seen below, is sensitive to surface charging. Similar dynamic changes in the resistance of silicon nanowires have been reported previously [3,8,19–21].

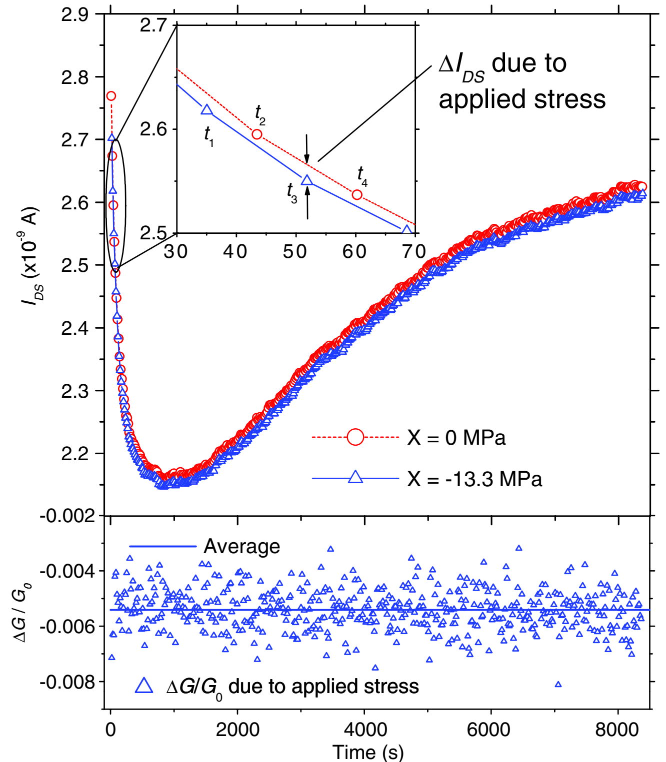

FIG. 2 (color online). (Top panel) Measurement of $I_{\rm DS}(t)$ after applying a source-drain voltage of $V_{\rm DS} = 0.5$ V at $t = 0$ across a 200 nm $\times$ 2000 nm $\times$ 30 μm n-type nanoribbon and alternating X between 0 MPa and −13.3 MPa. V_G was held at 0 V for the duration of the measurement. The inset indicates the sequence of measurements used in the stress modulation technique, where the lines are a guide to the eye. (Bottom panel) Relative conductance change due solely to X.

Figure 3(a) presents the results of a measurement designed to highlight how temporal changes in G_0 manifest themselves as an apparent giant PZR. Each solid line represents a single $I_{\rm DS} - V_{\rm DS}$ sweep for a particular X, with $V_{\rm DS}$ swept from -1 V to 1 V in increments of 0.1 V. X is incremented between each $V_{\rm DS}$ sweep from -13.3 MPa to 13.3 MPa, including a 0 MPa curve shown in black. The apparent stress-related change in the slope of the $I_{\rm DS} - V_{\rm DS}$ curves closely resembles published experimental data produced as evidence for giant PZR (see Fig. 2b of Ref. [1]). During this measurement sequence, however, it is possible to monitor the true zero-stress resistance using the stress modulation technique shown graphically in the inset of Fig. 2. For clarity this is shown only for the first $I_{\rm DS} - V_{\rm DS}$ sweep as black diamonds in Fig. 3(a), revealing that the true PZR is negligible and that the changes in slope of the $I_{\rm DS} - V_{\rm DS}$ curves are due to a nonstress-related temporal variation in G_0. Figure 3(b) shows the apparent PZR [open triangles, calculated relative to the black line in Fig. 3(a)] and the true PZR (open diamonds, measured with respect to the true zero-voltage resistance). For clarity, the real and apparent PZRs are only depicted for an applied voltage $V_{\rm DS} = 0.5$ V, but similar results are obtained at all voltages. The apparent PZR has an exponential dependence on X like the curves obtained in Ref. [1] (see Fig. 2c of that article) although other forms (including those labeled C, Z, and I in Ref. [1]) are observed at different moments along relaxation curves of the type

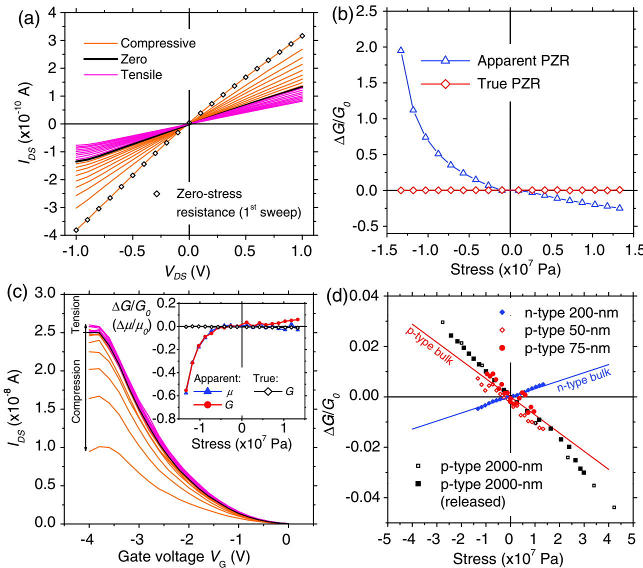

FIG. 3 (color online). (a) Successive $I_{\rm DS} - V_{\rm DS}$ measurements of a 50 nm × 50 nm × 1 μm p-type nanowire with $V_G = 0$ V. (b) Apparent and true PZR extracted from the $V_{\rm DS} = 0.5$ V data points in (a). (c) Successive $I_{\rm DS} - V_G$ measurements of a 50 nm × 50 nm × 1 μm p-type nanowire with $V_{\rm DS} = 0.5$ V, and an inset showing the apparent changes in mobility and conductance (calculations described in the methods section). (d) Relative conductance change due solely to X of various samples extracted using the stress modulation technique, together with typical values for n-type and p-type bulk silicon.

shown in Fig. 2. Changes that are even larger or of opposite sign are equally possible. π_l obtained from Fig. 3(b) is 450×10^{-11} Pa^{-1} and 77×10^{-11} Pa^{-1} (c.f. bulk value, Ref. [2]) for the nonstress-related and true PZR, respectively. Again, this apparent giant PZR is indistinguishable from true PZR if the stress modulation technique is not used.

By measuring $I_{\rm DS}$ versus V_G and by assuming a linear relationship between the slope of this characteristic and the mobility, the giant PZR was attributed to a mobility variation [1]. This measurement is replicated using a 50 nm × 50 nm × 1 μm p-type nanowire. The results are presented in Fig. 3(c), demonstrating that the apparent mobility extracted from the slope of an $I_{\rm DS} - V_G$ measurement can also change over time independently of X. The sign and magnitude of this change is the same as the apparent stress-dependent conductance change. The true stress-dependent conductance change is consistent with bulk silicon PZR (see inset). Figure 3(d) shows the true values of $\Delta G/G_0$ as a function of X obtained for four different, depleted silicon structures, together with the values expected from bulk silicon. Regardless of lateral wire size, or whether the device is released or not, the true PZR compares well with that of nondepleted, bulk silicon. Results from all measured samples can be found in Table I.

To better understand the origin of the dynamic conductance changes, a similar approach to that used in transistors is employed, in which a measurement of the subthreshold current,

$$I_{\rm DS} = I_0 \exp[(V_G + \Delta V_G)/S], \quad (1)$$

is made [22]. Here I_0 is a constant, S is the subthreshold slope, and ΔV_G is the shift in the effective gate voltage due to trapped oxide charge. ΔV_G at time t can then be expressed as

$$\Delta V_G(t) - \Delta V_G(0) = S \ln\frac{I_{\rm DS}(t)}{I_{\rm DS}(0)} - V_G(t) + V_G(0), \quad (2)$$

where S can be measured directly from a rapid $I_{\rm DS}$ versus V_G measurement. Measured $V_G(t) - V_G(0)$ data are then fitted by adapting a semiempirical model developed for positive charge trapping in metal-oxide-semiconductor (MOS) capacitors [23] so that it accounts for both positive and negative oxide charge trapping. The model assumes that the sheet density N of trapped charge has a saturation value N_∞ that depends linearly on the electric field across the oxide $\xi_{\rm ox}$, so that $N_\infty = \alpha\xi_{\rm ox}$ where α is a constant with units of cm^{-1} V^{-1}. N approaches N_∞ with a time constant τ, so that $\partial N/\partial t = -[N(t) - N_\infty]/\tau$, where τ is related to the capture cross section of the trap and the current density through the oxide [23,24]. The contribution of the trapped charge to the gate voltage is given by [23] $\Delta V_G = qNd_{\rm ox}/\epsilon_{\rm ox}$, where $d_{\rm ox}$ is the oxide thickness, q is the charge on an electron, and $\epsilon_{\rm ox}$ is the oxide permittivity. Figure 4 presents measured values of $V_G(t) - V_G(0)$ for a 200 nm × 2000 nm × 30 μm n-type nanoribbon, where

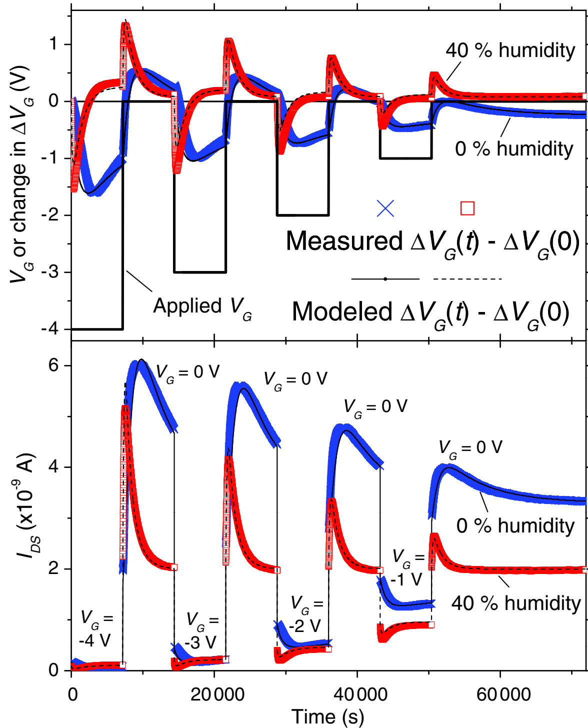

FIG. 4 (color online). Measurements and modeling of the change in ΔV_G due to oxide charge trapping and the values of I_{DS} for a 200 nm $\times$ 2000 nm $\times$ 30 μm n-type nanoribbon, measured in 0% and 40% relative humidity. The source-drain voltage V_{DS} was held constant at 0.2 V, while step changes were applied to the gate voltage V_G as indicated in the top panel.

$V_{DS} = 0.2$ V and a series of positive and negative steps were applied to V_G. Two sets of measurements were taken: one in a dry nitrogen atmosphere (0% relative humidity) and one in a relative humidity of $\approx$ 40%. Each set of data is modeled using one type of electron (hole) trap characterized by $N_e(0)$, α_e and τ_e [$N_h(0)$, α_h, and τ_h]. Excellent agreement is reached between the model and the measured values of $V_G(t) - V_G(0)$ over each 20-hour measurement period. The calculated current is determined by using the modeled values of $V_G(t)$ in Eq. (2) and by adjusting the parameter I_0. This closely matches the measured current as shown in the bottom frame of Fig. 4. This treatment yields several important insights into the origin of the dynamic conductance changes: (i) The observed changes in the current are the result of charge trapping of electrons and holes in SiO_2 layers at the wire surfaces; (ii) The changes in the current are much more rapid at higher relative humidity, consistent with the presence of water-related charge traps [23,25]; (iii) The fitted values of the constant α_h for the hole traps (1.2×10^{12} cm^{-1} MV^{-1} at 0% relative humidity and 1.5×10^{12} cm^{-1} MV^{-1} at 40% relative humidity) are almost identical to values obtained in MOS capacitor oxides [23]; (iv) Electron traps are associated with the rapid initial change in I_{DS}, while hole traps are associated with the slower change in the opposite direction, consistent with observations of charge trapping in MOS capacitors [24] and dielectric relaxation at Si/SiO_2 interfaces [18]. This is strong evidence that the observed dynamic conductance changes are due to water-related charge traps in the oxide layer at the silicon surface. Consistent with this, the apparent giant PZR of Ref. [1] was also shown to depend strongly on the characteristics of this oxide layer.

In conclusion, charge trapping and detrapping can mask the true PZR of depleted structures and mistakenly lead to claims of an apparent giant PZR. In more than 20 different depleted samples, the true PZR is found to be comparable with known values for bulk silicon (see Table I) [26]. This is in stark contrast to previous reports of giant PZR in structures of similar dimensions and doping levels. While this does not rule out giant PZR in depleted silicon structures, future claims must conclusively demonstrate that any measured resistance change be solely due to X.

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