Thermodynamics and Kinetics of Graphene Growth on SiC(0001)

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The formation of surface phases on the Si-terminated SiC(0001) surface, from the Si-rich (3×3) structure, through the intermediate (1×1) and $(\sqrt{3} \times \sqrt{3}) - R30°$ structures, to the C-rich $(6\sqrt{3} \times 6\sqrt{3})$ phase, and finally epitaxial graphene, has been well documented. But the thermodynamics and kinetics of these phase formations are poorly understood. Using *in situ* low energy electron microscopy, we show how the phase transformation temperatures can be shifted over several hundred degrees Celsius, and the phase transformation time scales reduced by several orders of magnitude, by balancing the rate of Si evaporation with an external flux of Si. Detailed insight in the thermodynamics allows us to dramatically improve the morphology of the final C-rich surface phases, including epitaxial graphene.

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The unusual and exotic electronic properties of graphene have captured the imagination of basic scientists and exploratory device technologists alike. Over the last three years, many exciting results have demonstrated that carbon-based electronics, potentially combining the strengths of single and multiwall carbon nanotubes with the unique properties of graphene, may over the next one or two decades supersede silicon-based microelectronics technology [1]. However, the highest performance graphene devices have been fabricated on mechanically exfoliated flakes, a fabrication strategy that does not lend itself to large-scale integration. In order to realize the synthesis of large-area graphene substrates, several routes are being pursued, including chemical synthesis and placement [2], as well as growth of graphene on both metallic [3] and semiconducting substrates [4]. Compatibility with existing semiconductor processing technologies would bring many advantages, and the epitaxial growth of graphene on SiC is considered one of the most promising options. The growth of graphitic films on SiC was first observed some three decades ago [5]. This can be accomplished on both Si-terminated SiC(0001) and C-terminated SiC(0001 bar) surfaces, by heating a suitably cleaned SiC wafer to temperatures in excess of 1100 °C. However, on the Si-terminated surface, it is found that the surface morphology is difficult to control, leading to the presence of numerous thermal etch pits on the surface, and relatively small graphene domain sizes [6]. The graphene film has a single azimuthal orientation relative to the substrate, allowing in principle for high quality epitaxial growth. On the C-terminated surface, on the other hand, the graphene flakes also have relatively small domain sizes, and additionally suffer from large azimuthal misorientations from layer to layer, and a rather rough surface morphology [7]. Thus, while growth of graphene on SiC is promising, much work remains to improve morphology, grain size, and epitaxial quality so as to be able to take full advantage of the unique properties of graphene.

Here, we focus on the growth of graphene on the Si-terminated surface. The phase formation sequence [8], from Si-rich to epitaxial graphene, is illustrated in Fig. 1. The initial Si-rich (3×3) phase can be obtained by exposing a well-outgassed SiC surface to a Si flux at a temperature of 800 °C. Starting from this (3×3) phase, the higher temperature phases are obtained simply by heating the wafer to increasing temperatures, leading to progressive desorption of Si from the surface. However, upon reaching the C-rich $(6\sqrt{3} \times 6\sqrt{3})$ and graphene phases, it is observed that the surface has become rough [6], even though the surface morphology was smooth at lower temperatures. The transformation from the $\sqrt{3}$ to $6\sqrt{3}$ phase was explored by LEEM and AFM previously, and the developing surface roughness was linked to kinetic limitations in the mobilities of atomic steps [6]. While Fig. 1 shows the sequence of phases, this does not address the thermodynamics of these phase transitions. Necessarily, heating in Ultra High Vacuum (UHV) at temperatures where Si evaporates from the surface drives the surface out of thermodynamic equilibrium, with little opportunity to control the kinetics of the phase transformations. Over the temperature range employed here, 800–1300 °C, only Si evaporates from the substrate, leading to gradual C enrichment of the surface. Other sample cleaning strategies include high temperature heating in the presence of a high pressure of hydrogen, which may lead to etching of both Si and C; however, this will not be considered here. We find that the reaction can be reversed from C rich to Si rich by adding an external background pressure of Si vapor:

$$(3\text{x}3) \xrightarrow{1000^{o}\text{C}} (1\text{x}1) \xrightarrow{1080^{o}\text{C}} (\sqrt{3}\text{x}\sqrt{3}) \longrightarrow (6\sqrt{3}\text{x}6\sqrt{3})+\text{graphene}$$

FIG. 1 (color online). Sequence of surface phases observed in the Si-terminated SiC(0001) surface, from Si rich on the left-hand side, to C rich on the right-hand side. Approximate transition temperatures are taken from Ref. [8].

$$\text{SiC (Si rich)}\langle - \rangle\text{SiC(C rich)} + \text{Si(vapor)} \qquad (1)$$

The presence of a background pressure of Si allows the surface to be equilibrated in a pressure-temperature phase diagram, enabling the exploration of the thermodynamics of the various phase transformations in near-equilibrium conditions. We have explored this *p-T* diagram using *in situ* LEEM [9], which enables the real-space and real-time observation of the surface at high temperatures in the presence of a Si background pressure. Thus, we have studied the surface over a temperature range of 800–1300 °C, in the presence of a background pressure of Si ranging from $1 \times 10^{-8} - 1 \times 10^{-6}$ Torr. We directly observe the phase transformations, both in real space using LEEM, and in reciprocal space using Low Energy Electron Diffraction (LEED). We have used disilane as a source of Si. At the temperatures and pressures used in our studies, disilane decomposes on the surface into Si and H, with H desorbing from the surface. At much high pressures, H can be used to etch; however, we are very far from this regime.

All experiments were performed in the IBM LEEM-II instrument [9]. Insulating 4H-SiC(0001) samples (Cree) were cleaned by outgassing at ~800 °C, and were then exposed at this temperature to disilane gas at a pressure of 1×10^{-7} Torr for several minutes. After this cleaning procedure, the surface shows a distinct (3×3) LEED pattern. The phase transformations shown in Fig. 1 were then explored as a function of both temperature and disilane background pressure to produce a pressure-temperature phase diagram for this surface. Temperatures were measured with an IR-pyrometer. On a given sample, phase transition temperatures were reproducible to within 10 K. Sample-to-sample variations were ~30 K or less. In the absence of disilane, our data were in good agreement with Ref. [8]. Figure 2(a) shows a real-space image of the $(3 \times 3) - (1 \times 1)$ phase transition at a disilane pressure of 8×10^{-7} Torr. In this bright-field LEEM image, the (3×3) phase is bright, the (1×1) phase dark. The (1×1) phase is seen to preferentially form along atomic steps (between red arrows) and along (3×3) domain boundaries (between blue arrows). The (3×3) and (1×1) phases coexist over a temperature range of 10–15 °C, suggesting that a difference in surface stress between the two phases stretches the phase coexistence over a finite temperature window, analogous to the Si(111)$(7 \times 7) - (1 \times 1)$ phase transition [10]. We take the temperature at which the (1×1) phase first appears in the image (upon heating) as the nominal phase transition temperature. Similarly, for the $(1 \times 1) - (\sqrt{3} \times \sqrt{3})$ phase transition, we take the temperature at which the (1×1) phase first appears (upon cooling) as the nominal phase transition temperature. Upon further heating, the $(6\sqrt{3} \times 6\sqrt{3})$ phase forms, as shown in Fig. 2(b). Again, we take the temperature at

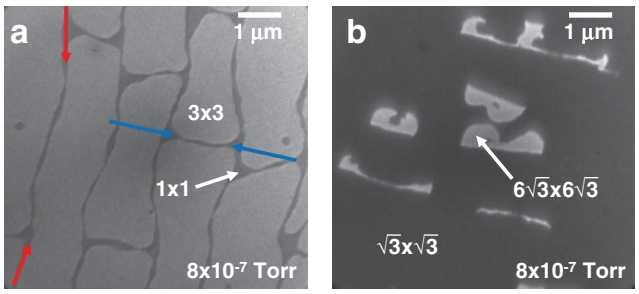

FIG. 2 (color). Bright field LEEM images obtained at the $(3 \times 3) - (1 \times 1)$ phase transition (a) and at the $(\sqrt{3} \times \sqrt{3}) - (6\sqrt{3} \times 6\sqrt{3})$ phase transition (b), in the presence of a Si background pressure of 8×10^{-7} Torr. In (a), we see the formation of the (1×1) phase along atomic steps (between red arrows) and at (3×3) domain walls on the atomic terraces (between blue arrows). Field of view 7 μm.

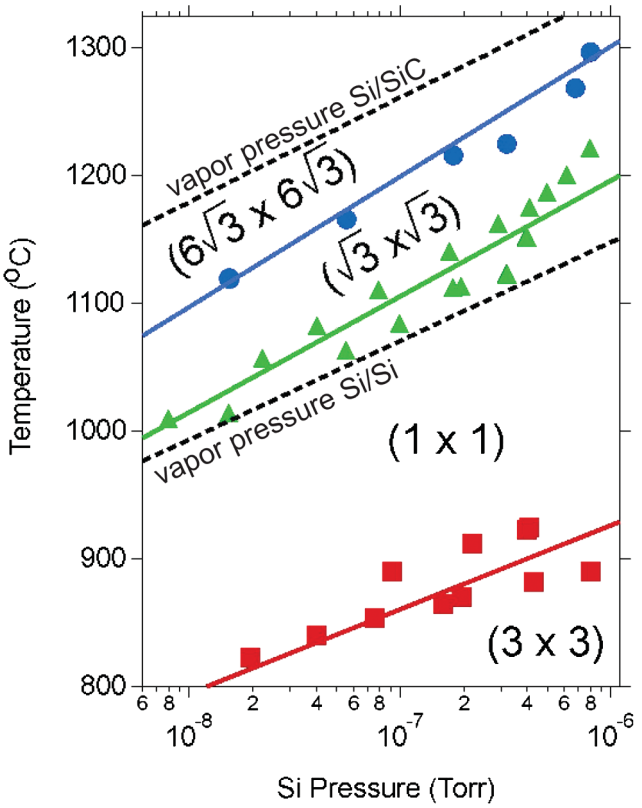

FIG. 3 (color). Pressure-temperature phase diagram for the 4H-SiC(0001) surface. The Si background pressure along the horizontal axis is taken as two times the disilane partial pressure, as each disilane molecule contains two Si atoms. From low to high temperature, we observe the phase formation sequence of Fig. 1, but with the transition temperature strongly dependent on the Si background pressure. Red, green, and blue lines are guides to the eye, and separate the different phase regions. The lower dashed black line is the equilibrium vapor pressure of Si over a Si substrate, while the upper dashed black line is the extrapolated equilibrium vapor pressure of Si over SiC (Ref. [11]). The $(1 \times 1) - (\sqrt{3} \times \sqrt{3})$ phase transition closely follows the Si over Si vapor pressure line, while the $(\sqrt{3} \times \sqrt{3}) - (6\sqrt{3} \times 6\sqrt{3})$ falls closer to the Si over SiC vapor pressure line.

which the $6\sqrt{3}$ first appears in the image as the phase transition temperature. Upon heating in UHV, it is in general not possible to return to the Si-rich phases, and it is not *a priori* clear if the structural transformations are reversible or irreversible, nor if they are hysteretic in nature or occur at a well-defined temperature. In the presence of disilane, however, we observe that all three phase transitions, $(3 \times 3) - (1 \times 1)$, $(1 \times 1) - (\sqrt{3} \times \sqrt{3})$, and $(\sqrt{3} \times \sqrt{3}) - (6\sqrt{3} \times 6\sqrt{3})$ are fully reversibly with stable phase coexistence at each transition, indicating that all three transitions are of first order at a well-defined phase transition temperature.

Figure 3 shows the pressure—temperature dependence of these transitions, measured with LEEM and LEED on three different samples. Particularly striking is the wide range of temperatures over which the phase transitions can be varied by the addition of relatively low Si background pressures. For comparison, the Si(111)$(7 \times 7) - (1 \times 1)$ phase transition could be lowered by ~3 °C by adding a disilane background pressure of 3×10^{-7} Torr[10]. Here, we are able to shift both the $(1 \times 1) - (\sqrt{3} \times \sqrt{3})$ and $(\sqrt{3} \times \sqrt{3}) - (6\sqrt{3} \times 6\sqrt{3})$ up by as much as 250 °C by adding a similar amount of disilane.

The equilibrium vapor pressure of Si over both Si and SiC substrates have been measured previously [11], and these equilibrium vapor pressures are also shown in Fig. 3 as black dashed lines. The heat of sublimation of Si from Si (108.3 + / − 3 kcal/mole) is lower than that from SiC (126.3 + / − 3 kcal/mole), leading to a lower vapor pressure over SiC at a given temperature. The $(1 \times 1) - (\sqrt{3} \times \sqrt{3})$ transition closely follows the Si over Si vapor pressure, while the $(\sqrt{3} \times \sqrt{3}) - (6\sqrt{3} \times 6\sqrt{3})$ transition occurs closer to the Si over SiC vapor pressure. The low temperature (3×3) structure is generally considered to consist of a Si layer on top of SiC, decorated with Si tetramers in a (3×3) network [12]. The $(3 \times 3) - (1 \times 1)$ transition is most likely a disordering transition, where the Si layer remains intact, but the ordered tetramer network is replaced by a disordered lattice gas of Si adsorbates. This phase transformation is not as sensitive to the presence of a Si background pressure as the higher temperature phase transitions. The $(\sqrt{3} \times \sqrt{3})$ phase is believed to consist of Si adatoms adsorbed in so-called $T4$ sites, directly on the bulk terminated SiC substrate [13]. Therefore, the $(1 \times 1) - (\sqrt{3} \times \sqrt{3})$ transition involves the thermal desorption of about a double layer of Si. Since this double layer of Si is not very different from a layer of Si on a Si(111) substrate, it is not surprising that this phase transition follows the vapor pressure curve of Si over a Si substrate. On the other hand, the $(\sqrt{3} \times \sqrt{3}) - (6\sqrt{3} \times 6\sqrt{3})$ transition involves the thermal desorption of Si from SiC [5,6], and therefore more closely follows the vapor pressure curve of Si over a SiC substrate. The fact that these transitions follow the bulk vapor pressure data so closely provides a natural explanation for the wide temperature range over which the transitions can be varied.

The ability to shift the phase transitions up by several 100 °C has important consequences for the kinetics of the transitions, as well as the resulting surface morphologies. For example, while the $(3 \times 3) - (1 \times 1)$ transition at the low end of the temperature range occurs on a time scale of minutes, it takes less than a second at the higher end of the temperature scale. This large enhancement in kinetics makes it possible to improve the surface morphology at higher temperatures, in the presence of disilane, and equilibrate towards a smooth surface morphology. Figure 4(a) shows the surface after initial cleaning in disilane, and formation of the $(\sqrt{3} \times \sqrt{3})$ structure. Atomic steps sepa-

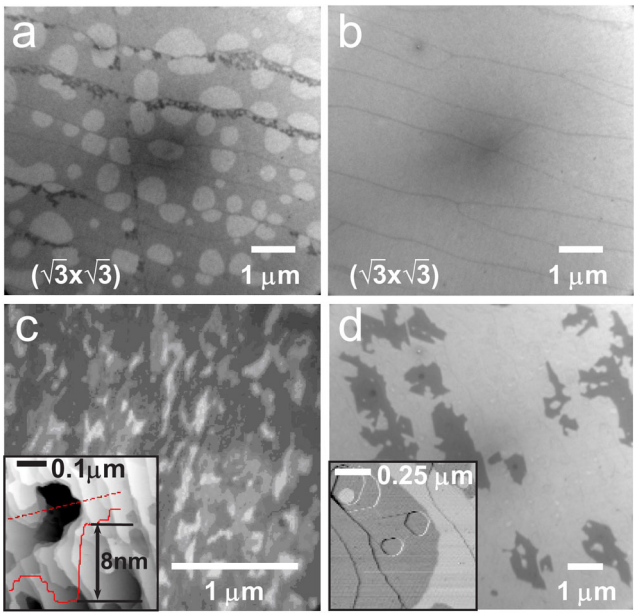

FIG. 4 (color online). (a) $(\sqrt{3} \times \sqrt{3})$ surface after initial formation in a 3×10^{-7} Torr Si background pressure. In addition to atomic steps, many atomic layer high 2D islands are seen on the terraces. After annealing in the same Si background at ~1140 °C, the 2D islands coarsen away, leaving an atomically flat surface with terrace sizes limited only by the sample miscut angle (b). At lower temperatures, and without a Si background pressure, such coarsening is not observed due to limited kinetics. Field of view 7 μm. (c) Graphene layers on SiC obtained by heating to ~1300 °C in the absence of a silicon background pressure. Different grey levels correspond to different graphene layer thicknesses, in the range of 1–4 atomic layers. The feature sizes are small, and there is a broad distribution of layer thicknesses. Field of view 2.8 μm. (d) Graphene layers on SiC obtained by heating in excess of 1300 °C in a disilane background pressure of 2×10^{-5} Torr. Light grey corresponds to 1 atomic layer of graphene, dark grey to 2 atomic layers of graphene. With a field of view of 8.6 μm, it is clear that the graphene flakes are about an order of magnitude larger in lateral size than in (c), and that the thickness distribution is much better controlled, even though the annealing temperature was significantly higher.

rate wide terraces on which we observe additional two-dimensional (2D) ($\sqrt{3} \times \sqrt{3}$) islands also bounded by atomic steps. With further annealing, these 2D islands undergo coarsening and finally disappear, leaving the surface covered with atomically smooth terraces, separated by atomic steps, free of any atomic-scale roughness other than intrinsic miscut steps [Fig. 4(b)]. In the absence of disilane, with the ($\sqrt{3} \times \sqrt{3}$) structure stable only at much lower temperatures, it is impossible to reach such smooth morphologies on reasonable time scales, and the surface always remains much rougher. The same holds for the formation of graphene. We have shown previously how in the absence of a background pressure of disilane, the $6\sqrt{3}$ structure (consisting of a single graphenelike buffer layer covalently bonded to the underlying SiC substrate [5,14]) is very rough, with thermal etchpits as deep as 10–20 nm[6]. Upon the subsequent formation of graphene, this roughness remains. Figure 4(c) shows a 2.8 μm field of view image of graphene formed by heating to ~1300 °C in the absence of a silicon background pressure. The surface is rough, with at least 4 different graphene layer thicknesses exposed. The situation is very different in Fig. 4(d). This sample was first annealed in a disilane background of 8×10^{-7} Torr, crossing the $\sqrt{3}$ to $6\sqrt{3}$ slowly to form large and continuous $6\sqrt{3}$ domains without etchpits. This was followed by an anneal in 2×10^{-5} disilane at temperatures exceeding 1300 °C to form graphene. This image, with a field of view of 8.6 μm, shows much larger feature sizes, and only 2 graphene layer thicknesses exposed, a significant improvement over Fig. 4(c). Thus, the ability to control the different phase transition temperatures by taking advantage of the thermodynamics of these phases and pushing the phase transitions to higher temperatures, allows us to dramatically improve the surface morphology, eliminate thermal pitting, and achieve domain sizes exceeding the sample miscut angle.

In conclusion, we have elucidated the thermodynamics of the various phase transitions on the Si-terminated 4H-SiC(0001) surface, and find that the phase transition temperatures can be varied over a wide temperature range by establishing thermodynamic equilibrium between the SiC sample and the external Si vapor pressure. We find that large, continuous $6\sqrt{3}$ domains, without etchpits, can be formed in near-equilibrium conditions in the presence of a Si background, enabling the subsequent formation of high quality graphene films. Similar results have been obtained on 6H-SiC(0001). We believe that the ability to control the formation temperatures and morphologies of the C-rich phases, including the growth of graphene, is an important advance in establishing practical SiC-based graphene epitaxy required for large-scale graphene device fabrication and integration.

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