Reliable Logic Circuit Elements that Exploit Nonlinearity in the Presence of a Noise Floor

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The response of a noisy nonlinear system to deterministic input signals can be enhanced by cooperative phenomena. We show that when one presents two square waves as input to a two-state system, the response of the system can produce a logical output (NOR/OR) with a probability controlled by the noise intensity. As one increases the noise (for fixed threshold or nonlinearity), the probability of the output reflecting a NOR/OR operation increases to unity and then decreases. Changing the nonlinearity (or the thresholds) of the system changes the output into another logic operation (NAND/AND) whose probability displays analogous behavior. The interplay of nonlinearity and noise can yield logic behavior, and the emergent outcome of such systems is a logic gate. This ''logical stochastic resonance'' is demonstrated via an *experimental* realization of a two-state system with two (adjustable) thresholds.

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Over the last few years, it has become increasingly obvious that understanding how noise and nonlinearity cooperate, in a dynamical system, to produce novel effects is critical in understanding how complex systems behave and evolve. Stochastic resonance (SR) provides one such example wherein the cooperative behavior between noise and dynamics produces interesting, often counterintuitive, physical phenomena. SR has received much attention over the past few decades [1,2] and consists of the enhancement of weak input signals through a delicate interplay between the signal, noise, and nonlinearity (threshold). Here, we investigate the response of a simple threshold detector to input signals, consisting of two random square waves. We find that, in an optimal band of noise, the output is a logical combination of the two input signals: logical stochastic resonance (LSR).

Our motivation stems from an issue that is receiving considerable attention today: as computational devices and platforms continue to shrink in size and increase in speed we are increasingly encountering fundamental noise characteristics that cannot be suppressed or eliminated [3]. Hence, an understanding of the cooperative behavior between a device noise floor and its nonlinearity is bound to play an increasingly crucial, even *essential* role in the design and development of future computational concepts and devices.

Consider a general nonlinear dynamic system, given by $\dot{x} = F(x) + I + D\eta(t)$, where $F(x)$ is a generic nonlinear function giving rise to a potential with two distinct energy wells. I is a low amplitude input signal and $\eta(t)$ is an additive zero-mean Gaussian noise with unit variance, D being the noise strength; the noise is taken to have correlation time smaller than any other time scale in the system, so that it may be represented, theoretically, as delta correlated.

Usually, a logical input-output correspondence is achieved by encoding N inputs in N square waves. Specifically, for two logic inputs, we drive the system with a low amplitude signal I, taken to be the sum of two trains of aperiodic pulses: $I_1 + I_2$, with I_1 and I_2 encoding the two logic inputs. The logic inputs can be either 0 or 1, giving rise to 4 distinct logic input sets (I_1, I_2): (0, 0), (0, 1), (1, 0), and (1, 1). Now the input sets (0, 1) and (1, 0) give rise to the same I, and so the 4 distinct input conditions (I_1, I_2) reduce to 3 distinct values of I. Hence, the input signal I, generated by adding two independent input signals, is a three-level aperiodic waveform.

The *output* of the system is determined by its state; e.g., the output can be considered a logical 1 if it is in one well, and logical 0 if its in the other. Specifically the output corresponding to this 2-input set (I_1, I_2), for a system with potential wells at $x_+ > 0$ and $x_- < 0$, is taken to be 1 (or 0) when the system is in the well at x_+, and 0 (or 1) when the system is in the other well (at x_-). Hence, when the system switches wells, the output is ''toggled.''

Here we will demonstrate that one observes, for a given set of inputs (I_1, I_2), a *logical* output from this nonlinear system, in accordance with the truth tables of the basic

TABLE I. Relationship between the two inputs and the output of the fundamental OR, AND, NOR and NAND logic operations. Note that the four distinct possible input sets (0, 0), (0, 1), (1, 0), and (1, 1) reduce to three conditions as (0, 1) and (1, 0) are symmetric. *Any* logical circuit can be constructed by combining the NOR (or the NAND) gates [4].

Input Set (I_1, I_2)	OR	AND	NOR	NAND
(0, 0)	0	0	1	1
(0, 1)/(1, 0)	1	0	0	1
(1, 1)	1	1	0	0

logic operations shown in Table I. A crucial observation is that this occurs consistently and robustly *only* in an optimal window of noise. For very small or very large noise the system does not yield any consistent logic output, in line with the basic tenets of SR. But in a reasonably wide band of moderate noise, the system produces the desired logical outputs consistently.

We now explicitly demonstrate LSR with a very simple nonlinear system, which we implement with an efficient electronic analog:

$$\dot{x} = -\alpha x + \beta g(x) + D\eta(t) + I_1 + I_2 \qquad (1)$$

with the nonlinear function $g(x)$ given by x [$x_l^* \le x \le x_u^*$, $x_l^*(x < x_l^*)$, and $x_u^*(x > x_u^*)$, where x_u^* and x_l^* are the upper and lower thresholds, respectively [see Fig. 1(a)]. The effective potential generated by the thresholding (see Fig. 1)] is bistable with stable energy states (potential minima) at $x_- = \beta x_l^*/\alpha$ and $x_+ = \beta x_u^*/\alpha$, in the absence of the signal I. Here, instead of manipulating the nonlinearity by varying α and β, we will vary the nonlinearity by simply changing the threshold x_u^* and x_l^* in $g(x)$. This allows the heights and asymmetry of the wells to be manipulated very efficiently (Fig. 1).

With no loss of generality, consider the two (randomly switched) inputs I_1 and I_2 to take value -0.5 when the logic input is 0, and value 0.5 when logic input is 1. Then, the input signal $I = I_1 + I_2$ is a three-level aperiodic square wave form. Figure 2 shows the response of the system (1) for thresholds $(x_u^*, x_l^*) = (1.3, -0.5)$ and 3 choices of noise intensity D. We observe that, under optimal noise [panel 2(b)], interpreting the state $x < 0$ as logic output 0 and the state $x > 0$ as logic output 1 yields a clean (i.e., stable) logical OR whereas interpreting the state $x > 0$ as logic output 0 and the state $x < 0$ as logic output 1 yields a clean logical NOR. In a completely analogous way, by setting the thresholds at $(x_u^*, x_l^*) = (0.5, -1.3)$, we can realize clean AND and NAND gates in almost the same optimal noise intensity regime as the previous case. Note that NAND and NOR are fundamental gates which can, in combination, yield all possible logical responses.

The (experimental) observations above, can be explained in the standard framework of SR in overdamped systems underpinned by double well potentials [1,2]. The different outputs, obtained by driving the state of the system to one or the other well, are realized by appropriately manipulating the heights and asymmetry of the wells. One can, then, readily understand the occurrence of a particular logic output: when inputs I_1 and I_2 are added, the effective position and depth of the wells change, to $x_- = \{\beta x_l^* + I_1 + I_2\}/\alpha$ and $x_+ = \{\beta x_u^* + I_1 + I_2\}/\alpha$. This asymmetry causes the state of the system to switch to the desired well under adequate noise. For $x_u^* > |x_l^*|$ one obtains the NOR logic operation, and for $x_u^* < |x_l^*|$ one obtains the NAND logic operation.

We can quantify the consistency (or reliability) of obtaining a given logic output by calculating the probability of obtaining the desired logic output for different input sets; this probability, P(logic), is the ratio of the number of correct logic outputs to the total number of runs. Each run samples over the four input sets (0, 0), (0, 1), (1, 0), (1, 1), in different permutations. If the logic output, as obtained from $x(t)$, matches the logic output in the truth table for all

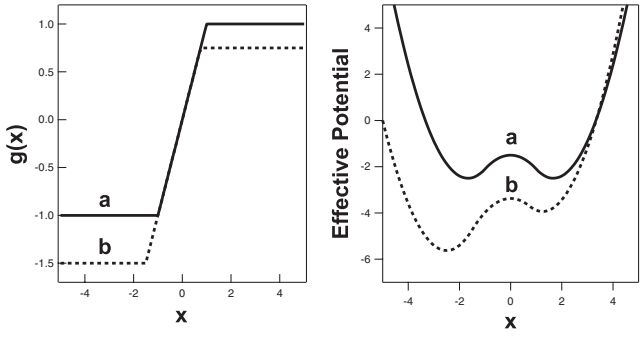

FIG. 1. For the system (1): (left) the piecewise linear function $g(x)$ and (right) the effective potential it gives rise to, with thresholds (a) $x_l^* = -1$, $x_u^* = 1$ (solid line) and (b) $x_l^* = -1.5$, $x_u^* = 0.75$ (dashed line). Equal upper and lower thresholds (i.e., $x_l^* = x_u^*$) give rise to symmetric wells. $I = 0$, $\alpha = 1.8$, $\beta = 3.0$.

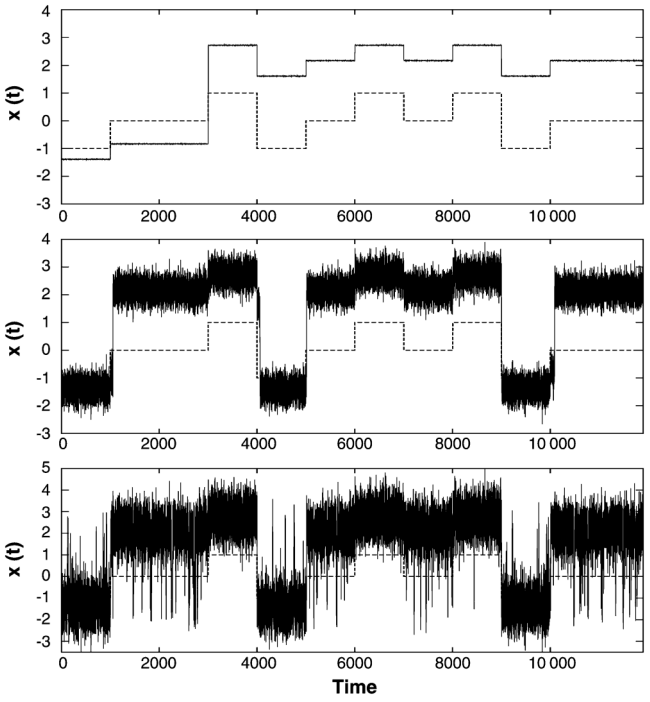

FIG. 2. Response of the system (1), with $\alpha = 1.8$, $\beta = 3.0$, and thresholds set to $(x_u^*, x_l^*) = (1.3, -0.5)$. Each panel has 2 curves. Solid curves represent the solution $x(t)$ from numerical simulations for additive noise intensities D equal to (top to bottom) 0.01, 0.5, and 1. The input I is the sum of randomly switched square pulse trains (see text), and is the same (dashed line) in each panel. For an optimal noise intensity (center panel) a reliable OR/NOR gate is obtained.

four input sets in the run, it is considered a success. When P(logic) is close to 1 the logic operation is obtained very reliably. Figure 3 shows this quantity obtained from extensive numerical simulations; it is evident that the fundamental logic operation NAND (and, analogously, NOR) is realized, consistently, in an optimal band of moderate noise. The remarkable thing here then is that these stable logic operations are only realized (for subthreshold input signals) in the presence of noise. More specifically, in relatively wide windows of moderate noise, the system yields logic operations with near certain probability, i.e., $P(\text{logic}) \sim 1$. We note the occurrence of a flat maximum rather than the usual peak associated with SR [1]. This is due to our choice (a probability) of performance measure. The logic response is almost 100% accurate in a wide window of the noise; in this sense, the gate is quite robust to background fluctuations.

It is clear that (perhaps, somewhat counterintuitively) noise plays a constructive role in obtaining a large, robust, asymmetric response to input signals; i.e., different (and distinct) levels of input pulses yield a 0/1 output, determined by the system being in either one of the two widely separated wells [5]. This kind of response is necessary for logic operations, as it allows one to consistently map different distinct inputs to a binary output. For instance, for NAND logic, two input signals, (0, 0) and $(0, 1)/(1, 0)$, result in the system being in the well at x_+ and one input set (1, 1) results in the system being in well x_-; whereas for NOR logic, two input signals, $(0, 1)/(1, 0)$ and (1, 1), result in the system being in the well at x_- and one input set (0, 0) results in the system being in well x_+. Such mappings can be obtained, in principle, for any multiple-input logic operation by an appropriate choice of parameters.

Further, for a fixed noise level, it is evident (Fig. 4) that different types of logic (NAND vis-a-vis NOR) are obtained in different ranges of thresholds. This is because the thresholds (x_l^*, x_u^*) determine the position, depths and asymmetry of the potential wells (Fig. 1), which in turn dictate the switching dynamics in response to the input stream. Significantly, this implies that one can "morph" between logic responses by simply adjusting a threshold in a suitable window of noise. This has been demonstrated, explicitly, in our electronic analog realization of (1). This is, of course, a desirable characteristic of the dynamics; one typically does not inject noise into the system if the desired behavior can be obtained by varying deterministic parameters (in this case, the thresholds).

The effect of an additional constant input bias C (over a temporal interval much longer than the noise correlation time) has also been studied. As the value of the bias changes (keeping the nonlinearity and noise level fixed), it is observed that the response of the system switches from NOR to NAND logic, or *vice versa*. The important point is that changing C changes the symmetry of the potential wells, and leads to different logical responses. It should be underscored that while the logic responses are switched by changing the nonlinearity or the bias, the desired output is obtained only for *optimal* noise intensities (Fig. 3), without which one would not be able to extract any significant consistent logic response. Figure 5 (obtained experimentally) shows the behavior described in the preceeding paragraphs. In each panel we plot the probability P(logic) vs the external bias C and the noise intensity D. For a given noise intensity (in the optimal range of Fig. 3) this figure shows that adjusting the parameter C will yield the desired logic behavior. The important point here is that the "plateaus" (Fig. 3) overlap for the NOR and NAND performance for the different thresholds (Fig. 4). Hence, for a noise intensity somewhere in the "plateau", we can switch from NOR to NAND (and *vice versa*) operations by simply adjustinging the nonlinearity (i.e., thresholds), or applying a (controlled) dc input signal C.

While in this explicit example we have demonstrated two-input logic; we have also observed multiple-input logic behavior, such as three-input logic, with the input signal being $I = I_1 + I_2 + I_3$ [6]; i.e., the input is an aperiodic train of four-level square pulses. We have also checked the *generality* of the idea over a range of systems, including very simple bistable systems such as a Schmitt Trigger and systems with soft nonlinearities. Further we found that multiplicative noise also yields LSR; the details will be published separately.

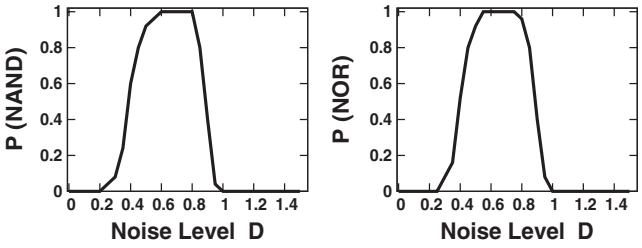

FIG. 3. (left) Probability of obtaining the NAND logic operation (see text), P(NAND), with $(x_l^*, x_u^*) = (-1.3, 0.5)$. A similar result is obtained (right) for P(NOR) taking $(x_l^*, x_u^*) = (-0.5, 1.3)$.

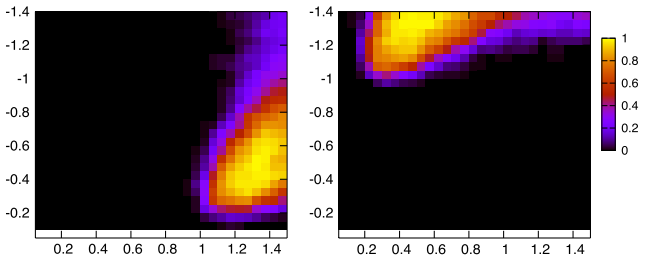

FIG. 4 (color online). Density map of P(logic) (see text) for the (left) NOR and (right) NAND logic operation, for fixed noise ($D = 0.7$), in the space of upper threshold x_u^* (x axis) and lower threshold x_l^* (y axis). The light portion of this plot indicates the nonlinearity [determined by x_u^* and x_l^* in (1) for which a logic output (NOR (left) and NAND (right)] is obtained reliably.

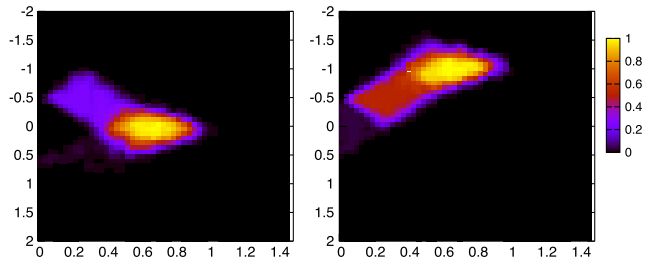

FIG. 5 (color online). $P(\text{NOR})$ (left) and $P(\text{NAND})$ (right) as functions of the noise intensity D (x axis) and asymmetrizing dc input C (y axis). Thresholds are fixed: $(x_l^*, x_u^*) = (-0.5, 1.3)$. Reliable NAND performance accrues for $C \sim -1$; for reliable NOR performance, $C \sim 0$. Optimal performance in both cases is obtained for D values lying within the optimal window (Fig. 3). Note that, for D outside the optimal window, one can still, for any D, optimize NAND/NOR performance by adjusting C as well as the thresholds (x_l^*, x_u^*) (this amounts to an adjustment of the nonlinearity for a given system noise floor).

One can exploit the observations of this paper to design morphing logic gates [7,8]. In addition to implementing a logic gate in the optimal window of noise, the system can also switch the logic response by changing the nonlinear characteristics determining well depth and position. So by adjusting the nonlinearity or bias parameters for a given value of the noise floor, one can obtain different logic gates; making this adjustment can, effectively, manipulate the (nonlinear) transfer characteristic of the system, to optimize the logic response for a given noise floor. This procedure is tantamount to using the nonlinearity as a ''knob'' to tune the system to select different logic truth tables.

In summary, we have shown how the interplay between a noise floor and the (in this case static) nonlinearity can be exploited for the design of key logic-gate structures [9]. Specifically we have shown the direct and flexible implementation of the fundamental logic gates NOR and NAND in an optimal band of noise, from which any universal computing device can be constructed. Further, we have demonstrated the switching of logic functions by using the (adjustable directly, or via a bias signal C) nonlinearity as a ''logic response controller.'' In effect, we are able to obtain the most basic ingredients of general purpose hardware that has potential for reconfigurability. Note that a very simple form of nonlinearity [underpinned by the dynamics (1) and the thresholds] was deliberately chosen in this work because of its ease of realization in an experimental circuit; more general potential systems have been considered but are outside the scope of this letter. Our work also raises the intriguing possibility that LSR could be exploited in nontraditional computing systems, even in the quantum realm [10].

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[5] In marked contrast to the enhanced response of a stochastic nonlinear system to low amplitude input pulses, noisy or noise-free linear systems *cannot amplify the output*; nor can linear systems yield the *strongly asymmetric* response to equispaced input levels necessary to map different input sets to a binary logic output. Further, noise has the effect of simply degrading performance in linear systems, completely unlike the nontrivial effect of noise here.
[6] Multiple-input logic gates are preferred mainly for reasons of space in circuits and, further, many combinational and sequential logic operations can be realized with these logic gates, in which one can minimize the propagation delay. Such multiple-input gates are more power efficient, and have better performance in a wide range of applications.
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