Direct Mapping of Strain in a Strained Silicon Transistor by High-Resolution Electron Microscopy

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Aberration-corrected high-resolution transmission electron microscopy (HRTEM) is used to measure strain in a strained-silicon metal-oxide-semiconductor field-effect transistor. Strain components parallel and perpendicular to the gate are determined directly from the HRTEM image by geometric phase analysis. $Si_{80}Ge_{20}$ source and drain stressors lead to uniaxial compressive strain in the Si channel, reaching a maximum value of -1.3% just below the gate oxide, equivalent to 2.2 GPa. Strain maps obtained by linear elasticity theory, modeled with the finite-element method, agree with the experimental results to within 0.1%.

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Introduction.—Strained silicon is now an integral design feature of the latest generation of micro- and nanoelectronic devices [1]. Strain dramatically increases the mobility of carriers, either electrons ($\times 2$ for strained Si) or holes ($\times 10$ for strained Ge) [2], leading to significantly enhanced performances in metal-oxide-semiconductor field-effect transistors (MOSFETs) [3]. Strain is expected to play a significant role in future devices based on nanowires [4] or in optoelectronic components [5]. Different techniques have been investigated to engineer strain in devices, such as the selective epitaxial growth of $Si_{1-x}Ge_x$ in recessed source and drain regions which produces uniaxial compressive stress in the Si channel of very short gate length p type MOSFETs [6]. The many processing routes and sample geometry produce different strain distributions. Performance gains can be understood and modeled only by knowing the exact strain distribution in two dimensions. Measuring strain in the active area of devices has therefore been a major characterization goal over the past few years but has proved difficult to achieve in practice [1,7].

Transmission electron microscopy (TEM) is the only viable tool for measuring strains in devices at the nanoscale, the most common techniques being based on electron diffraction [7]: convergent-beam electron diffraction (CBED) [8–10], nanobeam diffraction [11], or electron diffraction contrast analysis [12]. While CBED is highly successful for measuring small strains (of the order of 10^{-4}), difficulties are encountered when analyzing highly strained regions such as those found typically in the channel region of MOSFETs [13]. Lines are split because of lattice planes bending in the thin electron-transparent foils [14]. Measurements can still be carried out but require detailed comparisons with simulations based on finite-element modeling of the entire system [15]. We have therefore sought a more direct measurement technique that is capable of mapping strain distributions continuously across devices.

High-resolution transmission electron microscopy (HRTEM) is a powerful technique for measuring strains at the nanoscale [16]. Images are recorded of the crystalline lattice and can be analyzed using the peak-finding technique [17], geometric phase analysis (GPA) [18], or diffractogram analysis [19]. The technique has been used to measure strains in a range of semiconductor systems [20–23], including Si/SiGe heterostructures [24–26]. Nonetheless, there are two major drawbacks to using HRTEM for strain mapping in transistors: thin-film relaxation and precision. The first is the well-known problem that thinning a specimen to electron transparency introduces two free surfaces which allow strain to relax. Strain measured in a thin TEM foil is therefore modified with respect to the bulk sample. The second drawback is that an internal reference is required since measurements are carried out by comparing the distortion of the crystalline lattice with respect to an unstrained area of crystal. Measuring strain relative to areas recorded in different images is therefore difficult.

We propose to overcome these difficulties by carrying out measurements using aberration-corrected HRTEM [27] and recording the whole transistor on one image using a large-area CCD camera at relatively low magnification. The higher signal-to-noise of aberration-corrected images [25] allows us to carry out experiments on samples prepared by focused-ion beam (FIB) which are thicker than samples conventionally prepared for HRTEM imaging. The thickness is uniform and can be precisely measured by CBED. Recording images of the whole transistor allows us to define the reference crystal in a relatively unstrained region and compare even very small strain variations across the whole field of view. For this to be successful, we have developed a protocol that enables us to calibrate the geometrical distortions from the optical system, including the detector [28].

Experimental details.—A series of dummy transistors with a channel width of 50 nm were prepared at IMEC

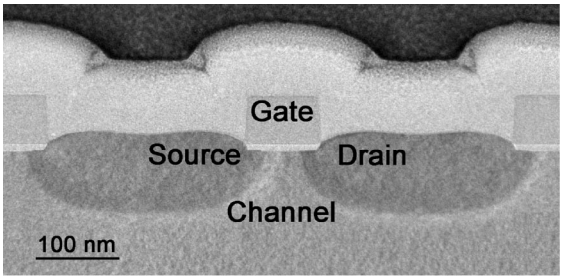

FIG. 1. Bright-field TEM image showing the SiGe recessed sources and drains on each side of the dummy gate stacks.

using $Si_{80}Ge_{20}$ sources and drains (grown in an ASM Epsilon 2000 reactor) to apply uniaxial compressive stresses to the Si channel. TEM samples were prepared by FIB for $[1\bar{1}0]$ zone axis observations (Fig. 1). Different geometries were investigated in order to minimize sample bowing and cracking. The optimized method maintains a relatively thick substrate region adjacent to the thinned outer edge. A significant improvement in the rigidity of the resulting structure is thus obtained, though a relatively thick amorphous layer is created on both sides of the specimen.

Microscope observations were performed on the SACTEM-Toulouse, a Tecnai F20 (FEI) transmission electron microscope operating at 200 kV which is equipped with a field-emission gun and an imaging aberration corrector (CEOS). Images were recorded on a 2k by 2k pixel CCD camera (Gatan USC1000). The specimen was oriented along to the $[1\bar{1}0]$ zone axis and images taken at a nominal magnification of 145 000 in order to image the whole active region of the transistor. Numerical images have a low sampling density of 0.063 nm/pixel which corresponds to only 5 pixels per (111) lattice fringe. Strain mapping was performed using *GPA Phase* software (HREM Research Inc.) a plug-in for the image processing package *DigitalMicrograph* (Gatan). The (111) lattice fringes were analyzed using a Fourier-space mask of 0.25 nm^{-1} which is necessary to reduce noise but limits the spatial resolution of strain measurements to 4 nm. Strain modeling was carried out using the COMSOL Multiphysics (COMSOL) software package.

Results.—Figure 2(a) shows an HRTEM image of the transistor. The x axis is defined to be parallel to the [110] direction and the z axis the [001] growth direction. The contrast is poor [see Fig. 2(b)] compared with that which can be obtained using this microscope [25] because of the particular constraints linked to this experiment. The specimen is 85 ± 5 nm thick (measured by CBED) and the amorphous surface layers from the FIB preparation obscure the crystalline lattice. Finally, the images were obtained at low magnification. The periodicities analyzed are damped due the modulation transfer function (MTF) of the CCD camera [29]. Nevertheless, the HRTEM images have all the necessary qualities for strain analysis, namely, uniform contrast across the whole field of view with little

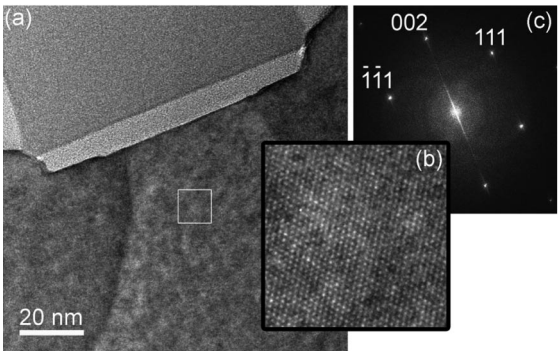

FIG. 2. High-resolution electron microscopy of transistors: (a) HRTEM image of a transistor with pseudomorphic $Si_{80}Ge_{20}$ stressors in the source and drain, revealed by the darker contrast; (b) enlargement of square region to show lattice fringes; (c) Fourier transform showing (111) and (002) lattice periodicities.

sample bending [30]. This is the major advantage of preparing samples by FIB.

The 2-dimensional map of the local deformation ε_{xx} obtained from the analysis of the HRTEM image is shown in Fig. 3. The reference region of crystal was taken in the silicon at a distance of 120 nm from the channel region. The source and drain made of $Si_{80}Ge_{20}$ have a larger lattice parameter than the silicon substrate and therefore appear with positive deformation values. The channel region is revealed to be compressed in the x direction, with a maximum just below the gate and decreasing progressively towards the substrate. With such maps, the strain components can be extracted in different ways, either as profiles or point to point. The precision, estimated from the standard deviation of the random fluctuations in the substrate, is 0.3%. However, measured values are affected by thin-film relaxation. We therefore need to carry out modeling to evaluate and apply corrections if needed.

Modeling.—We calculate the local strain within the framework of linear elasticity theory by the finite-element

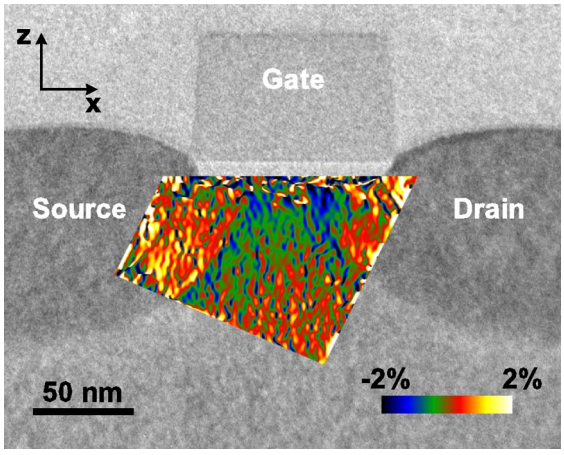

FIG. 3 (color online). Strain component parallel to the gate ε_{xx} obtained by GPA of the HRTEM image (Fig. 2) superimposed on the bright-field image (Fig. 1).

method (FEM) [31]. We simulate in 3D an 80 nm thick specimen with $Si_{80}Ge_{20}$ sources and drains. The geometry of the model mimics the actual geometry revealed by TEM (Fig. 1). The top surfaces of the foil were considered to be free. No account was taken of the gate oxide. We also simulated the bulk sample (assuming plane strain conditions) to assess the extent of thin-film relaxation.

The HRTEM image is a projection of the 3D specimen. We have thus assumed that for small strains, the measured strains correspond to the strain averaged over the electron path. This approximation is accurate for uniformly strained layers [26]. Experimental and simulated results for the expansion/contraction and shear components of the strain are shown in Fig. 4, with identical color scales. In fact, a larger area was modeled. The simulated strain maps are, according to our assumption, integrated over the thickness of the specimen. Specific features such as the highly compressed region near the gate (ε_{xx}), the corresponding region in expansion in the perpendicular direction (ε_{zz}), and the positive and negative shear components (ε_{xz}) localized at the interface between $Si_{80}Ge_{20}$ and the Si channel are well reproduced theoretically. We have extracted profiles across the transistor from source to drain to show the quantitative agreement (Fig. 4). These profiles are integrated over windows of 20 nm in z in order to reduce noise. Experimental and simulated profiles are in quantitative agreement. The channel is in a compression state in x ($\varepsilon_{xx} = -1\%$) whereas the source and drain regions are in tension in z direction ($\varepsilon_{zz} = +1\%$).

Because of the impact on hole mobility of compressive strains in the channel region, we analyze the ε_{xx} component in detail. Figure 5 shows the variation of this component from gate to substrate. The values are averaged parallel to the gate across the width of the channel. The experimental curve was obtained by averaging four experimental curves from four different but nominally identical transistors. Experimental values are in agreement provided that a 0.1% deviation is factored in, which is our precision estimation. Figure 5 also shows two FEM simulations, one including thin-foil relaxation and the other without, corresponding to the bulk sample. Notice that there is no significant difference between the results from the two simulations, except in the first tens of nanometers below the gate where the relaxation reduces the compression by 0.12%.

Discussion and conclusion.—The Si channel of very short gate length MOSFETs with recessed $Si_{0.8}Ge_{0.2}$ sources and drains is in a uniform lateral compression that decreases with increasing z and has a maximum ε_{xx} of $-1.3 \pm 0.1\%$ near the gate oxide (after correction for thin-film relaxation). Our modeling shows that this component is relatively insensitive to thin-film relaxation, in contrast to the ε_{zz} component which is significantly modified. As we measure these two components independently, this is not so much of a problem. More importantly, the hole mobility is controlled by the in-plane compression ε_{xx}, the less affected component of the strain. In this respect, it is essential to be able to measure strain in the region directly below the gate where the majority of current flows. Converting the strain values into stress gives an in-plane compression of 2.0 ± 0.2 GPa in the first 10 nm below the gate, which should increase hole mobility by about a factor of 4 [6].

The combination of GPA and HRTEM has a number of advantages over CBED analysis of strained silicon devices. In particular, strain can be measured in critical regions

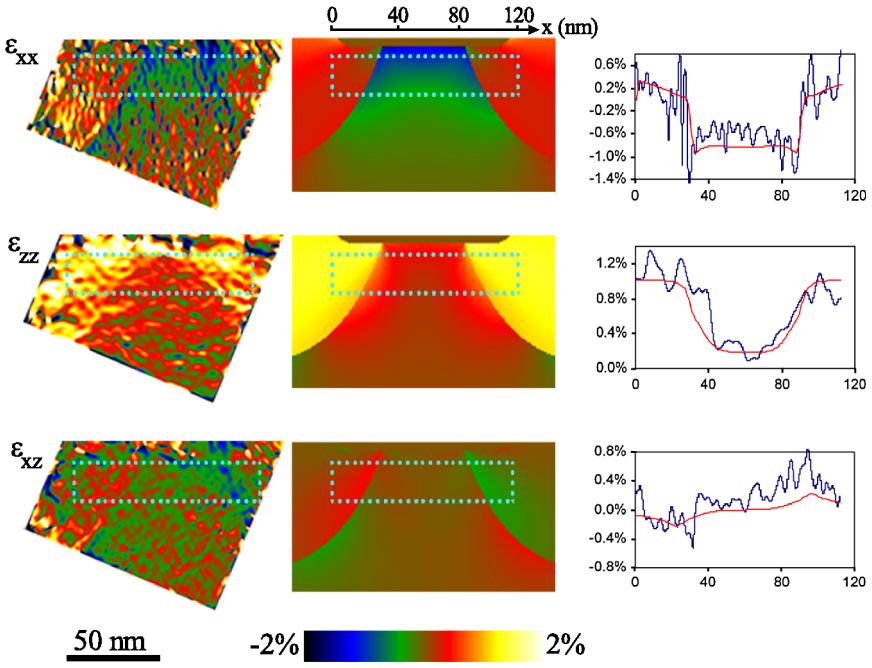

FIG. 4 (color online). Comparison of experimental (left) and modeled (middle) maps of strain components. Profiles (right) compare experimental and simulated strain 30 nm below the gate.

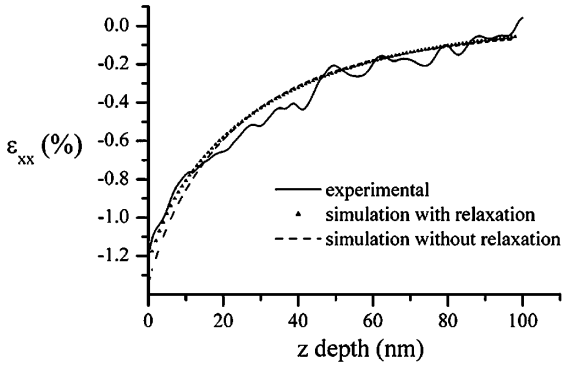

FIG. 5. Comparison between experimental and simulated ε_{xx} from the gate to the substrate: simulation including thin-foil relaxation (triangular dots), 3D simulation without relaxation (dashed line), experimental curve (continuous line).

where strain gradients are large. HRTEM contrast is not directly affected by column bending. Most importantly perhaps, HRTEM provides maps of strain across the whole field of view rather than at isolated points.

Our results show that the strain distribution in the active area of a transistor can be measured to an accuracy of 0.1% with a spatial resolution of about 4 nm when averaged over the width of the channel. Different strategies can be applied to diminish the amorphous layer from FIB thinning, which is the main accuracy limitation. Smaller structures will also be easier to analyze, and the use of even larger CCD cameras will improve contrast and ease. This opens up the possibility of detailed comparisons between modeling and device design with the aim to engineer and control strain for increased device performances.

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[1] *International Technology Roadmap for Semiconductors* (SEMATECH, Austin, 2005).
[2] M. L. Lee, E. A. Fitzgerald, M. T. Bulsara, M. T. Currie, and A. J. Lochtefeld, Appl. Phys. **97**, 011101 (2005).
[3] D. A. Antoniadis, I. Aberg, C. Ni Chleirigh, O. M. Nayfeh, A. Khakifirooz, and J. L. Hoyt, IBM J. Res. Dev. **50**, 363 (2006).
[4] R. R. He and P. D. Yang, Nature Nanotechnology **1**, 42 (2006).
[5] R. S. Jacobsen, K. N. Andersen, and P. I. Borel, J. Fage-Pedersen, L. H. Frandsen, O. Hansen, M. Kristensen, A. V. Lavrinenko, G. Moulin, H. Ou, C. Peucheret, B. Zsigri, and A. Bjarklev, Nature (London) **441**, 199 (2006).
[6] S. E. Thompson, G. Y. Sun, Y. S. Choi, and T. Nishida, IEEE Trans. Electron Devices **53**, 1010 (2006).
[7] B. Foran, M. H. Clark, and G. Lian, *Future Fab International* (Mazik Media Inc., San Francisco, 2006), Vol. 20, p. 127.
[8] J. Huang, M. J. Kim, P. R. Chidambaram, R. B. Irwin, P. J. Jones, J. W. Weijtmans, E. M. Koontz, Y. G. Wang, S. Tang, and R. Wise, Appl. Phys. Lett. **89**, 063114 (2006).
[9] P. Zhang, A. A. Istratov, E. R. Weber, C. Kisielowski, H. F. He, C. Nelson, and J. C. H. Spence, Appl. Phys. Lett. **89**, 161907 (2006).
[10] W. Zhao, G. Duscher, G. Rozgonyi, M. A. Zikry, S. Chopra, and M. C. Ozturk, Appl. Phys. Lett. **90**, 191907 (2007).
[11] K. Usuda, T. Numata, T. Irisawa, N. Hirashita, and S. Takagi, Mater. Sci. Eng. B **124**, 143 (2005).
[12] J. Li, D. Anjum, R. Hull, G. Xia, and J. L. Hoyt, Appl. Phys. Lett. **87**, 222111 (2005).
[13] L. Clément, R. Pantel, L. F. T. Kwakman, and J. L. Rouvière, Appl. Phys. Lett. **85**, 651 (2004).
[14] F. Houdellier, C. Roucau, L. Clément, J. L. Rouvière, and M. J. Casanove, Ultramicroscopy **106**, 951 (2006).
[15] A. Spessot, S. Frabboni, R. Balboni, and A. Armigliato, J. Microsc. **226**, 140 (2007).
[16] M. J. Hÿtch, J. L. Putaux, and J. M. Pénisson, Nature (London) **423**, 270 (2003).
[17] R. Bierwolf, M. Hohenstein, F. Phillipp, O. Brandt, G. E. Crook, and K. Ploog, Ultramicroscopy **49**, 273 (1993).
[18] M. J. Hÿtch, E. Snoeck, and R. Kilaas, Ultramicroscopy **74**, 131 (1998).
[19] K. W. Ang, K. J. Chui, V. Bliznetsov, C. H. Tung, A. Du, N. Balasubramanian, G. Samudra, M. F. Li, and Y. C. Yeo, Appl. Phys. Lett. **86**, 093102 (2005).
[20] E. Sarigiannidou, E. Monroy, B. Daudin, and J. L. Rouvière, Appl. Phys. Lett. **87**, 203112 (2005).
[21] T. P. Bartel, P. Specht, J. C. Ho, and C. Kisielowski Philos. Mag. **87**, 1983 (2007).
[22] K. Tillmann, L. Houben, and A. Thust, Philos. Mag. **86**, 4589 (2006).
[23] S. Kret, P. Ruterana, A. Rosenauer, and D. Gerthsen, Phys. Status Solidi (b) **227**, 247 (2001).
[24] N. Cherkashin, M. J. Hÿtch, E. Snoeck, A. Claverie, J. M. Hartmann, and Y. Bogumilowicz, Mater. Sci. Eng. B **124–125**, 118 (2005).
[25] M. J. Hÿtch and F. Houdellier, Microelectron. Eng. **84**, 460 (2007).
[26] F. Hüe, M. J. Hÿtch, J. M. Hartmann, Y. Bogumilowicz, and A. Claverie, Intitute of Physics Conference Series (to be published).
[27] M. Haider, S. Uhlemann, E. Schwan, H. Rose, B. Kabius, and K. Urban, Nature (London) **392**, 768 (1998).
[28] F. Hüe, C. L. Johnson, S. Lartigue-Korinek, G. Wang, P. R. Buseck, and M. J. Hÿtch, J. Electron Microsc. **54**, 181 (2005).
[29] R. R. Meyer, A. I. Kirkland, R. E. Dunin-Borkowski, and J. L. Hutchison, Ultramicroscopy **85**, 9 (2000).
[30] M. J. Hÿtch and T. Plamann, Ultramicroscopy **87**, 199 (2001).
[31] Y. C. Yeo and J. S. Sun, Appl. Phys. Lett. **86**, 023103 (2005).