

Memory states in small arrays of Josephson junctions

Y. Braiman,^{1,2} B. Neschke,^{1,2,*} N. Nair,^{1,2} N. Imam,³ and R. Glowinski⁴

¹*Computer Science and Mathematics Division, Computing and Computational Science Directorate, Oak Ridge National Laboratory, Oak Ridge, Tennessee 37831, USA*

²*Department of Mechanical, Aerospace, and Biomedical Engineering, University of Tennessee, Knoxville, Tennessee 37996, USA*

³*Computing and Computational Science Directorate, Oak Ridge National Laboratory, Oak Ridge, Tennessee 37831, USA*

⁴*Department of Mathematics, Houston University, Houston, Texas 77204, USA*

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We study memory states of a circuit consisting of a small inductively coupled Josephson junction array and introduce basic (write, read, and reset) memory operations logics of the circuit. The presented memory operation paradigm is fundamentally different from conventional single quantum flux operation logics. We calculate stability diagrams of the zero-voltage states and outline memory states of the circuit. We also calculate access times and access energies for basic memory operations.

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I. INTRODUCTION

As conventional computing systems grow to very large systems (such as exascale computers) it is becoming increasingly important to reduce power consumption, reduce size, and increase the speed of a single computing operation. Such desire to study how to improve computing schemes has led to some very interesting ideas of processor design based on quantum computing [1], biological computing [2], and nonlinear dynamics based chaotic computing [3].

One of the main challenges in modern computing systems is developing fast, small size, and energy efficient memory. As the requirements for memory grow immensely in modern times, so does the total cost to operate memory in exascale and other types of computing. One possible way to speed up memory access while reducing power consumption is cryogenic computing [4]. Cryogenic electronics based on superconducting devices (such as Josephson junctions and superconducting quantum interference devices) are generically very fast and energy efficient [5]. A single Josephson junction can operate at a speed close to THz and switching between the states may require as little as 10^{-18} – 10^{-19} J (0.1–1 aJ).

Cryogenic memory plays an important role in the development of superconducting-based computing. A variety of designs have been proposed, including memories based on single flux quantum digital logic [6], hybrid superconducting complementary metal-oxide semiconductor designs [7,8], magnetic random access memory (RAM) [9], and others [10]. Some of the main challenges in developing superconducting memory are reducing power dissipation, increasing access speed, and reducing the size of the chip [10].

Superconducting single flux quantum digital logic circuits show promise to significantly advance performance in a variety of applications including computer CPUs, memories, digital radio frequency receivers, and others [4]. The energy efficiency of single flux quanta (SFQ) circuitry has significantly increased

in recent years [10,11]. However, designing RAM still poses significant challenges and the slow development of cryogenic memory is one of the major bottlenecks for advancement in cryogenic supercomputing. While SFQ technology provides seemingly satisfactory solutions for cryogenic processing, only 4096 bits of memory have been demonstrated so far [6]. Moreover, when projected to a 1 PB memory, the power dissipation nears 85 MW, which is unacceptable [10].

In this paper we introduce a very simple memory paradigm based on the existence of multiple stable states present in a large variety of nonlinear systems. This paradigm is fundamentally different from a conventional paradigm that employs SFQ for memory operation. While we specifically address cryogenic memory based on small coupled arrays of Josephson junctions, the proposed paradigm may be more generic and applicable to systems other than cryogenic memory. Since we use junctions coupled through inductors, the stored energy in the circuit array can no longer be perfectly quantized. The equations of motion describing the dynamics of Josephson junctions in the framework of the resistively shunted junction (RSJ) model resemble the equations for physical pendulums with sinusoidal nonlinearity terms. Consequently, there are many systems that possess a similar type of nonlinearity [12]. In the proposed paradigm read, write, and reset operations can be executed on the same circuit. Such systems may be highly tolerant to noise and disorder. In the absence of memory operations, the average voltage of each junction is zero, thus energy will dissipate only at the time of memory access operations. Both memory access times and energies can be minimal if the parameter set is chosen properly. The number of junctions and coupling design may vary, however it is desirable to operate a small array (two to three junctions) to reduce the size of the system.

As an example, we present the principles of operation of a circuit consisting of three inductively coupled Josephson junctions. In our design, an inductively coupled array of three Josephson junctions operates at cryogenic temperatures and is compact, fast, and energy efficient. Write, read, and reset operations are applied to the same circuit. Pulse energies required for implementation of the memory operations may be very low [in the range of 10^{-19} J (0.1 aJ)] and response

*Present address: Raytheon Missile Systems, Tucson, AZ 85730, USA.

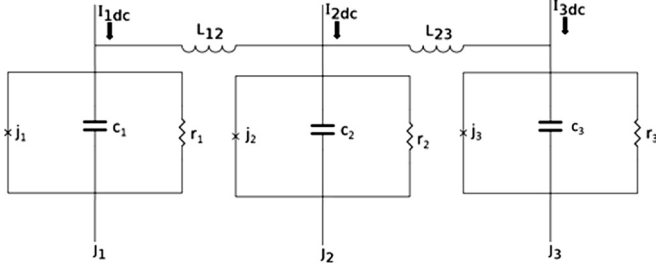


FIG. 1. Schematic circuit diagram of three coupled RSJ Josephson junctions.

times, measured from the application of the pulse to the circuit response, may be lower than 100 ps.

II. MEMORY CIRCUIT DESIGN

Our proposed memory circuit incorporates an inductively coupled array of three Josephson junctions with free-end boundary conditions. Figure 1 shows a schematic design of the proposed circuit.

The following relations in Eq. (1) define the current $I_{c,k}$ and the voltage V_k . The equation modeling an uncoupled RSJ circuit is provided by Eq. (2). This assumes operation in a cryogenic environment:

$$I_J = I_c \sin \phi, \quad V = \frac{\hbar}{2e} \frac{d\phi}{dt}, \quad (1)$$

$$C \frac{dV}{dt} + \frac{1}{R} V + I_J = I_{\text{ext}}. \quad (2)$$

Here I_J is the Josephson (superconducting) current in the junction, V is the voltage in the junction, C is the junction capacitance, R is the junction resistance, I_c is the junction critical current, I_{ext} is the external driving current, e is the electric charge, and \hbar is Planck's constant. Phase difference between the two parts of superconductors forming the junction is denoted by ϕ . By combining Eqs. (1) and (2) we obtain the equation for the phase ϕ ,

$$\frac{\hbar C}{2e} \frac{d^2\phi}{dt^2} + \frac{\hbar}{2eR} \frac{d\phi}{dt} + I_c \sin \phi = I_{\text{ext}}. \quad (3)$$

The dimensionless equation for a single junction (5) is realized with the parameters defined in Eq. (4),

$$\omega_J^2 = \frac{2e I_c}{\hbar C}, \quad \tau = \omega_J t, \quad \frac{I_{\text{ext}}}{I_c} = i, \quad (4)$$

$$\gamma = \sqrt{\frac{\hbar C}{2e I_c}} \frac{1}{RC} = (\omega_J RC)^{-1}, \quad (4)$$

$$\frac{d^2\phi}{d\tau^2} + \gamma \frac{d\phi}{d\tau} + \sin \phi = i. \quad (5)$$

We used the values of $\gamma = 0.7$ for the first and third junctions and $\gamma = 1.1$ for the middle second junction. Since $\gamma = 1/\sqrt{\beta_c}$, the value of $\gamma = 0.7$ corresponds to the values of $\beta_c \approx 1.2$ [a different way of writing Eq. (5) would be $\beta_c \frac{d^2\phi}{d\tau^2} + \frac{d\phi}{d\tau} + \sin \phi = i$], which corresponds to an approximately 670–770 nm feature size junction with a critical current density

of $J_c \approx 50 \text{ kA/cm}^2$ [13]. This critical current density implies that the critical current $I_c = A_J J_c$ ($A_J = \frac{\pi}{4} d^2$) can range approximately from 175 to 400 μA for feature size ranging from 670 to $O(1000)$ nm. For lower critical current processes (10 and 20 kA/cm^2) values of the critical current will be lower.

The dimensionless equations for an inductively coupled circuit consisting of three inductively coupled Josephson junctions are provided by

$$\begin{aligned} \frac{d^2\phi_1}{d\tau^2} + \gamma_1 \frac{d\phi_1}{d\tau} + \sin \phi_1 &= i_1 + \kappa_1(\phi_2 - \phi_1), \\ \frac{d^2\phi_2}{d\tau^2} + \gamma_2 \frac{d\phi_2}{d\tau} + \sin \phi_2 &= i_2 + \kappa_1(\phi_1 - \phi_2) + \kappa_2(\phi_3 - \phi_2), \\ \frac{d^2\phi_3}{d\tau^2} + \gamma_3 \frac{d\phi_3}{d\tau} + \sin \phi_3 &= i_3 + \kappa_2(\phi_2 - \phi_3). \end{aligned} \quad (6)$$

Here $\kappa = \frac{\Phi_0}{2\pi L I_c}$, $\Phi_0 = \frac{h}{2e}$ is the magnetic flux quantum, and L is the inductance of the inductor that couples Josephson junctions. The applied current to the junctions includes a dc component and a pulse applied at a certain time for a certain duration,

$$i_k(\tau) = i_{\text{dc},k} + \frac{i_{\text{pulse},k}}{\sqrt{2\pi\sigma_k^2}} e^{-(\tau-\tau_k)^2/2\sigma_k^2}. \quad (7)$$

The value of the inductance is related to the value of the coupling constant κ according to $L = \frac{L_{J_0}}{\kappa}$, where $L_{J_0} = \frac{\hbar}{2eI_c} = \frac{\Phi_0}{2\pi I_c}$ and will be in the range of $0.83 < L_{J_0} < 1.9$ pH for $175 < I_c < 400 \mu\text{A}$. For $\kappa = 0.1$, the characteristic value of the inductance L will be approximately $8.3 < L < 19$ pH.

As we discussed the feature size for a Josephson junction, we would like to briefly discuss the size of the inductor. To estimate the area of the inductor we can employ an approach offered in Ref. [14]. Following Ref. [14], for state-of-the-art inductor fabrication we can calculate the area of the inductor as $A_L = \frac{l}{\gamma}(\omega + s)$, where L is the inductance, l is the typical stripline inductance (approximately equal to 0.6 pH/ μm), ω is the inductor linewidth (approximately 0.35 μm), and s is the spacing between the inductors (approximately 0.5 μm). Consequently, the area for the inductor will be $12.2 < A_L < 27 \mu\text{m}^2$ for $8.3 < L < 19$ pH. For practical applications it is very important that area of the memory cell will be small, therefore reduction of the inductor size is important. Consequently, reduction of the inductor area can be achieved by increasing the value of the coupling constant κ . We have confirmed that a similar memory cell logics can be implemented also for larger values of the coupling constant, for example, $\kappa = 0.5$. For $\kappa = 0.5$, the values of the inductances will be $1.6 < L < 3.8$ pH for $175 < I_c < 400 \mu\text{A}$ and, consequently, the area of the inductor will be in the range of $2.4 < A_L < 5.4 \mu\text{m}^2$. Additional reduction of the inductor area may be achieved by further increasing the value of the coupling constant κ .

In this section we introduce the Josephson junction array memory states. We will start with the derivation of the potential energy of the entire system. The equation for the potential energy of the system V can be obtained by integrating the right-hand sides of Eqs. (6) with respect to the phases and including the potential energy due to linear inductive coupling between junctions. The function is defined to be zero when all

of the phases and their derivatives are zero:

$$V(\phi_1, \phi_2, \phi_3) = \frac{1}{2}\kappa_1(\phi_2 - \phi_1)^2 + \frac{1}{2}\kappa_2(\phi_3 - \phi_2)^2 + 3 + \sum_k (-\phi_k i_k - \cos \phi_k). \quad (8)$$

Equation (9) shows the derivative of the potential energy function with respect to the three junction phases. A junction phase increase will coincide with the storage or release of energy in the inductors. An inductor stores no energy when the phases of the two adjacent junctions are equal. In addition, to increase the phases against the direction of the external currents, work has to be performed. The applied current pulses are omitted for now to investigate the steady states of the system. In equilibrium, each junction's phase resides in a local potential minimum and each of the phase derivatives is equal to zero:

$$\begin{aligned} \frac{\partial V}{\partial \phi_1}(\phi_1, \phi_2, \phi_3) &= \kappa_1 \phi_1 - \kappa_1 \phi_2 - i_{dc,1} + \sin \phi_1, \\ \frac{\partial V}{\partial \phi_2}(\phi_1, \phi_2, \phi_3) &= \kappa_1 \phi_2 - \kappa_1 \phi_1 + \kappa_2 \phi_2 - \kappa_2 \phi_3 - i_{dc,2} + \sin \phi_2, \\ \frac{\partial V}{\partial \phi_3}(\phi_1, \phi_2, \phi_3) &= \kappa_2 \phi_3 - \kappa_2 \phi_2 - i_{dc,3} + \sin \phi_3. \end{aligned} \quad (9)$$

The coupling terms in Eq. (8) are the lowest when the phases are relatively close to each other.

Equilibrium junction phases (junction voltages are equal to zero) can be defined by their offsets θ_k from the negative cosine function's minima, as shown in Eq. (10). When adjacent phase differences and external currents are relatively small, the coupling terms will not contribute as much to the potential energy and the phases will have small offsets. The small-angle approximation in (11) can then hold:

$$\phi_k = 2\pi n_k + \theta_k, \quad (10)$$

$$|n_k - n_{k+1}| < 3 \Rightarrow |\theta_k| \leq \frac{\pi}{6} \Rightarrow \sin \phi_k \approx \theta_k. \quad (11)$$

Applying this relation to Eq. (9) and setting the derivatives to zero yields the linearized set of equations, whose solutions θ_k^* estimate the true equilibrium offsets θ_k . Therefore, as long as the phases ϕ_k are near the values of $2\pi n_k$ while system is

in equilibrium, their set of offsets θ_k is approximated by the matrix equation in (13):

$$\begin{aligned} 0 &= \kappa_1(\theta_1^* + 2\pi n_1) - \kappa_1(\theta_2^* + 2\pi n_2) - i_{dc,1} + \theta_1^*, \\ 0 &= \kappa_1(\theta_2^* + 2\pi n_2) - \kappa_1(\theta_1^* + 2\pi n_1) + \kappa_2(\theta_2^* + 2\pi n_2) \\ &\quad - \kappa_2(\theta_3^* + 2\pi n_3) - i_{dc,2} + \theta_2^*, \\ 0 &= \kappa_2(\theta_3^* + 2\pi n_3) - \kappa_2(\theta_2^* + 2\pi n_2) - i_{dc,3} + \theta_3^*, \end{aligned} \quad (12)$$

$$\begin{aligned} \begin{bmatrix} \theta_1^* \\ \theta_2^* \\ \theta_3^* \end{bmatrix} &= \begin{bmatrix} \kappa_1 + 1 & -\kappa_1 & 0 \\ -\kappa_1 & \kappa_1 + \kappa_2 + 1 & -\kappa_2 \\ 0 & -\kappa_2 & \kappa_2 + 1 \end{bmatrix}^{-1} \\ &\quad \times \begin{bmatrix} i_{dc,1} - 2\pi\kappa_1(n_1 - n_2) \\ i_{dc,2} - 2\pi\kappa_1(n_2 - n_1) - 2\pi\kappa_2(n_2 - n_3) \\ i_{dc,3} - 2\pi\kappa_2(n_3 - n_2) \end{bmatrix}. \end{aligned} \quad (13)$$

For the sake of simplicity, in this paper we consider the case of equal coupling values $\kappa_1 = \kappa_2 = \kappa$ and opposite currents applied to the junctions on the ends $i_{dc,1} = -i_{dc,3}$. Equation (14) shows the solutions of Eq. (13) given the constraints on the parameters and the definitions $d_{12} = n_1 - n_2$, $d_{23} = n_2 - n_3$,

$$\begin{aligned} \theta_1^* &= \frac{1}{\kappa + 1} i_{dc,1} + \frac{\kappa}{3\kappa + 1} i_{dc,2} + \frac{-2\pi\kappa(2\kappa + 1)}{3\kappa^2 + 4\kappa + 1} d_{12} \\ &\quad + \frac{-2\pi\kappa^2}{3\kappa^2 + 4\kappa + 1} d_{23}, \\ \theta_2^* &= 0 \times i_{dc,1} + \frac{\kappa + 1}{3\kappa + 1} i_{dc,2} + \frac{2\pi\kappa}{3\kappa + 1} d_{12} + \frac{-2\pi\kappa}{3\kappa + 1} d_{23}, \\ \theta_3^* &= -\frac{1}{\kappa + 1} i_{dc,1} + \frac{\kappa}{3\kappa + 1} i_{dc,2} + \frac{2\pi\kappa^2}{3\kappa^2 + 4\kappa + 1} d_{12} \\ &\quad + \frac{2\pi\kappa(2\kappa + 1)}{3\kappa^2 + 4\kappa + 1} d_{23}. \end{aligned} \quad (14)$$

Sets of steady-state phase offsets, normalized by 2π , are presented in Table I. The driving currents are $i_{dc,1} = 1.0$, $i_{dc,2} = 0.8$, and $i_{dc,3} = -1.0$ and the coupling parameters are $\kappa_1 = \kappa_2 = 0.1$. The table includes all of the possible sets of steady-state offsets where $n_1 \geq n_2 \geq n_3$ and $n_1 - n_3 \leq 2$. Without loss of generality, n_3 is defined to be 0 since the locations of local minima are symmetric to shifting all phases by 2π . For simplicity, we only present in Table I the states for $n_j < 3$. The estimated offsets θ_k^* found from (14) are rather close (within $\sim 17^\circ$) to the numerical solutions θ_k found from minimization via the Nelder-Mead simplex (direct search)

TABLE I. Offset phases of local minima of the potential function V in Eq. (8), when $i_{dc,1} = 1.0$, $i_{dc,2} = 0.8$, $i_{dc,3} = -1.0$, and $\kappa_1 = \kappa_2 = 0.1$. Each row shows the approximated offset phases from Eq. (13) θ_k^* and the true offset phases of the local minima θ_k for a given set of the multiples of 2π phase differences n_k . All of the offset phases (in radians) are scaled by 2π . The last column provides the potential value V at the local minima.

n_1	n_2	n_3	$\theta_1^*/2\pi$	$\theta_2^*/2\pi$	$\theta_3^*/2\pi$	$\theta_1/2\pi$	$\theta_2/2\pi$	$\theta_3/2\pi$	V
0	0	0	0.1545	0.1077	-0.1349	0.1992	0.1187	-0.1552	-1.272
1	0	0	0.0706	0.1847	-0.1279		no stable minimum		
1	1	0	0.1475	0.0308	-0.0510	0.1810	0.0338	-0.0515	-9.918
2	0	0	-0.0134	0.2616	-0.1209		no stable minimum		
2	1	0	0.0636	0.1077	-0.0440	0.0661	0.1164	-0.0437	-14.05
2	2	0	0.1405	-0.0461	0.0329	0.1670	-0.0443	0.0333	-15.29

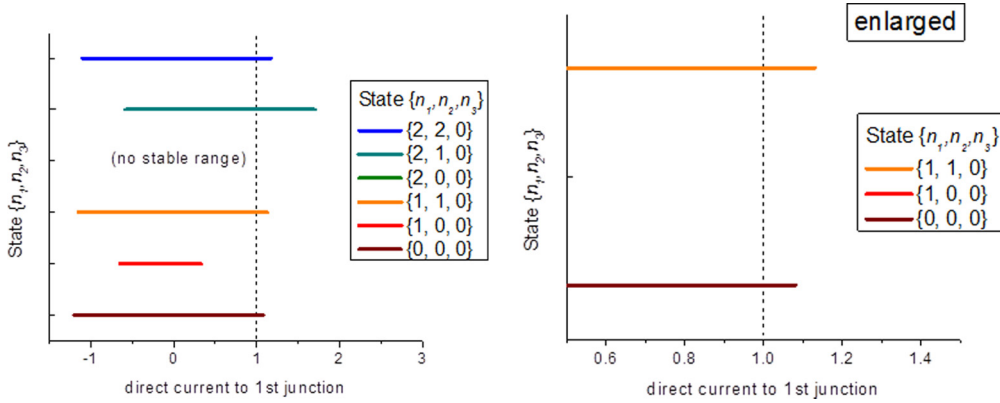


FIG. 2. Ranges of stability for the available states as a function of $i_{dc,1}$. Here $i_{dc,2} = 0.8$ and $i_{dc,3} = -1.0$. The vertical dashed line shows the default value of $i_{dc,1} = 1.0$. The right plot shows two stable states ($\{0, 0, 0\}$ and $\{1, 1, 0\}$) that we employed for memory operations. State $\{1, 0, 0\}$ is not shown in the right plot since it is unstable for parameter set that we used.

method on the potential function. The final column shows the values of the potential function at the local minima.

For the set of dc currents and coupling parameters employed, no steady-state set exists when the first junction phase is about 2π greater than both of the other two junction phases (see rows where $\{n_1, n_2, n_3\} = \{1, 0, 0\}$ and $\{2, 0, 0\}$). As will be discussed further in the next section, the lack of these stable states is crucial to our memory cell design since for memory cell demonstration we are only interested in manipulating the system within a particular sets of states, namely, states $\{0, 0, 0\}$ and $\{1, 1, 0\}$ in rows 1 and 3 of Table I.

The set of states $\{n_1, n_2, n_3\}$ listed in Table I shows equilibrium phases for the specific set of driving currents $i_{dc,1} = 1.0$, $i_{dc,2} = 0.8$, and $i_{dc,3} = -1.0$. If any of these currents were to change slightly, the equilibrium phases would adjust accordingly, but still reside in the same potential wells described by n_k . When the values of the dc currents change significantly, some of these steady states become unstable or no longer exist.

Figure 2 shows state $\{n_1, n_2, n_3\}$ existence intervals as a function of the values of the first junction dc current $i_{dc,1}$ while keeping the values of the other junction currents fixed. Figures 3 and 4 show state existence intervals as functions of the dc current applied to the second and the third junction,

respectively. The right plots show enlarged views of intervals of state existence curves near the parameter values that we will be using for memory operations. These are identified by the vertical dashed lines.

These stability diagrams are used in defining the values of dc current for memory operations. Adequately choosing parameter values and states to consider for memory operations is very important since many options are available. In this paper we do not perform rigorous optimization studies to optimize parameters for memory operation. We note that junction currents where states partially (not fully) overlap may be chosen as a possible candidate for memory operation. Operating the circuit with the dc current values that are at the edges of the state overlap may be beneficial to memory cell operations. Such memory operations are demonstrated later in the paper.

III. MEMORY ACCESS TIMES AND ENERGIES

In this section we describe the dynamics of the circuit and calculate the access times of circuit response to current pulses, which constitute memory write, read, and reset operations. The dynamics of the array is described by Eqs. (6). Our numerical results and mathematical analysis show that, in the

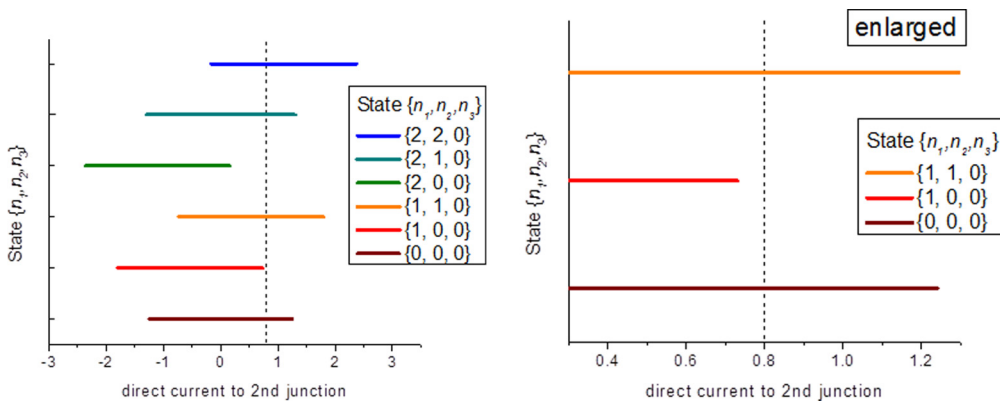


FIG. 3. Ranges of stability for available states as a function of $i_{dc,2}$. Here $i_{dc,1} = 1.0$ and $i_{dc,3} = -1.0$. The vertical dashed line shows the default value of $i_{dc,2} = 0.8$. The right plot shows two stable states ($\{0, 0, 0\}$ and $\{1, 1, 0\}$) that we employed for memory operations. In this figure we show an unstable state $\{1, 0, 0\}$.

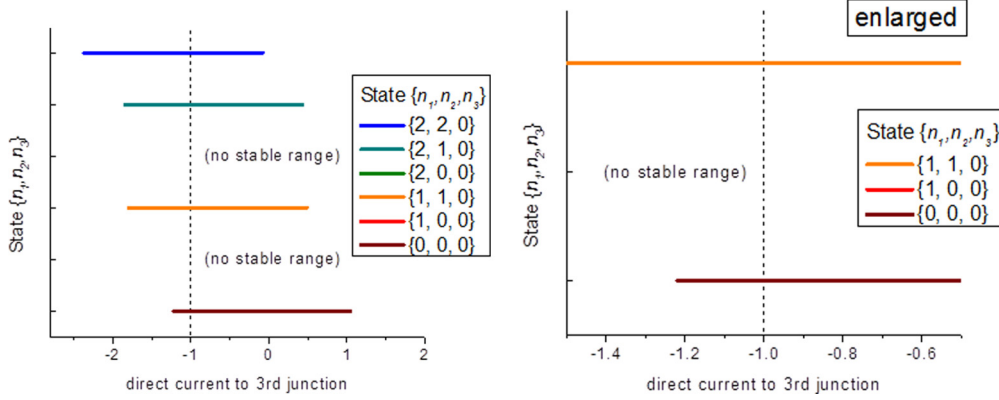


FIG. 4. Ranges of stability for available states as a function of $i_{dc,3}$. Here $i_{dc,1} = 1.0$ and $i_{dc,2} = 0.8$. The vertical dashed line shows the default value of $i_{dc,3} = -1.0$. The right plot shows two stable states ($\{0, 0, 0\}$ and $\{1, 1, 0\}$) that we employed for memory operations. State $\{1, 0, 0\}$ is not shown in this figure since it is unstable for parameter set that we used.

limit of weak coupling strength (possibly weak to moderate coupling), pulse operation on a single junction induces separable dynamics where only one junction moves significantly at a given time while the rest of the junctions are close to their steady-state positions (examples of such separable behavior are presented in the next section, where we present examples of memory operations). This conclusion is also consistent with the previously published work [15,16]. To study the dynamics of the array, we first rewrite Eqs. (6) in the form

$$\begin{aligned}\gamma_1 \frac{d\phi_1}{d\tau} &= i_1 + \kappa_1(\phi_2 - \phi_1) - \sin \phi_1, \\ \gamma_2 \frac{d\phi_2}{d\tau} &= i_2 + \kappa_1(\phi_1 - \phi_2) + \kappa_2(\phi_3 - \phi_2) - \sin \phi_2, \\ \gamma_3 \frac{d\phi_3}{d\tau} &= i_3 + \kappa_2(\phi_2 - \phi_3) - \sin \phi_3.\end{aligned}\quad (15)$$

We neglect the contribution of the second derivative since for the regimes of our consideration it is rather small relative to the first derivative. Since we have chosen all the coupling terms to be equal, we can rewrite these equations in the following way:

$$\begin{aligned}\gamma_1 \frac{d\phi_1}{d\tau} &= i_1 + \kappa(\phi_2 - \phi_1) - \sin \phi_1, \\ \gamma_2 \frac{d\phi_2}{d\tau} &= i_2 + \kappa(\phi_1 - 2\phi_2 + \phi_3) - \sin \phi_2, \\ \gamma_3 \frac{d\phi_3}{d\tau} &= i_3 + \kappa(\phi_2 - \phi_3) - \sin \phi_3.\end{aligned}\quad (16)$$

Due to separable motion of each junction (only one junction moves at a given time), Eqs. (16) can be decoupled and rewritten in the form

$$\begin{aligned}\gamma_1 \frac{d\phi_1}{d\tau} &= i_1 + \kappa(\phi_{2eq} - \phi_1) - \sin \phi_1, \\ \gamma_2 \frac{d\phi_2}{d\tau} &= i_2 + \kappa(\phi_{1eq} + 2\pi - \phi_2) - \kappa(\phi_2 - \phi_{3eq}) - \sin \phi_2, \\ \gamma_3 \frac{d\phi_3}{d\tau} &= i_3 + \kappa(\phi_{2eq} + 2\pi - \phi_3) - \sin \phi_3.\end{aligned}\quad (17)$$

Here ϕ_{1eq} , ϕ_{2eq} , and ϕ_{3eq} are the equilibrium phases of the junctions. The mathematical basis for the solution of these equations was presented in [15,16]. However, we would like

to clarify that while in Refs. [15] and [16] all the junctions were dc current driven and the steady solution constituted the nonzero voltage (velocity), in this paper we only drive one junction for a short period of time. We are only interested in one period of integration that is required for the array to respond to an external pulse applied to that single junction. Subsequently, in the time between the pulse excitations required for memory operations, the junctions' voltages are zero. We also approximate the pulse shape for excitation as rectangular. Taking into consideration all the approximations presented above, for reasons of completeness and clarity, we are following derivations from Ref. [15]. We first write these equations in a rather generic form

$$\gamma \frac{d\phi}{dt} = F(\phi) \quad (18)$$

and

$$dt = \gamma \frac{d\phi}{F(\phi)}. \quad (19)$$

Subsequently,

$$T = \gamma \int \frac{d\phi}{F(\phi)} = \gamma \int d\phi \exp\{-\ln[F(\phi)]\}. \quad (20)$$

We can now expand

$$\begin{aligned}\ln F(\phi) &\approx \ln[F(\phi_c)] + \frac{F'}{F}(\phi - \phi_c) + \frac{FF'' - F'^2}{2F^2}(\phi - \phi_c)^2 \\ &\quad + \dots\end{aligned}\quad (21)$$

Since $F'(\phi_c) = 0$, we get

$$\ln F(\phi) \approx \ln[F(\phi_c)] + \frac{F''(\phi_c)}{2F(\phi_c)}(\phi - \phi_c)^2 + \dots \quad (22)$$

Using saddle-point integration method, we obtain

$$T \approx \gamma F^{-1}(\phi_c) \int_{-\infty}^{\infty} \exp\left[-\left(\frac{F''(\phi_c)}{2F(\phi_c)}(\phi - \phi_c)^2\right)\right] d\phi \quad (23)$$

or

$$T \approx \gamma F^{-1}(\phi_c) \sqrt{\frac{2\pi F(\phi_c)}{F''(\phi_c)}} = \gamma \sqrt{\frac{2\pi}{F(\phi_c)F''(\phi_c)}}. \quad (24)$$

For each junction we will use a subscript to describe the particular F ,

$$\begin{aligned} F_1(\phi_1) &= i_1 + \kappa(\phi_{2\text{eq}} - \phi_1) - \sin \phi_1, \\ F_2(\phi_2) &= i_2 + \kappa(\phi_{1\text{eq}} + 2\pi - \phi_2) - \kappa(\phi_2 - \phi_{3\text{eq}}) - \sin \phi_2, \\ F_3(\phi_3) &= i_3 + \kappa(\phi_{2\text{eq}} + 2\pi - \phi_3) - \sin \phi_3. \end{aligned} \quad (25)$$

In our setup, $i_{3\text{dc}} = -i_{1\text{dc}}$, thus

$$F_3(\phi_3) = -i_{1\text{dc}} + i_{3\text{pulse}} + \kappa(\phi_{2\text{eq}} + 2\pi - \phi_3) - \sin \phi_3. \quad (26)$$

Also for very small values of the coupling κ , $\phi_c \approx \pi/2t$, therefore we rewrite the expressions for functions F as

$$\begin{aligned} F_1(\phi_c) &= i_1 + \kappa(\phi_{2\text{eq}} - \pi/2) - 1, \\ F_2(\phi_c) &= i_2 + \kappa(\phi_{1\text{eq}} + 2\pi - \pi/2) - \kappa(\pi/2 - \phi_{3\text{eq}}) - 1, \\ F_3(\phi_c) &= i_3 + \kappa(\phi_{2\text{eq}} + 2\pi - \pi/2) - 1. \end{aligned} \quad (27)$$

Since the second derivative of F is equal to $\sin(\phi_c) \approx 1$, this term can now be omitted. Thus we get

$$\begin{aligned} T_1 &\approx \gamma \sqrt{\frac{2\pi}{i_1 + \kappa(\phi_{2\text{eq}} - \pi/2) - 1}}, \\ T_2 &\approx \gamma \sqrt{\frac{2\pi}{i_2 + \kappa(\phi_{1\text{eq}} + 2\pi - \pi/2) - \kappa(\pi/2 - \phi_{3\text{eq}}) - 1}}, \\ T_3 &\approx \gamma \sqrt{\frac{2\pi}{i_3 + \kappa(\phi_{2\text{eq}} + 2\pi - \pi/2) - 1}}. \end{aligned} \quad (28)$$

We can estimate the values of the time (period T) required to complete the transition from one state to another (which is, in principle, the time delay between the application of the pulse to the circuit response):

$$\begin{aligned} T_1 &\approx \gamma \sqrt{\frac{2\pi}{i_1 + \kappa(\phi_{2\text{eq}} - \pi/2) - 1}} \\ &\approx \gamma \sqrt{\frac{2\pi}{i_1 + \kappa(2\pi \times 0.15 - \pi/2) - 1}} \\ &\approx \gamma \sqrt{\frac{2\pi}{i_{\text{pulse}} - 0.2\kappa\pi}} \approx 6.25 \approx 26 \text{ ps}, \end{aligned}$$

$$\begin{aligned} T_2 &\approx \gamma \sqrt{\frac{2\pi}{i_2 + \kappa(\phi_{1\text{eq}} + 2\pi - \pi/2) - \kappa(\pi/2 - \phi_{3\text{eq}}) - 1}} \\ &\approx \gamma \sqrt{\frac{2\pi}{i_2 + \kappa(\phi_{1\text{eq}} + 2\pi - \pi/2) - \kappa(\pi/2 - \phi_{3\text{eq}}) - 1}} \\ &\approx 6.5 \approx 27 \text{ ps}, \\ T_3 &\approx \gamma \sqrt{\frac{2\pi}{i_3 + \kappa(\phi_{2\text{eq}} + 2\pi - \pi/2) - 1}} \\ &\approx \gamma \sqrt{\frac{2\pi}{i_3 + \kappa(\phi_{2\text{eq}} + 2\pi - \pi/2) - 1}} \approx 3 \approx 12 \text{ ps}. \end{aligned} \quad (29)$$

The time periods in Eqs. (29) provide a fair estimation of the access times for memory operations (memory operations can be applied to any junction and in the following section we will provide examples of the memory operation). Our numerical results show similar access times, thus our estimation is that access times for the entire operation (including reset times) will stay in the range of 10–100 ps (dependent on the parameter values).

We would like to briefly discuss junction switching and dissipation energies required for basic memory cell operations. The RSJ potential energy can be written as $E(\varphi) = E_J(1 - \cos\varphi - \frac{I_b}{I_c}\varphi)$, where I_b is the bias current, I_c is the critical current, and $E_J = I_c\Phi_0/2\pi$. The energy difference between the two minima is given by $\Delta E = 2\pi \frac{I_b}{I_c} E_J$. The switching energy is equal to the height of the potential barrier between the adjacent minima, which is $\Delta E = 2\pi \frac{I_b}{I_c} E_J = 2\pi \frac{I_b}{I_c} \frac{I_c\Phi_0}{2\pi} = I_b\Phi_0$. Consequently, the switching energy for a conventional SFQ process theoretically can be very low provided that the bias current is low. This is not the case in typical experiments and the typical value of the bias current due to circuit speed and error bit optimization process is $I_b = 0.7I_c$ [14], which makes the switching energy equal to about 1.4×10^{-19} J.

For a design based on coupled arrays of Josephson junctions, the switching energy can also be arbitrarily small and is equal to $\Delta E = I_{\text{pulse}}\Phi_0$, where I_{pulse} is the pulse current. For very small pulses, however, one could run into the same issues as for a conventional switching process. If I_{pulse} is very small, the robustness and stability of memory operation may be compromised due to parameter disorder, noise, and other

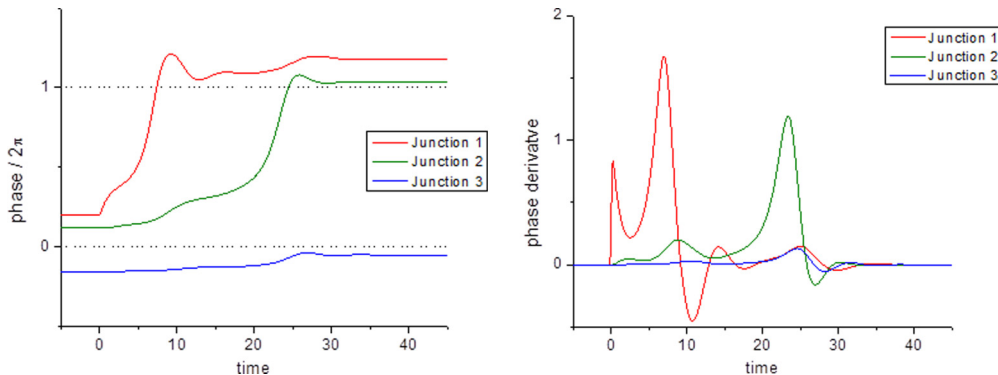


FIG. 5. Time dependences of phases scaled by 2π (left) and phase derivatives (right) of the system in response to a Gaussian pulse applied to the first junction when the system is in state 0. Here $i_{\text{pulse},1} = 1.0$.

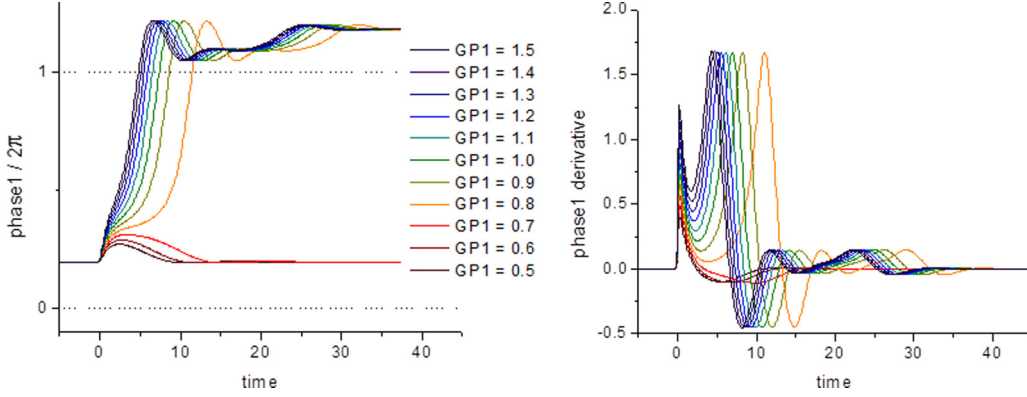


FIG. 6. Time series of the first junction phase scaled by 2π (left) and first junction phase's derivative (right) of the system in response to a Gaussian pulse applied to the first junction when the system is in state 0. The pulse amplitudes $i_{\text{pulse},1}$ vary from 0.5 (dark red) to 1.5 (dark violet).

reasons. For that same reason, in our simulations the switching energy was also in the range of 5×10^{-18} – 10^{-19} J.

Perhaps a much more important parameter in memory cell operation would be energy loss or dissipation per bit of operation. Energy dissipation for one flip is given by the same expression as the expression for flipping energy $I_b \Phi_0$. High energy dissipation is one of major challenges for superconducting computing [10]. For rapid single flux quantum cells the average number of Josephson junction switches per bit operation is in the range of 10 [14]. Since in the proposed design all major memory cell operations (read, write, and reset) are implemented on the same circuit, the number of switching per bit could be reduced. For the proposed logic circuits, only one or two junctions have to be switched in order to implement any of the basic memory operations. This could potentially indicate a benefit of using array-based memory cell logic circuits.

IV. MEMORY CELL OPERATION

In this section we will present basic memory cell operations (write, read, and reset). A circuit can operate as a memory cell if a set of operations can transition the system to well-defined states and can generate a signal that carries information about memory states. The value n_k , as presented in Eq. (10), will describe the location of the k th junction phase. When all three junction phases are in the zero sinusoidal potential well, the system will be considered in the 0 state $\{n_1, n_2, n_3\} = \{0, 0, 0\}$. When the phases of the first and second junctions are shifted to the next potential well (about 2π greater), the cell will be in the 1 state, $\{n_1, n_2, n_3\} = \{1, 1, 0\}$. These two states correspond to the first and third rows of Table I.

The proposed circuit (see Fig. 1) or family of similar circuits can be employed in a variety of ways to implement a functional memory device. Here we are demonstrating just one example of basic memory operation and we only use two states as 0 and 1. We would like to note that memory operations presented below may not be optimal for this circuit and additional studies are required to optimize memory cell operation designs. We will be employing Gaussian pulses to demonstrate memory cell logic circuits, however, other types of pulses (such as rectangular pulse, SFQ, or other shapes) can be used as well.

The presented memory cell logic circuits are fundamentally different from the conventional SFQ logic circuits. An SFQ pulse is a voltage pulse generated at the Josephson junction when the phase difference for a junction flip is exactly 2π . The Josephson relation $\frac{d\varphi}{dt} = \frac{2e}{\hbar} V$ guarantees then that SFQ pulses have a quantized area equal to a single flux quantum $\int V dt = \frac{\hbar}{2e} \int_0^{2\pi} \frac{d\varphi}{dt} dt = \frac{\hbar}{2e} \equiv \Phi_0$ that is a single flux quantum. Since in our presented memory cell design, memory states are generated and recorded based on the array dynamics, junction phase rotations are not equal exactly to 2π or its multiples.

A. Write 1 operation

If a pulse applied to the system always yields a transition to the 1 state, then the operation can be considered as a memory write 1 operation. The equilibrium configuration of the phases in the 1 state is a stable state where the phases of the first and second junctions are shifted into their next potential well (approximately 2π greater than the phase of the third junction). In order for the transition from the 0 state to the 1 state to be successful, the energy injected into the system by a pulse must only affect the phases of the first and second junctions. In our example design, we apply a pulse to the first junction. Due to

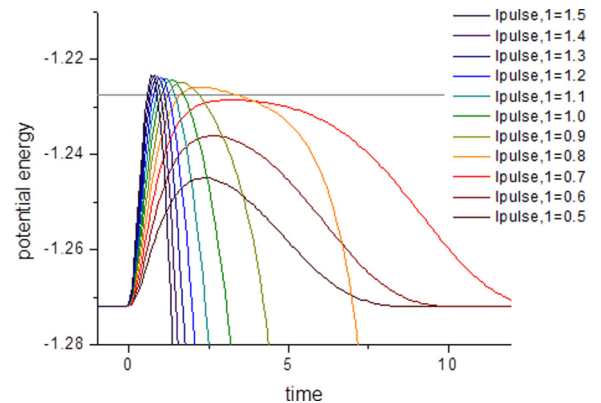


FIG. 7. Time series of the system's potential energy of the responses shown in Fig. 6. The Gaussian pulse amplitudes $i_{\text{pulse},1}$ vary from 0.5 (dark red) to 1.5 (dark violet). The barrier energy is around 0.045. The gray line shows the sum of the initial potential energy and the barrier energy.

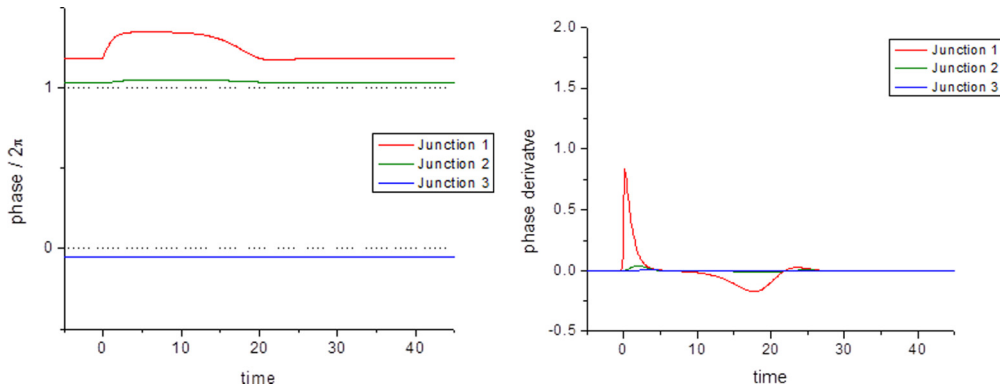


FIG. 8. Time series of phases scaled by 2π (left) and phase derivatives (right) of the system in response to a Gaussian pulse applied to the first junction when the system is in state 1. Here $i_{\text{pulse},1} = 1.0$.

the coupling between the first and second junctions, this pulse will cause the phase shift of the second junction as well. The potential energy of state 1 is less than the potential energy of state 0. The state $\{n_3\}$ of the third junction will not change for the choice of system and pulse parameters.

The curves in Fig. 5 show the response to the Gaussian pulse of size $i_{\text{pulse},1} = 1.0$ being applied to the first junction after the system has settled into its 0 state. All of the pulses described in this section will have a pulse width of $\sigma = 0.1$ and a pulse center at zero time. The phase dynamics shown in Fig. 5 show the phase of the first junction rising quickly to the next local minimum, followed by the phase of the second junction. The phase of the third junction slightly shifts its equilibrium position but stays in the same potential well. The period of the full transition from states 0 to 1 is of the order of 25 units of time, which is the equivalent of 100 ps. The slower time scale is due to the fact that the system undergoes two transitions. The energy per pulse is of the order of 5×10^{-19} J. This value of the energy per pulse is typical to all the other memory command energy per pulse values. After the first transition, junction phases begin to slow down near the state $\{n_1, n_2, n_3\} = \{1, 0, 0\}$, but since no local minimum exists there phases then start a second transition to state 1 at $\{n_1, n_2, n_3\} = \{1, 1, 0\}$.

Figure 6 shows the responses of the first junction phase as a function of time for a variety of pulse amplitudes. The pulse widths σ are all fixed at 0.1, but the amplitudes $i_{\text{pulse},1}$ range from 0.5 to 1.5 [see Eq. (7) for the definition of the Gaussian pulse].

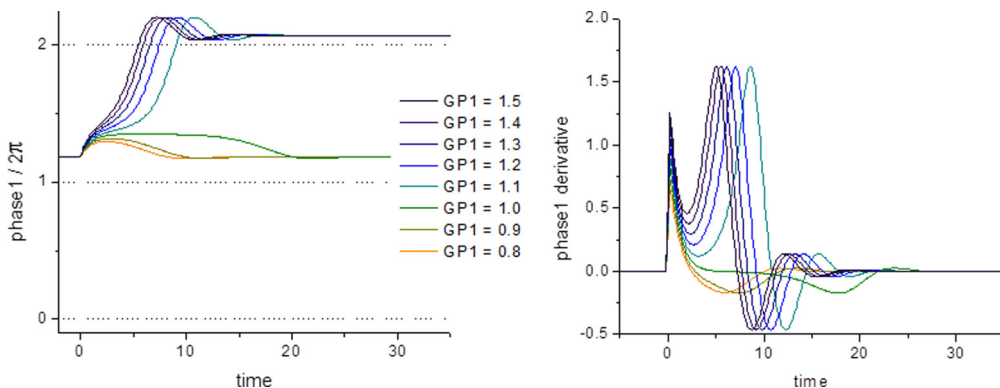


FIG. 9. Time series of first junction phase scaled by 2π (left) and first junction phase’s derivative (right) of the system in response to a Gaussian pulse applied to the first junction when the system is in state 1. The pulse amplitudes $i_{\text{pulse},1}$ vary from 0.8 (yellow) to 1.5 (dark violet).

The pulses add energy into the system. If this energy is sufficient to overcome the barrier energy, then the system transitions into the steady state corresponding to state 1. The maximum value of the phase derivative is approximately 1.6 which is equivalent to 0.8 mV. The phase derivative spike is caused by the phase slip and is almost independent on the characteristics of the pulse that triggered the phase slip.

The time series of the system’s potential energy is plotted in Fig. 7. It shows the potential energy of the system over time for the responses plotted in Fig. 6. Most of the curves show a potential energy increase and then a rapid decrease after the system passed the energy barrier. The three curves where pulse values $i_{\text{pulse},1}$ are less than 0.8 indicate that the system failed to pass beyond the potential threshold and consequently did not transition to the next state. The barrier energy found from this figure is about 0.045, which is the equivalent of 10^{-19} J or 0.1 aJ.

If the same pulse (as the one in Fig. 5) is applied to the first junction when the system is already in state 1, as shown in Fig. 8, no change to the junction’s phase occurs (after the transient dynamics dissipate). The system remains in state 1. Therefore, this pulse can be interpreted as a write 1 operator since the final state will always be 1 regardless of whether initial state was 0 or 1.

Another criterion for the first pulse’s amplitude must be noted: It cannot be strong enough to drive the system out of state 1. In Fig. 9 we demonstrate the time-dependent responses of the first junction phase to a set of pulses with variable

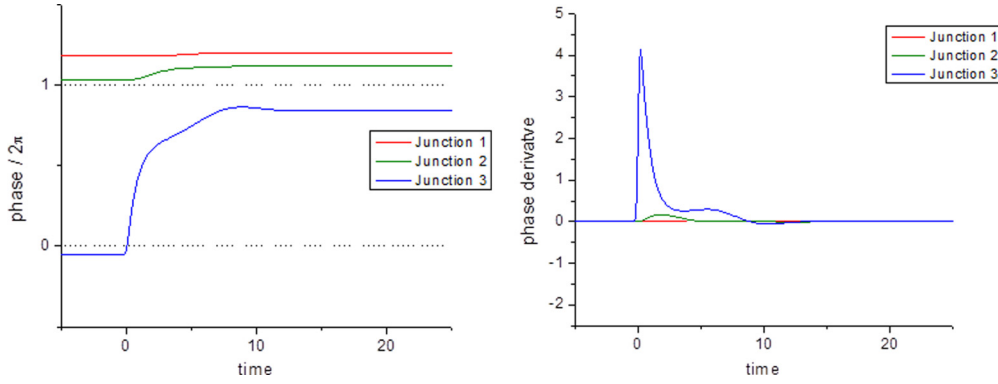


FIG. 10. Time series of phases scaled by 2π (left) and phase derivatives (right) of the system in response to a Gaussian pulse applied to the third junction when the system is in state 1. Here $i_{\text{pulse},3} = 5.0$.

strengths. If the pulse strength is proper it will transition the circuit from state 0 to 1. Strong enough pulses that exceed the energy barrier will drive the circuit from the state $\{n_1, n_2, n_3\} = \{1, 1, 0\}$ to the state $\{n_1, n_2, n_3\} = \{2, 1, 0\}$. These pulses are unacceptably strong.

B. Write 0 operation

The memory’s write 0 or reset operation is implemented by sending a pulse to the third junction. The transition from state 1 back to 0 is demonstrated in Fig. 10, where the pulse applied to the third junction has an amplitude of $i_{\text{pulse},3} = 5.0$. After the third junction phase moves to the next potential well, all the phases are within the same potential well (i.e., have the same multiple of 2π). The new steady-state phases are exactly 2π larger than the phases in the $\{0, 0, 0\}$ state. The new state is $\{n_1, n_2, n_3\} = \{1, 1, 1\}$, which by definition is equivalent to state $\{0, 0, 0\}$. The transformation occurs over a similar time period that was calculated according to the approximation calculated in Eq. (29).

For this pulse to successfully reset the state from 1 to 0, the pulse needs to be strong enough to counter the driving current in the opposing direction. This is why this pulse’s amplitude is greater than that of the write 1 pulse. Figure 11 shows the responses of the system in state 1 to a collection of pulses applied to the third junction whose amplitudes $i_{\text{pulse},3}$

range from 4.5 to 5.2. Only the pulse amplitudes equal to 4.9 and larger are sufficient to let the system exceed the potential threshold. The derivative of the third junction phase reaches a value of 4.5, which is equivalent to 2.25 mV.

To analytically estimate the barrier energy of this transition, a simplified description of the dynamics is used. The response is considered to describe the transition of the third junction phase while the phases of other junctions remain in their positions. The potential function would then become

$$V(\phi_3 | \phi_1 = \phi_2 = 2\pi) = \frac{\kappa_2}{2}(\phi_3 - 2\pi)^2 - i_{\text{dc},3}\phi_3 - \cos \phi_3 - 2\pi(i_{\text{dc},1} + i_{\text{dc},2}) + 1. \tag{30}$$

The local minimum and maximum would occur when ϕ_3 satisfies Eq. (31), which equates a linear function with a sine function. These two functions are plotted on the left-hand side in Fig. 12 for the set of parameters as defined above. The corresponding potential as a function of the third junction phase (30) is plotted on the right-hand side of Fig. 12. The intersections of the left plot correspond to local extrema on the right plot. The difference in potential between the minimum near 0 and the maximum before reaching the next potential well is 4.00, the estimated barrier energy using the simplified description of the dynamics. The ϕ_3 value of local extrema of V , when $\phi_1 = \phi_2 = 2\pi$, is

$$-\kappa_2\phi_3 + 2\pi\kappa_2 + i_{\text{dc},3} = \sin \phi_3. \tag{31}$$

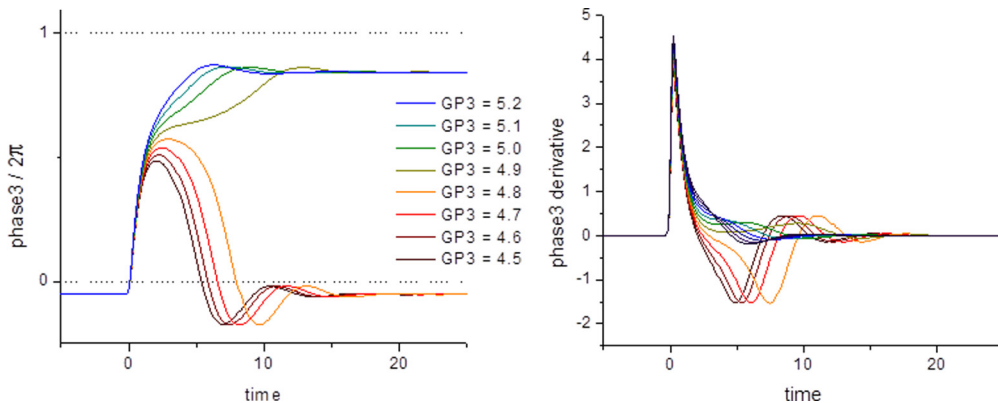


FIG. 11. Time series of the third junction phase scaled by 2π (left) and third junction phase’s derivative (right) of the system in response to a Gaussian pulse applied to the third junction when the system is in state 1. The pulse amplitudes $i_{\text{pulse},3}$ vary from 4.5 (dark red) to 5.2 (blue).

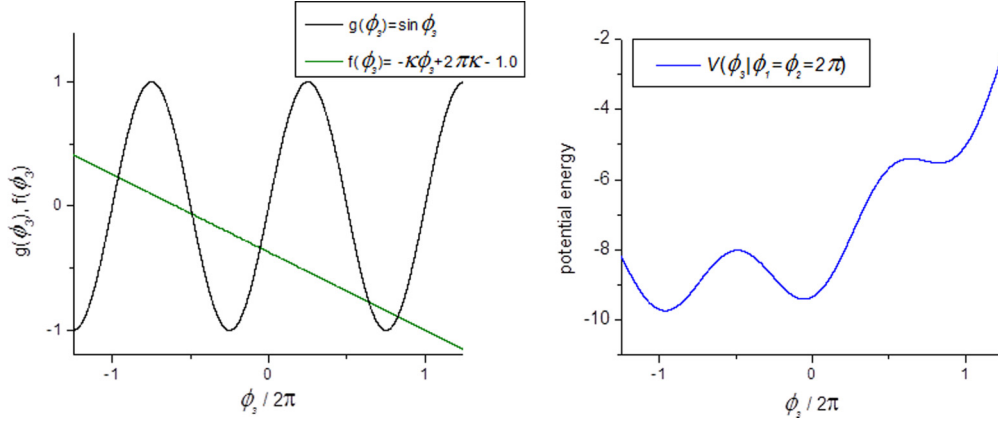


FIG. 12. The left figure compares the functions on the left (green) and right (black) sides of Eq. (31), where $i_{dc,3} = 1$ and $\kappa_2 = 0$. The right figure shows the potential energy V as a function of the third junction phase when the other junction phases are fixed at 2π . Intersections in the left plot correspond to local extrema in the right plot. The barrier energy between the minima near $\phi_3 = 0$ and $\phi_3 = 2\pi$ is 4.00.

Figure 13 shows potential energies of the system as functions of time for responses to pulses of different amplitudes. The set of responses that result in a new steady state for the system indicate that the array received enough energy from the pulse to make a transition. The grey line in Fig. 13 defines a threshold for this transition, indicating that in order to transition to the next state the gain in potential energy of the circuit due to the external pulse must be at least 3.81 (in dimensionless units). The reduced-order model presented above predicted a barrier energy of 4.00, which is reasonably close to the numerical estimation.

Figure 14 shows the responses to the same pulse as the one in Fig. 11 when the junction array state is 0. No change in the state is observed after the transient behavior dissipates. This pulse will transition the system to state 0 from either initial state. This suggests that the pulse applied to the third junction can be used as a write 0 operation.

Figure 15 shows that if a pulse is too strong, it would provide too much kinetic energy to the third junction and the system would transition over the potential barrier in the opposite direction. This third junction phase would settle

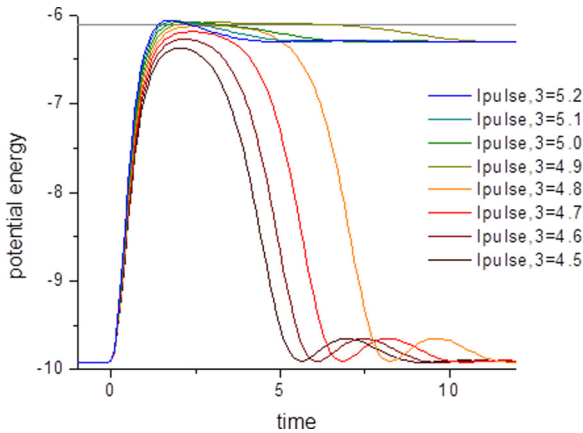


FIG. 13. Time series of the system's potential energy of the responses shown in Fig. 11. The Gaussian pulse amplitudes $i_{pulse,3}$ vary from 4.5 (dark red) to 5.2 (blue). The barrier energy is around 3.81. The grey line shows the initial potential energy plus the barrier energy.

into a steady state that is different from the other junction phases by approximately a multiple of 2π . This would be the state $\{n_1, n_2, n_3\} = \{0, 0, -1\} = \{1, 1, 0\}$. The figures show the responses of the system in state 0 to a set of pulses applied to the third junction whose amplitudes $i_{pulse,3}$ range from 4.5 to 5.5.

C. Read operation

In order to read the memory state, we use a pulse that can be applied to one of the junctions. A condition of a successful read operation is that application of a read pulse results in different outputs from the circuit dependent on whether the circuit was at the 0 or 1 memory state. Reading memory state of the array can be implemented by probing response of the second junction to a pulse applied to the first junction. When the initial state of the circuit is 1, there will be very weak phase and phase derivative responses of the second junction to a pulse applied to the first junction. On the contrary, when the initial state of the memory circuit is 0, the external pulse to the first junction causes phase shift of the second junction to the next stable equilibrium position of the second junction. This phase shift is close (but not equal) to 2π . Consequently, the second junction phase derivative (voltage) time series displays a strong spike that can be sensed by an appropriate sense circuit. Thus, the second junction response depends on the initial state of the circuit. However, as it is for destructive read operations, after the read command is performed the circuit state will always be settling in state 1. Figure 16 shows the responses of the second junction to the pulse sent to the first junction [the same as a write 1 operation (Figs. 5 and 8)].

A read operation could also be implemented by sending a pulse to the third junction and subsequently reading the response from that same junction. Sending a pulse to the third junction will also always set the circuit to the 0 state, similar to our previous example.

In Table II we summarize the above example of the basic memory cell operations presented in this section.

V. MEMORY PERFORMANCE EVALUATION

In order to evaluate and improve the Josephson junction based memory circuit performance we performed an iterative

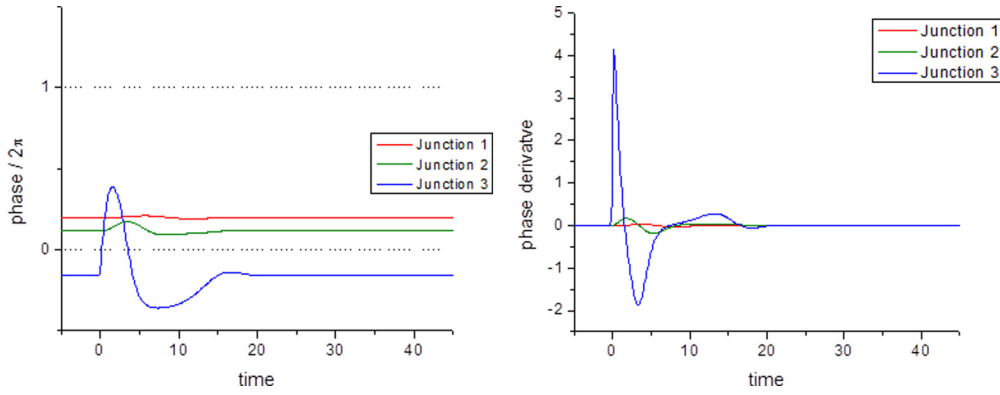


FIG. 14. Time series of phases scaled by 2π (left) and phase derivatives (right) of the system in response to a Gaussian pulse applied to the third junction when the system is in state 0. Here $i_{\text{pulse},3} = 5.0$.

optimization algorithm. The iterative algorithm employed is called simulated annealing (SA), a globally convergent optimization technique. Simulated annealing attempts to minimize a function in a manner similar to annealing to find a global minimum of the preselected cost function. Corana *et al.* [17] implementation of SA for continuous variables is used in the present methodology in conjunction with our coupled junction simulation module. Simulated annealing explores the target function’s entire surface by performing random walks in m parameter space, where m represents the number of optimization variables. A rough view of the parameter space is first obtained by moving with large step lengths. As the algorithm progresses and falls, it focuses on the most promising area within the parameter space. Simulated annealing attempts to optimize the function while moving both uphill and downhill in order to escape local minima. Simulated annealing has other advantages, which suggest its use for the optimization of Josephson junction parameters. First, unlike many iterative optimization schemes (e.g., Newton or steepest-descent schemes), SA can produce accurate results even for poor choices of initial conditions. Moreover, SA makes no assumption that a cost function is continuous, which is important here because we have defined our cost functions to be discontinuous. Finally, SA can be used on cost functions of arbitrary numbers of variables. For more details about SA and its applications, see, for example, [17–19].

We employed a SA procedure for external pulse and external current parameters to numerically calculate access times and access energies. Comprehensive results for optimization procedure will be reported in Ref. [20] and in the present paper we only provide a very brief summary of the results. We kept pulse and external current parameter variation in such a way that variations in these parameters would not affect the existence of two predesigned memory states $(\{0,0,0\}-\{1,1,0\})$ and would allow transitions between these states to implement valid read, write, and reset operations. Such a requirement, for obvious reasons, has limited the values of the parameters that can be employed. As we iterated pulse parameters in acceptable limits to stay within the prescribed or preselected states we observed that the fluctuations in access times and access energies can vary (perhaps by a factor of 1.5–2 or more). An example of the minimal pulse amplitudes to implement transitions from 0 state to 1 and from 1 state to 0 (and consequently, valid write, read, and reset operations) as functions of the dc amplitudes of the junctions 1 and 3 is demonstrated in Fig. 17. Note that in Fig. 17 we are showing results for a larger value of the coupling constant, namely, $\kappa = 0.5$, while for other figures in the paper we have used the value of $\kappa = 0.1$. The reason for that is that our calculation of the access time (and consequently access energies) utilizes an approximation of separable dynamics [Eqs. (17)–(29)] that is accurate in the limit of the weak coupling. However, we

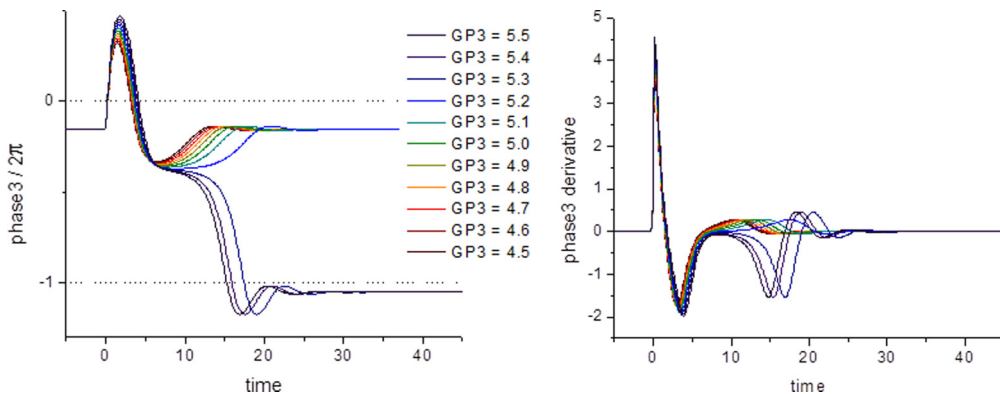


FIG. 15. Time series of the third junction phase scaled by 2π (left) and third junction phase’s derivative (right) of the system in response to a Gaussian pulse applied to the third junction when the system is in state 0. The pulse amplitudes $i_{\text{pulse},3}$ go from 4.5 (dark red) to 5.5 (dark violet).

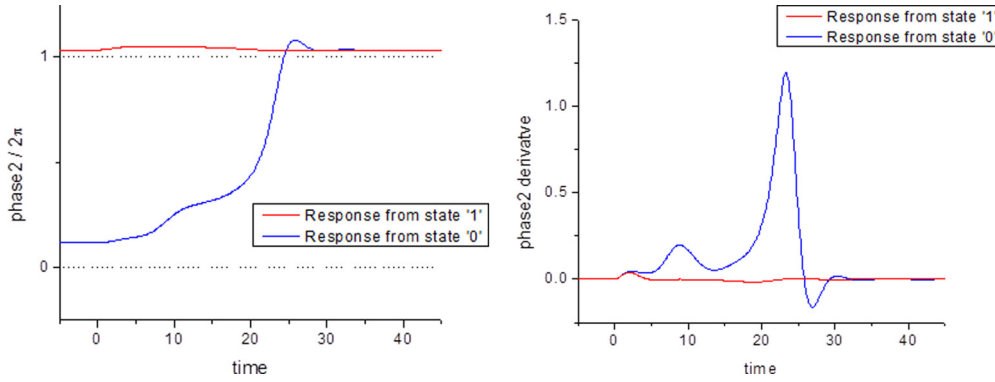


FIG. 16. Time series of the second junction phase scaled by 2π (left) and second junction phase’s derivative, or voltage (right), in response to a Gaussian pulse applied to the first junction when the system is in state 1 (red curves) and 0 (blue curves). Here $i_{\text{pulse},1} = 1.0$.

would also like to show that the proposed logic circuits can be applicable for a much larger value of the coupling constant (thus substantially reducing the size of the memory cell).

There exists some parameter range for which access times and access energies vary modestly and for some other parameter range memory operations may be very sensitive to pulse and external current parameter values (since parameter fluctuations will alter Josephson junction array memory states and consequently affect memory operation). Our main conclusion is that it is indeed possible to set pulse and external current parameter values amenable for nonfaulty and robust memory operation. For those parameter values the access times are in the range of 10–100 ps (for read, write, and reset operations) and access energies are in the range of 5×10^{-18} – 10^{-19} J (0.1–5 aJ).

We would also like to briefly discuss the scalability of the proposed memory logic circuits to large memory cell arrays. First, we would like to note that the stability diagram of the three-junction array (see Fig. 4) shows multistability; consequently, one can in principle design a four- or even possibly eight-bit operation for each memory cell. It would be fascinating to explore memory states of larger arrays of coupled junctions, however we would be cautious not to propose such a design (at this time) as a route for scalability to large memory cell arrays. Since in currently available memory cell array designs memory cells are operated as separate (uncoupled) components with separate access to each cell, a seemingly straightforward route towards scalability would be following currently available designs (see, for example, Refs. [6,21–23]). Moreover, since our proposed memory cell design seems to be much less complicated and small in size

than, for example, today’s state-of-the-art design [6] where read and write operations are implemented on separate circuits, peripheral circuits such as sense and current driver circuits could also be less complex and consequently smaller in size and perhaps requiring lower operational energy. We would also like to note that scaling the memory cell to large arrays requires consideration of all the peripheral circuits (including decoders, drivers, sense circuits, and others [6,21–23]). Consequently, since basic current and pulse driving and the pulse sensing requirement of the proposed memory cell are rather common to other memory cell designs we believe that scaling to large memory arrays is possible. Moreover, the proposed memory cell design is simpler and smaller in size than other memory cell circuits (see, for example, the memory cell circuit in Refs. [6,22]).

VI. SUMMARY

In this paper we demonstrated a paradigm for cryogenic memory operation and presented a specific example of a circuit that consists of three inductively coupled Josephson junctions. We have employed Josephson junction nondimensionless parameter values that are consistent with the current state-of-the-art Josephson junction fabrication capabilities as presented in Ref. [13]. The principles of memory design and operation described in the paper can in principle be implemented for other Josephson junction based circuits. In the proposed circuit write, read, and reset operations are implemented on the same circuit. For the parameter values presented in the paper, access

TABLE II. Logic circuits of basic memory cell operations.

Initial state	Write 0	Write 1	Read
original state 0	applied junction J_3 end state 0	applied junction J_1 end state 1	applied junction J_1 end state 1 read junction J_2
original state 1	applied junction J_3 end state 0	applied junction J_1 end state 1	applied junction J_3 end state 1 read junction J_2

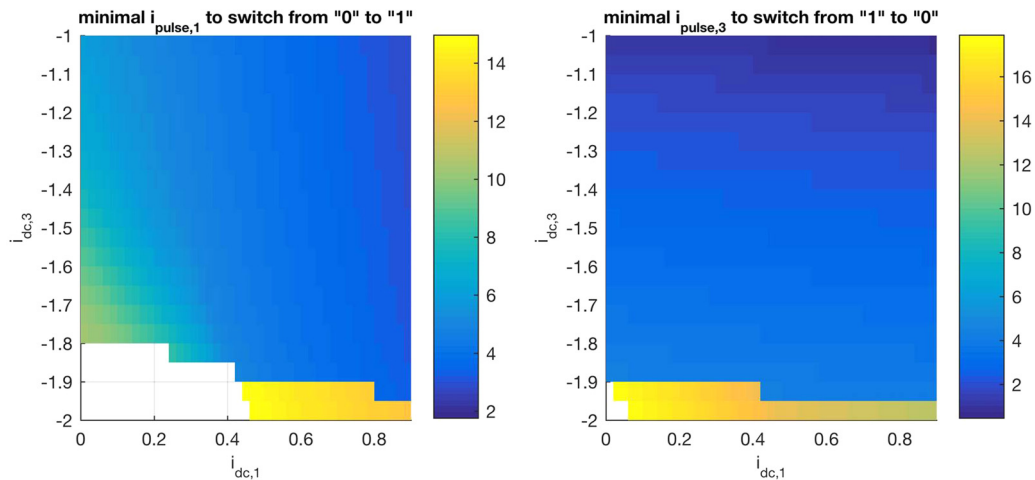


FIG. 17. Shown on the left is the minimal Gaussian pulse amplitude for transition from 0 to 1 and on the right is the minimal pulse amplitude for transition from the 1 to 0 operation.

times are of the order of 10–100 ps, while access energy is of the order of 0.1–5 aJ. A wide variety of parameters can be used for memory operation in the regime of weak to moderate coupling ranges, while so far the challenge was to increase the values of the coupling constant κ to the limit of strong coupling [20] and consequently decrease the feature size or area of the inductor. This may require modifications of the presented circuit or modifications of the single junction parameters of the circuit.

ACKNOWLEDGMENTS

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