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Noise-free logical stochastic resonance

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The phenomena of *logical stochastic resonance* (LSR) was demonstrated recently [Phys. Rev. Lett. **102**, 104101 (2009)]: namely, when a bistable system is driven by two inputs it consistently yields a response mirroring a logic function of the two inputs in an optimal window of moderate noise. Here we examine the intriguing possibility of obtaining dynamical behavior equivalent to LSR in a noise-free bistable system, subjected only to periodic forcing, such as sinusoidal driving or rectangular pulse trains. We find that such a system, despite having no stochastic influence, also yields phenomena analogous to LSR, in an appropriate window of frequency and amplitude of the periodic forcing. The results are corroborated by circuit experiments.

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It has been shown that a noisy bistable system, when driven by two square waves as inputs, produces a logical response in some optimal range of noise [1]. The probability of getting such response increases to unity with increasing noise intensity, and then decreases for noise strengths exceeding the optimal window. Further, it was observed that varying the threshold (or bias) allowed the system to morph the output into different logical operations. This concept, named "logical stochastic resonance" (LSR) has led to much recent research, spanning both basic aspects of the interplay between noise and nonlinearity, and applied problems such as design of flexible logic gates with enhanced performance [1–7]. The relevance of LSR has been established in physical systems, ranging from electrical [2,4] and nanomechanical [3] to optical systems [5,6]. It has also been found to occur in chemical [7] and biological [8] scenarios.

Now we examine the possibility of "noise-free LSR," by driving a two-state system with periodic forcing instead of random noise. The central question is this: if the driving is completely regular, such as sinusoidal forcing or a periodic train of pulses, would we still observe LSR? Namely, is noise a necessary ingredient of LSR?

Here we will demonstrate how noise-free LSR is indeed possible, i.e., we will show that when a nonlinear bistable system is presented a low amplitude input signal, consisting of (aperiodic) pulses encoding logic inputs, accompanied with periodic forcing, the state of the system accurately and consistently mirrors the output of a logic gate. We also show how one can reconfigure the type of logic response obtained by variation of a readily adjustable bias. Further, this concept can be potentially used to recover LSR-like response in situations where noise is suboptimal.

First we lay out the general principle. Consider a nonlinear system under periodic forcing:

$$\dot{x} = F(x) + b + I + Df(\omega t), \tag{1}$$

where $F(x)$ is a generic nonlinear function obtained via the negative gradient of a potential with two distinct stable energy wells at x_+ and x_-. The bias b has the effect of asymmetrizing the two potential wells. I is the low amplitude input, typically aperiodic, signal. The functional form of the periodic forcing is f, with ω being the frequency and D being the amplitude (intensity) of the forcing.

A logical input-ouptut association (cf. Table I) can be obtained by feeding the system with an input signal $I = I_1 + I_2$, where I_1 and I_2 are two (aperiodic) trains of square pulses encoding the two logic inputs. Without loss of generality, consider the inputs to take value 0.5 when the logic input is 1, and value -0.5 when the logic input is 0. The logic inputs being 0 or 1, produce four sets of binary inputs (I_1, I_2): (0,0), (0,1), (1,0), and (1,1). These four distinct input conditions give rise to three distinct values of I. Hence, the input signal $I = I_1 + I_2$, is a three-level aperiodic wave form.

The *logic output* is determined by the state x, and can be defined by a threshold value x^*, obtained from the position of the barrier between the two potential wells. If $x > x^*$, i.e., when the system is around the potential well x_+, then logic output is 1. The logic output is 0 if $x < x^*$, i.e., when the system is in the other well. Thus the output toggles as the state of the system switches between wells.

We now explicitly demonstrate noise-free LSR, under sinusoidal forcing, for a system with cubic nonlinearity:

$$\dot{x} = 2x - 4x^3 + b + I_1 + I_2 + Df(\omega t), \tag{2}$$

where $f(\omega t) = \sin(\omega t)$.

This particular nonlinear function, $F(x) = 2x - 4x^3$, is efficiently realized by a linear resistor, linear capacitor, and a small number of complementary metal-oxide-semiconductor (CMOS) [9] transistors [2], and is capable of operating in very high frequency regimes [10]. Further, such a system may be implemented with integrated circuits and nanoelectronic devices.

For this system the threshold value x^*, defining the output, is 0. So, we interpret the state $x > 0$ as logic output 1 and $x < 0$ as logic output 0. Alternately, complementary gates can be obtained by interpreting the output as 1 when $x < 0$, and as 0 when $x > 0$.

The response of the system under different angular frequencies of sinusoidal forcing is displayed in Fig. 1. Interestingly

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TABLE I. Relationship between the two inputs and the output of the fundamental OR and AND logic, and the complementary NOR and NAND logic operations. All possible logical circuits can be constructed by combining the NOR (or NAND) gates [11].

Input set (I_1,I_2)	OR	AND	NOR	NAND
(0,0)	0	0	1	1
(0,1)/(1,0)	1	0	0	1
(1,1)	1	1	0	0

we observe, that in order to produce a robust logical combination of the inputs, the system requires an appropriate forcing frequency, which is neither too small nor too large. Namely, for a given value of bias b and amplitude of forcing D, we get the desired logical output *only for some suitable range of* ω.

Note that by simply changing the bias we can easily switch to another logic operation. In this case, when bias b is changed from 0.5 to -0.5, we morph from OR logic to AND logic. This is clearly evident from the timing sequences displayed in Fig. 2. This effect arises from the change in the symmetry and depths of the potential wells due to changing b. The complementary logic gates, namely, NOR and NAND, can be straightforwardly obtained by the alternate output interpretation.

We can quantify the consistency of obtaining a given logic output as follows: first we calculate the probability of obtaining the desired logic output for different sets of input, i.e., the ratio of the number of successful runs (namely, a run where the desired logic output is obtained) to the total number of runs. We then define a very stringent measure P reflecting the reliability of the system as a logic gate: when the probability defined above is ~ 1 (i.e., when the logic operation is correctly obtained for all given input sets) we take P to be 1, and 0 otherwise. Namely, partial success, where certain combinations of inputs fail to give the correct logic output, leads to $P = 0$, since we want the logic response to be obtained for *all* random combinations of inputs. From the point of view of applications, anything less is not useful, and our measure of successful gate operation P reflects this stringent requirement.

Figure 3 shows the variation of P for logic operations AND and OR with respect to drive frequency. It is clearly evident that we obtain a window of angular frequency for which our system consistently gives the desired logic response as output, i.e., for $\omega_{\text{low}} < \omega < \omega_{\text{high}}$ the system yields perfect gate operations. Forcing at angular frequencies lower than ω_{low} acts like a quasistatic "signal," akin to a bias, as the time scale of the drive is too slow and does not vary much vis-à-vis the natural time scale of the system. Frequencies larger than ω_{high} do not achieve the desired response, as the drive then varies so fast that the system effectively responds to an averaged force field.

Further, we observe in Fig. 4 that by increasing the amplitude of sinusoidal forcing (D) the optimal window we get for ω, widens and shifts to the higher end. Namely, the lower and upper thresholds of optimal angular frequency (ω_{low} and ω_{high}) increases for increased value of D.

In order to demonstrate the generality of our results, we now drive the system with a periodic rectangular wave form,

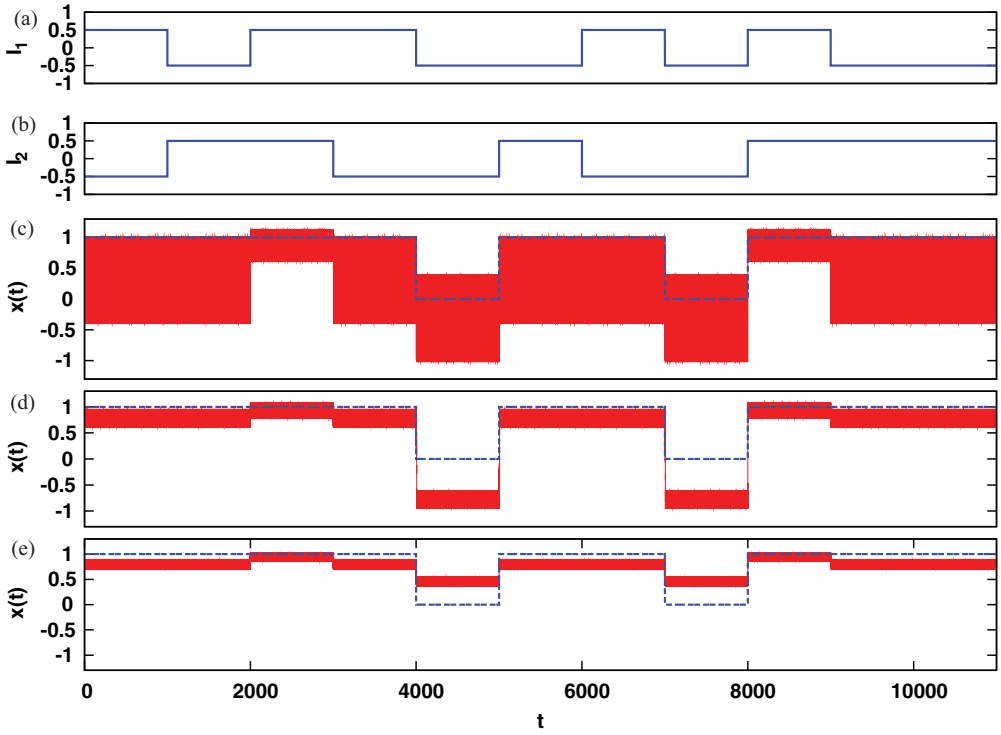

FIG. 1. (Color online) Panels top to bottom show (a) streams of inputs I_1 and (b) I_2 (which take value -0.5 when logic input is 0 and value 0.5 when logic input is 1), and output $x(t)$ for forcing frequencies [cf. Eq. (2)]: (c) $\omega = 2$, (d) $\omega = 10$, and (e) $\omega = 20$. Here, $b = 0.5$ and $D = 2$. The dashed blue line in panels (c)–(e) indicates the expected OR logic output (with state $x > 0$ being logic output 1, and $x < 0$ being logic output 0). Clearly, only when $\omega = 10$, do we get the desired OR gate consistently.

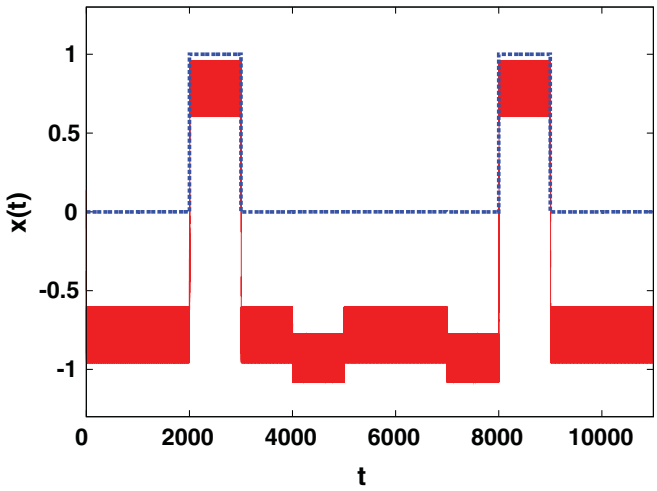

FIG. 2. (Color online) Wave form of $x(t)$ [cf. Eq. (2)] with angular frequency $\omega = 10, b = -0.5$, and $D = 2$. The bold blue line indicates the expected AND logic output. By changing bias b from 0.5 to -0.5, we were able to switch from an OR (cf. Fig. 1) to an AND gate.

and show that this too allows us to obtain a LSR-like response. So consider the system in Eq. (2) above, now forced with a rectangluar wave, where $f(\omega t)$ switches periodically between the values 1 and -1, with time period $T = 2\pi/\omega$, where ω is the angular frequency, D is the amplitude of rectangular pulse, and b is the asymmetrizing bias. In this system too, we observe that reliable logic output is obtained for intermediate frequencies.

Further it is evident from Fig. 4 that driving with rectangular pulses is more efficient, as the system can function as a logic gate for lower amplitudes D, as well as over larger ranges of forcing frequencies for fixed D. We also investigated the logic response under increasingly low input strengths. We found that rectangular forcing allows logic behavior for lower input strengths than sinusoidal forcing, again demonstrating the efficiency of driving with rectangular wave forms.

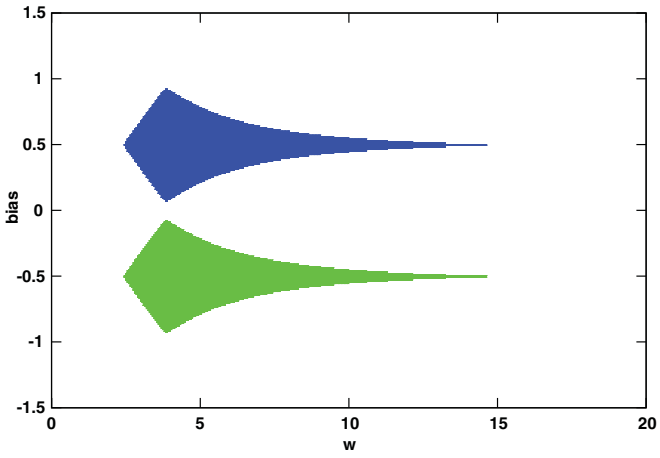

FIG. 3. (Color online) The shaded areas indicate where the probability P of obtaining the OR (top blue) and AND (bottom green) logic operations is 1, as functions of angular frequency (x axis) and bias (y axis). In both cases, $D = 2$.

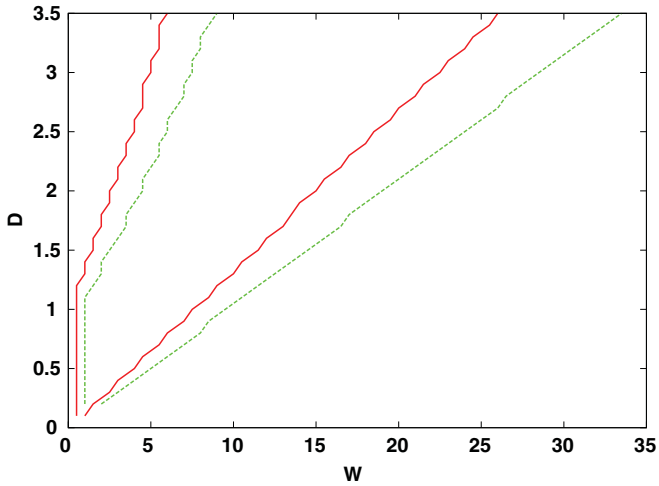

FIG. 4. (Color online) The curves indicate the limiting forcing frequencies ω_{low} and ω_{high}, for varying amplitude D, for sinusiodal forcing (red solid line) and rectangular forcing (green dashed line). Here $b = 0.5$ and the probability of obtaining the OR logic operation (leaving small transience after the switching of inputs) is 1 for the values of D and ω lying between the two lines, i.e., the lines mark the highest and lowest forcing frequencies yielding robust logic for different forcing amplitudes (and analogously the highest and lowest driving amplitudes for different frequencies).

In the examples above, we have thus shown that noise is not a necessary condition to obtain a consistent logic response. It is possible to have phenomena completely analogous to LSR, without noise. So the forcing that induces the desired hopping in response to inputs does not have to be random noise, but can be a sine wave or even a cyclic set of pulses. The system needs only appropriate pushes sufficiently often, in order to change its state to the desired well. The time scale of the forcing is crucial, while its form can range from noise to sinusoidal forcing or rectangular pulses.

An explanation for the optimal band of frequencies is obtained by examining the time taken by the system to cross over the barrier from the bottom of the wells under the input signal encoding the logic inputs (0,1) or (1,0), which is the most difficult and sensitive case to satisfy consistently. The inverse of this time is analogous to the Kramer's rate representing the characteristic escape rate from a stable state of a potential, and determines the band of forcing frequencies and amplitudes that allow robust logic response. Now, in order to obtain a consistent logic response, the system must simultaneously satisfy certain conditions. First, the driving frequency should be more than the frequency at which the stream of inputs switch. Secondly, for a fixed value of amplitude D, the following has to be ensured: when the input signal encodes the logic input set (0,1) or (1,0) (i.e., $I = I_1 + I_2 = 0$), the system should be in the appropriate well. For instance, for OR logic, under net zero input signal the system should be in the higher well. So it should be able to cross the barrier from the lower to the upper side. At the same time, the reverse crossing should not occur. These two conditions set the two limits on forcing frequency (see Fig. 5).

Further, the forcing frequency should not be so high that the system is unable to respond to it, i.e., the time for which

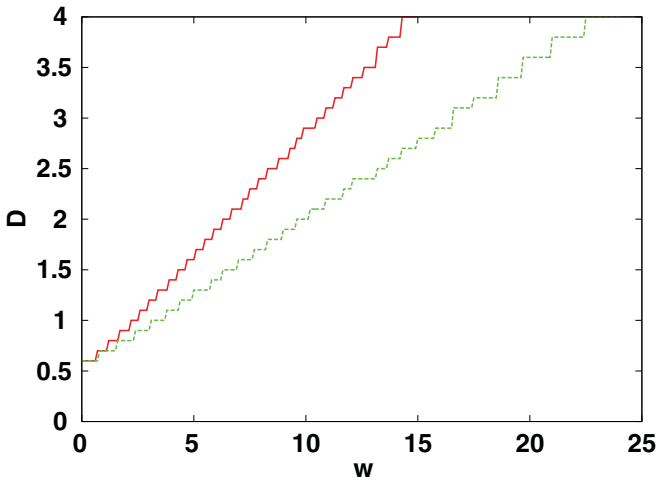

FIG. 5. (Color online) Lines indicating the limiting forcing frequencies for which the system crosses the barrier, when driven by a rectangular wave of amplitude D. Specifically for all frequencies ω and amplitudes D above the lines, the system crosses over with probability 1, within 100 time steps, from upper to lower well (solid red line), and from lower well to upper well (dashed green line). Here bias $b = 0.5$ (appropriate for OR logic) and input signal $I = 0$ [namely, encoding logic input set $(1,0)/(0,1)$]. The area inside these curves gives the allowed forcing frequency and amplitude band, as it allows crossing from the lower to the upper well, but not the reverse. These curves mirror the ones displayed in Fig. 4.

the driving force pushes the system in the requisite direction should be more than the time that the system takes to shift from one well to other. The amount of time taken by the system to cross over to the desired well in response to a new input signal, namely, the transience (which determines latency), should also be sufficiently high so that the system has enough time to make the passage. Further, for very low frequency forcing, the system may have long transience as the transient period must include at least one full cycle of forcing.

Lastly, we present the realization of these results in electronic circuit experiments. In Fig. 6, the analog simulation circuit for Eq. (2) is depicted. The input sinusoidal signal is denoted as $f(t)$. The amplitude of the sinusoidal signal is fixed at $2V$ and the frequency values range from 500 Hz to 30 KHz. $I(t)$ corresponds to logic input signal $(I_1 + I_2)$, where the logic

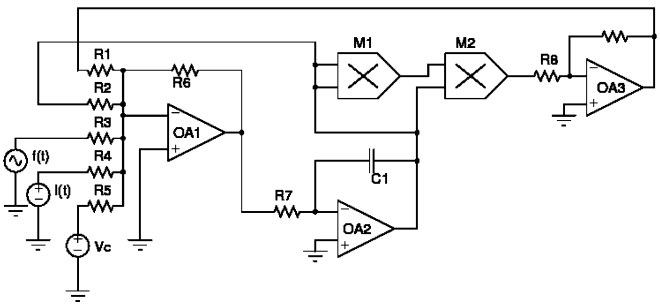

FIG. 6. Circuit diagram: here OA1, OA2, and OA3 are operational amplifiers (AD712). $M1$ and $M2$ are analog multipliers (AD633). The resistor values are fixed as $R1 = R3 = R4 = R5 = R6 = R8 = 100\,\mathrm{k}\Omega$. $R2 = 50\,\mathrm{K}\Omega$, $R7 = 10\,\mathrm{K}\Omega$, and $R9 = 400\,\mathrm{k}\Omega$. The capacitor value is fixed as $C1 = 0.01\ \mu\mathrm{F}$.

input signals I_1 and I_2 take value -0.5 V when logic input is 0 and value 0.5 V when logic input is 1. The bias voltage V_c corresponds to bias b in Eq. (2). We set V_c equal to 0.5 and -0.5 V for the different logic operations. The output node voltage (V_O) of operational amplifier OA2 corresponds to $x(t)$ of Eq. (2).

Representative results of circuit realizations of sinusoidal forcing are displayed in Fig. 7. Comparison with Fig. 1 clearly shows that the same phenomenon is observed in these experiments. Namely, only with sinusoidal forcing with moderate frequency, equal to 10 KHz, do we get the desired logic gate operation reliably.

In summary, we have explicitly shown through numerics and circuit experiments, that it is possible to obtain a logic response similar to LSR, without the presence of noise. Using only a periodically driven bistable system, we are able to produce a logical combination of two inputs streaming in any random sequence. For very small or very large forcing frequencies the system does not yield any consistent logic output, but in a wide band of moderate frequencies the system produces the desired logical output very reliably. Furthermore, the logic response of the system can be easily switched from one logic gate to another by varying the bias in the system. Thus it is evident that noise-free LSR indeed exists, and noise is not a necessary ingredient to facilitate changes of state that reliably mirror logical outputs.

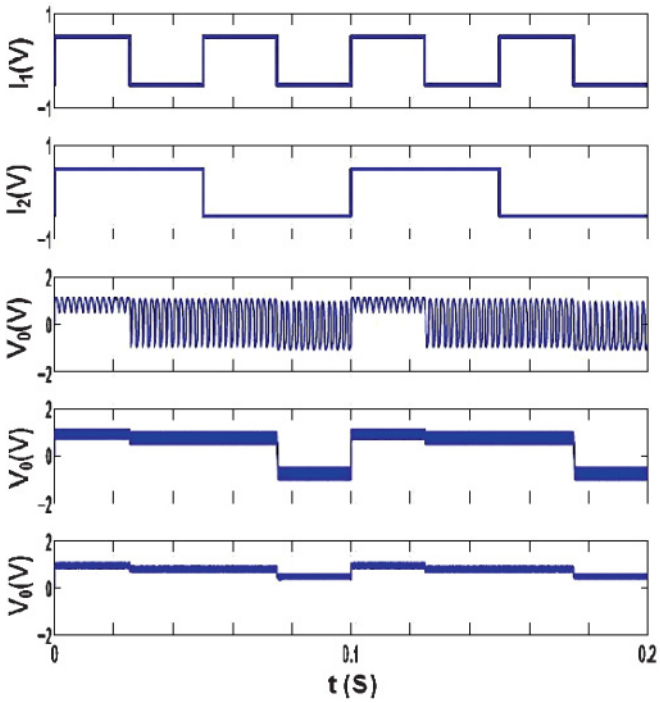

FIG. 7. (Color online) From top to bottom: panels (a) and (b) show streams of inputs I_1 and I_2, which take value -0.5 when logic input is 0 V and value 0.5 V when logic input is 1; panels (c)–(e) show the wave forms of the output voltage, with angular frequencies: $\omega = 2$ KHz, $\omega = 10$ KHz, and $\omega = 20$ KHz. Here, $b = 0.5$ V and $D = 2$ V. The bold blue line indicates the expected OR logic output. Clearly, only when $\omega = 10$ KHz, do we get the desired OR gate consistently.

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[9] CMOS is widely used for constructing integrated circuits, microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for certain analog circuits such as image sensors, data converters, and highly integrated transceivers used for communication. Since CMOS devices have very low static power consumption, they are used extensively in VLSI (very large scale integration) chips.

[10] The equations are dimensionless. For instance, it is shown in Ref. [2] that x corresponds to voltage scaled by maximum voltage, and t is scaled by RC.

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