Emergent noise-aided logic through synchronization

Manaoj Aravind* and P. Parmananda
Department of Physics, Indian Institute of Technology Bombay, Powai, Mumbai 400 076, India

Sudeshna Sinha
Indian Institute of Science Education and Research Mohali, Knowledge City, SAS Nagar, Sector 81, Manauli, Punjab, PO 140 306, India

(Received 3 October 2021; accepted 24 November 2021; published 14 December 2021)

In this article, we present a dynamical scheme to obtain a reconfigurable noise-aided logic gate that yields all six fundamental two-input logic operations, including the XOR operation. The setup consists of two coupled bistable subsystems that are each driven by one subthreshold logic input signal, in the presence of a noise floor. The synchronization state of their outputs robustly maps to two-input logic operations of the driving signals, in an optimal window of noise and coupling strengths. Thus the interplay of noise, nonlinearity, and coupling leads to the emergence of logic operations embedded within the collective state of the coupled system. This idea is manifested using both numerical simulations and proof-of-principle circuit experiments. The regions in parameter space that yield reliable logic operations were characterized through a stringent measure of reliability, using both numerical and experimental data.

DOI: 10.1103/PhysRevE.104.064207

I. INTRODUCTION

Exploiting the richness in the behavior of nonlinear dynamical systems for computational tasks has attracted extensive research interest. Various theoretical schemes have been proposed to realize reconfigurable devices using the rich patterns in chaotic systems and varied experimental implementations of these schemes have been been realized [1–3].

An interesting recent line of enquiry is the effect of noise in such schemes. This approach is crucial as this leads to the possibility of noise-aided computational devices that can utilize noise to facilitate computing. Logical stochastic resonance (LSR) [4–15] is one such scheme in which a bistable system driven by a subthreshold stream of inputs can generate responses consistent with a desired logical operation for an optimal window of noise. This again has been implemented in a wide variety of experimental systems [5,16–19] that range from synthetic gene networks [20–25] and optical systems [26,27] to Coulomb coupled quantum dots [28]. More recent efforts have focused on using chaotic attractor hopping [29,30] and strange nonchaos [31,32] to yield logic gates.

The effect of coupling on such noisy bistable systems has garnered new interest [33,34]. Coupling induced LSR [35] demonstrated that logic operations may be obtained from the state variable of coupled bistable systems in an optimal window of noise.

In this work, we show a possibility that the logical output can be embedded in a collective state of the coupled system, rather than in the state variable of one of the subsystems. This change leads to a rich construct, which can yield all two-input logic operations for an optimal window of noise strength and coupling strength.

II. SCHEME

Consider coupled bistable systems with two kinds of coupling schemes defined as follows (refer Fig. 1):

$$\begin{aligned} \dot{x_1} &= F(x_1) + c(x_2 - x_1) + I_1(t) + b + D\,\eta_1(t), \\ \dot{x_2} &= F(x_2) + c(x_1 - x_2) - I_2(t) - b + D\,\eta_2(t) \end{aligned} \tag{1}$$

and

$$\begin{aligned} \dot{x_1} &= F(x_1) + c(-x_2 - x_1) + I_1(t) + b + D\,\eta_1(t), \\ \dot{x_2} &= F(x_2) + c(-x_1 - x_2) + I_2(t) + b + D\,\eta_2(t). \end{aligned} \tag{2}$$

Here, F can be any nonlinear function that yields a bistable potential. The terms η_1 and η_2 are two uncorrelated, zero mean, univariate Gaussian noises of noise strength D. The drive signals I_1 and I_2 are two low amplitude (subthreshold) input streams that encode the two binary inputs to the system. A constant asymmetrizing bias b acts as the tether that morphs the bistable potential, leading to reconfigurability in our scheme. In the above equations, two kinds of coupling terms have been used. In Eq. (1), the coupling between the two subsystems is bidirectional and attractive in nature with coupling strength c. This typical diffusive kind of coupling interaction [36] tends to synchronize the subsystems; i.e., in the context of bistable systems, the two subsystems are pulled to the same potential well. In Eq. (2), the coupling interaction is bidirectional and repulsive in nature. This form of coupling repels the states of the subsystems, thus tending to antisynchronize the subsystems [34,37,38]; i.e., for bistable systems, the subsystems are pushed to different potential wells. Thus Eq. (1) describes *attractive coupling* and Eq. (2) describes

*Corresponding author: manaojaravind@iitb.ac.in

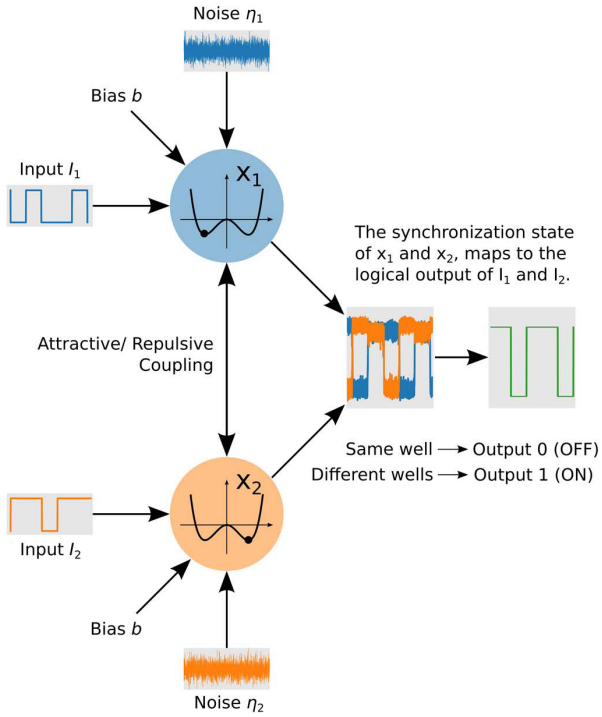

FIG. 1. Schematic representation of the concept.

repulsive coupling. In conjunction with the bias b, we demonstrate that changing between these two coupling forms offers another degree of control that allows us to obtain all six fundamental logic operations (cf. Table II).

The signals I_1 and I_2 encode the stream of binary inputs to be processed by the logic gate, where without loss of generality I_1(or I_2) <0 corresponds to a 0 (OFF state) and I_1(or I_2) >0 corresponds to a 1 (ON state). It is important to note that these input signals are subthreshold, i.e., they cannot cause a transition between the potential wells on their own and the transitions are actively facilitated by the noise floor, reminiscent of logical stochastic resonance (LSR). The crucial differentiating factor of this scheme from all previous attempts to achieve noise-aided logic operations is that the output from the system is embedded in the collective state of the coupled system. Specifically, the synchronization state of the two subsystems embeds outputs corresponding to logical operations on the input streams. As a convention, the synchronized state (both systems in the same potential well) is taken to encode 0 and the antisynchronized state (both systems in different potential wells) is taken to encode 1. The binary input output relations represented by the six fundamental two-input logic gates are detailed in Table I. With these conventions in place, we now show that this scheme is capable of producing all the six fundamental logic operations in a robust, reliable manner over a large region of parameter space.

III. IMPLEMENTATION

The scheme is first implemented in silico, by numerically simulating Eqs. (1) and (2) using the Euler-Maruyama method. For the bistable potential, we use the simple cubic function $F(x_i) = 4(x_i - 5x_i^3)$. The input signals I_1 and I_2 are taken to assume the values -0.5 for the binary input 0 and $+0.5$ for binary input 1. The time trials of the system variables x_1 and x_2 thus obtained are depicted in Fig. 2 for various values of noise strength D, coupling strength c, and bias b. In this figure, the top two panels show the input streams I_1 (blue) and I_2 (orange) being fed into the two subsystems and the expected logical output (green) of these inputs for each of the six logic operations are overlaid on the time trails as a visual aid to perceive the correct logical operation. For the six cases depicted, the time trails of x_1 and x_2 constantly alternate between the synchronized and antisynchronized states modulated by the input streams. As defined earlier, the logical output is considered 0 when the two state variables are in the same potential wells (synchronized) and 1 when the state variables are in the opposite potential wells (antisynchronized). From Fig. 2 it is apparent that robust logic operations are obtained at specific parameter values and coupling forms, for all six types of logic gates.

Next we construct a proof-of-principle electronic implementation of the scheme. Two piecewise-linear bistable circuits were built, using simple passive components and two operational amplifiers (op-amps) as depicted in Fig. 3. The detailed description and characterization of the bistable circuit used can be found in Ref. [39]. The two bistable units were coupled attractively via a resistor as shown in Fig. 3(a) or repulsively via inverting amplifiers as shown in Fig. 3(b). The inputs and bias to the bistable system are fed through the inverting input of the op-amps; hence the signals and biases were inverted to stay consistent with the scheme description and the numerical exploration. The nondimensionalized form of the coupled equation governing the circuits in Fig. 3(a) (attractively coupled circuit) and Fig. 3(b) (repulsively coupled circuit) assumes the form described in Eq. (1) and Eq. (2), respectively, where F of the bistable unit is given by the piecewise linear function

$$F(x_i) = \begin{cases} -(x_i + 1), & x_i < -0.5, \\ x_i, & -0.5 \leqslant x_i \leqslant 0.5, \\ -(x_i - 1), & x_i > 0.5 \end{cases} \tag{3}$$

TABLE I. Relationship between the two inputs and the output of the fundamental OR, AND, NOR, NAND, XOR, and XNOR operations, for the four distinct possible input sets (0,0), (0,1), (1,0), and (1,1).

Input set (I_1, I_2)	OR	AND	NOR	NAND	XOR	XNOR
(0,0)	0	0	1	1	0	1
(0,1)/(1,0)	1	0	0	1	1	0
(1,1)	1	1	0	0	0	1

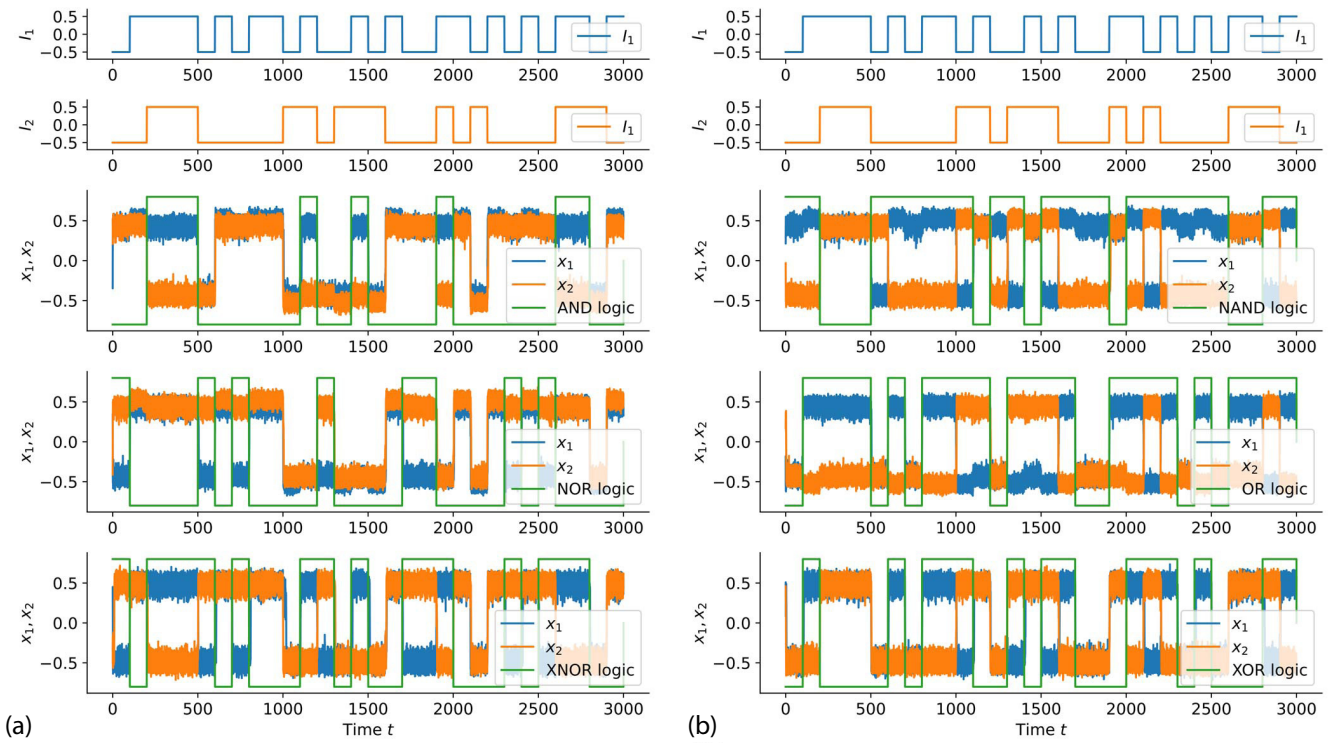

FIG. 2. Top two panels show the input streams I_1 and I_2 that take the value -0.5 when the logic input is 0 and $+0.5$ when the logic input is 1. The bottom three panels depict the time series of the state variables x_1 (blue) and x_2 (orange) obtained from the numerical simulation of (a) the attractive coupling scheme [cf. Eq. (1)] and (b) the repulsive coupling scheme [cf. Eq. (2)]. The expected logic output (green) corresponding to each logic operation is plotted over the time series as a visual aid. When x_1 and x_2 are synchronized, the output is interpreted as 0; when x_1 and x_2 are antisynchronized the outputs are interpreted as 1. Panel 3 shows AND logic operation in the attractive scheme and NAND logic operation in the repulsive scheme for noise strength $D = 0.2$, coupling strength $c = 1.2$, and bias $b = 0.5$. Panel 4 shows NOR logic in the attractive scheme and OR logic in the repulsive scheme for $D = 0.2$, $c = 1.2$, and $b = -0.5$. Panel 5 shows XNOR operation in the attractive scheme and XOR operation in the repulsive scheme for $D = 0.25$, $c = 0$, and $b = 0$.

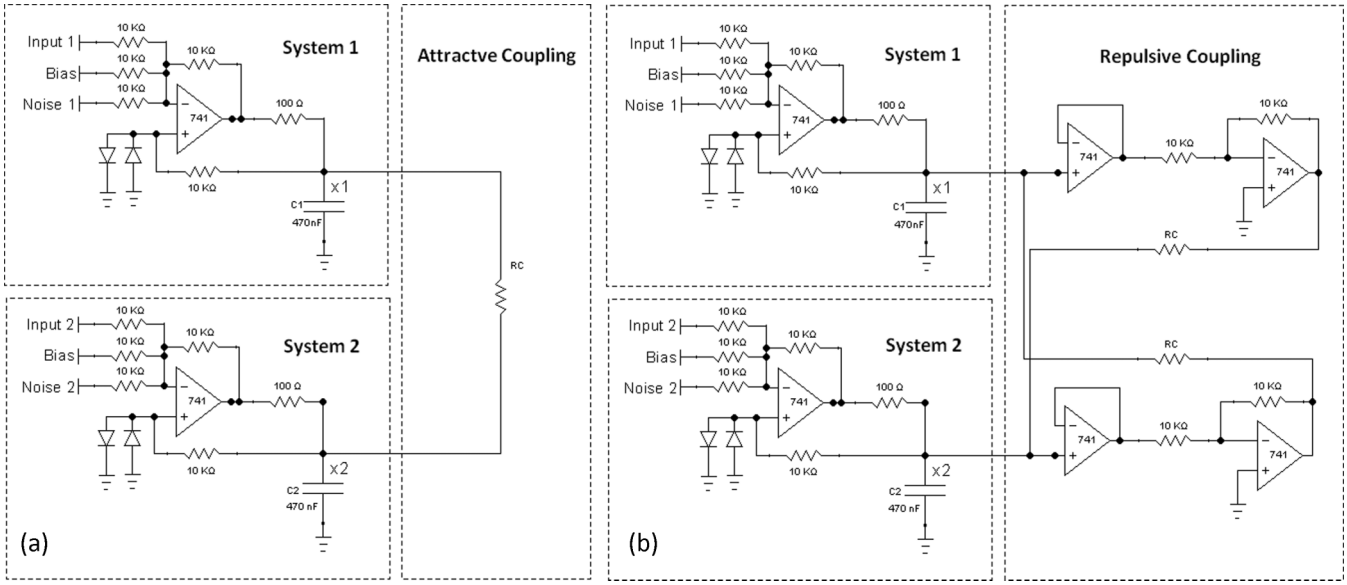

FIG. 3. Schematic circuit diagram of (a) the attractively coupled system represented by Eqs. (1) and (3). (b) The repulsively coupled system represented by Eqs. (2) and (3). All component values are indicated in the diagram. The diodes used in the circuit are 1N4148 diodes. Both systems are studied for two values of coupling resistances $R_C = 300\ \Omega$ and $R = 10\ \mathrm{K}\,\Omega$. The system variables x_1 and x_2 in Eqs. (1) and (2) are proportional to the voltages V_1 and V_2 across the capacitors C_1 and C_2.

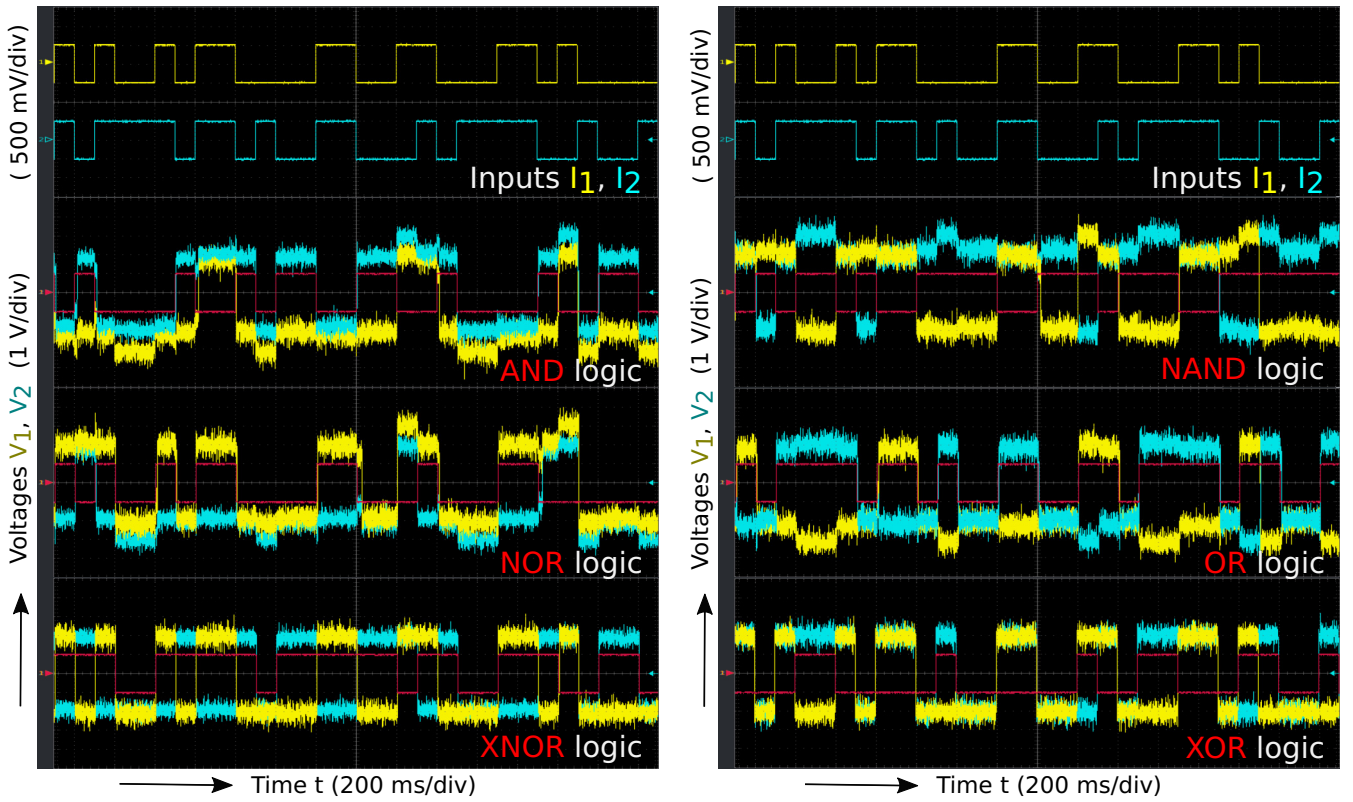

FIG. 4. Top panels on both sides are the oscilloscope trace of the logic input signals used to drive the circuits. Left: oscilloscope traces of the voltages V_1 (yellow) and V_2 (blue) across capacitors C_1 and C_2 of the attractive circuit [cf. Fig. 3(a)]. The expected logical output for each logic gate is presented (in red) as a visual aid. Panel 2 shows AND logic operation obtained for bias $b = 400$ mV, noise strength $D = 0.55$ V, and coupling resistance $R_C = 300\ \Omega$. Panel 3 shows NOR logic for $b = -400$ mV, $D = 0.55$ V, and $R_C = 300\ \Omega$. In panel 4, XNOR logic is obtained for $b = 0$ mV, $D = 0.45$ V, and $R_C = 10$ K Ω. Right: oscilloscope traces of V_1 (yellow) and V_2 (blue) from the repulsive circuit [cf. Fig. 3(b)]. Panel 2 shows NAND logic operation is obtained for bias $b = 400$ mV, noise strength $D = 0.55$ V, and coupling resistance $R_C = 300\ \Omega$. Panel 3 shows OR logic is obtained for $b = -400$ mV, $D = 0.55$ V, and $R_C = 300\ \Omega$. In panel 4, XOR logic is obtained for $b = 0$ mV, $D = 0.45$ V, and $R_C = 10$ K Ω.

and where the state variables x_1 and x_2 are proportional to the voltages V_1 and V_2 across the capacitors C_1 and C_2. The time trails of the experimental systems were obtained using a Tektronics 2104B Digital Storage Oscilloscope. A high speed data acquisition device (Measurement Computing USB-1616HS) was used to both generate signals (I_1, I_2, η_1, η_2) and collect high throughput voltage data (V_1, V_2) for further analysis. All signal generation and data collection were done at a rate of 2×10^4 samples per second. All specific component values used in the construction of the circuit are indicated in the circuit schematic (cf. Fig. 3).

In Fig. 4 oscilloscope trails of V_1 (yellow) and V_2 (blue) obtained from the attractive circuit (left) and repulsive circuit (right) are presented. The top panel shows the input streams (I_1 and I_2) driving the coupled system, while the remaining six panels clearly show robust logic response akin to the behavior observed in Fig. 2. The expected logic output of the input streams are again overlaid (in red) as a visual aid. The synchronized segments faithfully map to the output 0, while the antisynchronized segments map to 1 for all six logical operations.

The attractive and repulsive coupling schemes yield three logic gates each. The attractive scheme yields AND, NOR, and XNOR gates, while the repulsive scheme yields NAND, OR, and XOR gates. Notice that the two schemes yield complementary logic operations for the same set of parameter values, suggesting that these two coupling schemes are symmetric counterparts of one another. Within a specific coupling form, the value of the constant bias b (positive, negative, or zero) determines the logical operation obtained from the system. The bias ranges and the coupling forms where each of the six logic operations occur are detailed in Table II.

TABLE II. Logic operations obtained for the various coupling schemes and bias b values.

	Positive bias	Negative bias	Zero bias
Attractive coupling	AND	NOR	XNOR
Repulsive coupling	NAND	OR	XOR

IV. MEASURE OF RELIABILITY

Robust operation of the scheme has been demonstrated using both simulation and experiment for a stream of inputs,

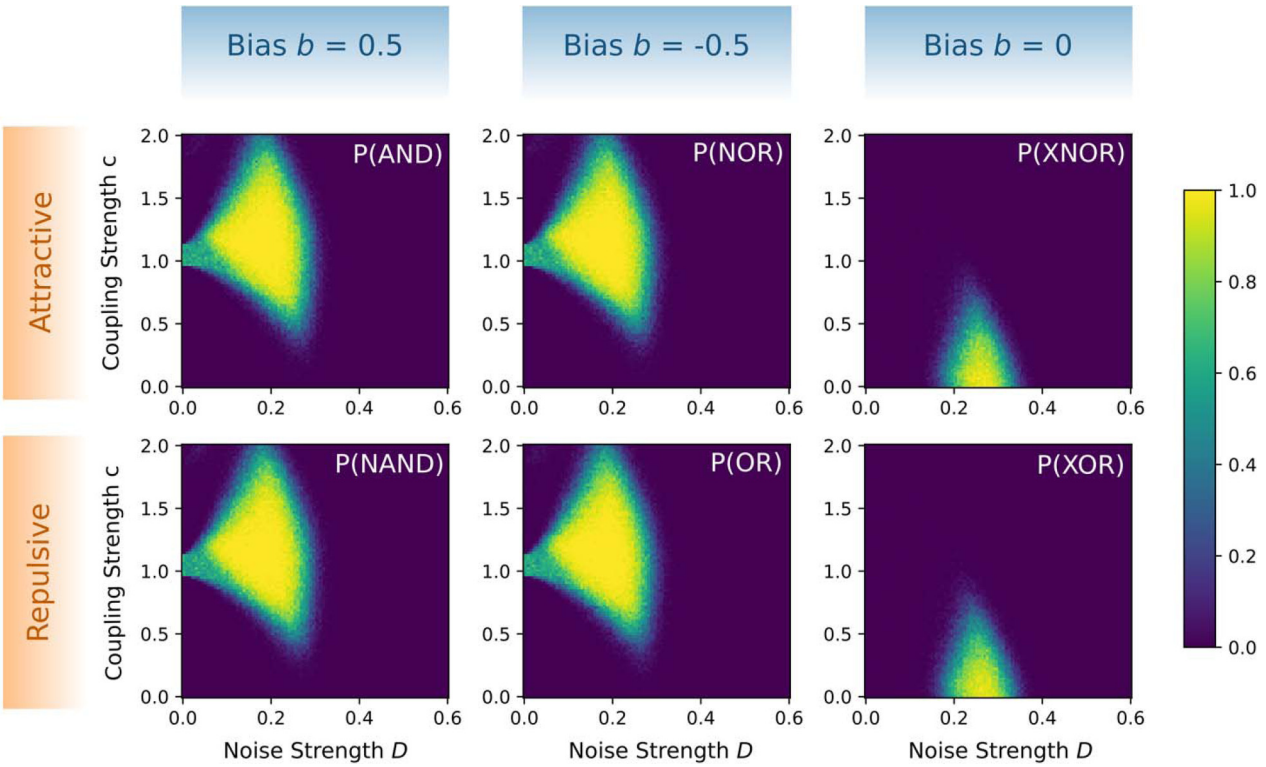

FIG. 5. Probability of obtaining reliable logic operations $P(logic)$ for all six fundamental logic operations [P(AND), P(NOR), etc.] is plotted as a function of noise strength D and coupling strength c. The plots are made for both attractive and repulsive coupling schemes at three specific values of bias b, depicting broad regions in parameter space where all six logic operations are consistently obtained.

with specific values of system parameters. The performance of this system is now quantified with a large number of input sets over a significant section of the parameter space. To do this, the system is subject to a large number of $(I_1 - I_2)$ sets, divided into runs where each run consists of a permutation of the four input sets (0,0), (0,1), (1,0), and (1,1) and the response of the systems to these inputs are recorded. A run is considered successful only if the system produced the correct logical output (corresponding to each truth table; cf. Table I) throughout the run time of each signal pulse for all four input sets. The probability of obtaining a specific logic operation $P(logic)$ is then defined as the ratio of successful runs to the total number of runs sampled. A small transient time amounting to one-tenth the duration of each input pulse is allowed for the system to respond to each new input set. The $P(logic)$ corresponding to specific logic operations are denoted as P(AND), P(XOR), etc. This measure is then obtained for a large range of parameter values to ascertain the prevalence of reliable logic operations.

In Fig. 5, numerically obtained probabilities of obtaining different logic gates are plotted for a range of noise strengths D and coupling strengths c. In these simulations the $P(logic)$ was determined by subjecting the system to 100 runs as described earlier, for each combination of parameter values. Reliable logic operations were seen to occur in large sections of parameter space where the $P(logic)$ value tends to 1 (bright yellow regions in Fig. 5). The probability plots were made for each of the six logic operations at the corresponding coupling scheme and bias b values mentioned in Table II. Thus we see that, for a window of optimal noise strengths and coupling strengths, all logic operations can be obtained. The coupling form and bias b act as the control to morph the coupled system from one logic operation to the other. Note that, contrary to coupling induced LSR [35], where robust logic occurs for all values above a critical coupling strength, we find an optimal range of coupling strengths yield reliable logic operations.

To further strengthen this assertion, we also obtain the *same stringent measure* of reliable operations $P(logic)$ from the experimental implementation of the scheme. This was made possible by interfacing and voltage data analysis through the high speed DAQ. The experimental circuits were driven by an input stream containing 100 runs with a permutation of the four input sets (0,0), (0,1), (1,0), and (1,1) in every run. Again, $P(logic)$ is obtained from the ratio of successful runs to total number of runs sampled. The inputs were fed into the system at 10 Hz (10 binary inputs per second) and again one-tenth of that pulse width was allowed as transient and was not included in the computation of $P(logic)$. Experimentally, two values of coupling resistances were studied: $R = 300\Omega$ and $R = 10$ K Ω. The distribution of $P(logic)$ thus obtained for all the six logic gates is shown in Fig. 6. A clear maximization of reliable logic operations occurs for a broad window of noise strength D for all the logic operations. Surprisingly, contrary to the numerical exploration, experimentally we find a more robust and broad region of XOR and XNOR operations. Note that the XOR/XNOR operations were the hardest to

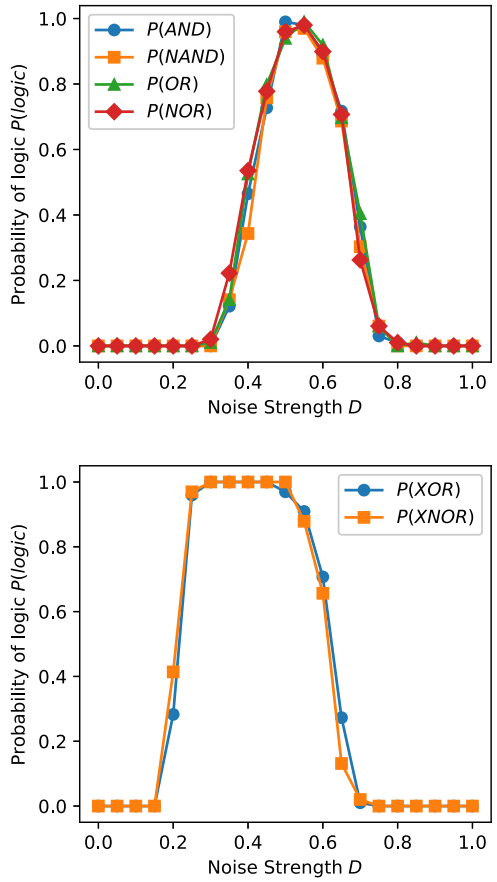

FIG. 6. Probability of logic $P(logic)$ calculated from experimentally obtained voltage data, plotted as a function of noise strength D. Top: for coupling resistance $R_C = 300\ \Omega$, $P(\text{AND})$ and $P(\text{NAND})$ logic plotted for bias $b = 400$ mV. $P(\text{NOR})$ and $P(\text{OR})$ are plotted for $b = -400$ mV. Bottom: for coupling resistance $R_C = 10\ \text{K}\,\Omega$, $P(\text{XNOR})$ and $P(\text{XOR})$ logic plotted for bias $b = 0$ mV.

implement in the past, and their realization necessitated the use of more complicated triple well potentials [40], where specific output definitions were assigned for each logic operation. Here, the multiple gates emerge from the collective dynamics of the coupled system and the binary outputs are inferred from their synchronization state.

V. CONCLUSION

A scheme to make reconfigurable noise aided logic gates, based on synchronization of coupled nonlinear systems, was introduced. This scheme was implemented both through numerical simulations and electronic experiments. The robustness of the logical operations and the reconfigurability of the scheme was elucidated for both attractive and repulsive coupling. A quantitative measure of performance was used to characterize the region in parameter space of coupling strength and noise strength where reliable logic operations can be obtained. This was done both in simulations and in circuit experiments through live collection and processing of high throughput voltage data. Importantly, all six fundamental logic operations were reliably obtained, using a bias and the coupling form to morph between the logic functionalities. So our results suggest the potential of exploiting synchronization, arising from the interplay of noise and the nature of coupling, to implement flexible logic gates in the presence of a noise floor.

ACKNOWLEDGMENTS

The authors gratefully acknowledge the discussions with Dr. K. Murali, Anna University, Chennai, which helped shape the experimental implementation of the repulsive coupling scheme used in this work.

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