Nanoscale x-ray imaging of circuit features without wafer etching

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Modern integrated circuits (ICs) employ a myriad of materials organized at nanoscale dimensions, and certain critical tolerances must be met for them to function. To understand departures from intended functionality, it is essential to examine ICs as manufactured so as to adjust design rules ideally in a nondestructive way so that imaged structures can be correlated with electrical performance. Electron microscopes can do this on thin regions or on exposed surfaces, but the required processing alters or even destroys functionality. Microscopy with multi-keV x rays provides an alternative approach with greater penetration, but the spatial resolution of x-ray imaging lenses has not allowed one to see the required detail in the latest generation of ICs. X-ray ptychography provides a way to obtain images of ICs without lens-imposed resolution limits with past work delivering 20–40-nm resolution on thinned ICs. We describe a simple model for estimating the required exposure and use it to estimate the future potential for this technique. Here we show that this approach can be used to image circuit detail through an unprocessed 300-μm-thick silicon wafer with sub-20-nm detail clearly resolved after mechanical polishing to 240-μm thickness was used to eliminate image contrast caused by Si wafer surface scratches. By using continuous x-ray scanning, massively parallel computation, and a new generation of synchrotron light sources, this should enable entire nonetched ICs to be imaged to 10-nm resolution or better while maintaining their ability to function in electrical tests.

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I. INTRODUCTION

Understanding the as-manufactured structure of integrated circuits (ICs) is important for a variety of reasons. It can allow one to explain or predict departures from the intended circuit performance for reasons ranging from manufacturing process variation to insertion of unintended functionality by outside manufacturers [1]. It can also be used to gain insight into the functionality of obtained ICs for which documentation of their design or functionality is unavailable [2]. Electron microscopy is the main method used for this purpose today. Transmission electron microscopy (TEM) offers atomic resolution on sufficiently thin structures; however, the mean free path for inelastic scattering of 200-keV electrons in silicon is about 0.1-μm [3], and plural electron-scattering limits the achievable spatial resolution to about 30–50 nm when imaging micrometer-thick circuitlike structures using high angle dark-field methods [4]. As a result, TEM can be used to

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view small preselected regions for which the silicon has been substantially thinned, but this approach cannot be extended to larger areas without risk of breakage and/or alteration of electrical properties. TEM and scanning electron microscopy (SEM) can also be used to view specific cross sections obtained using sectioning or focused ion-beam milling, but this is necessarily destructive to IC function. Delayering approaches where the chip surface is repeatedly imaged in a scanning electron microscope after successive layers of the IC have been removed by etching [2] can be used to reconstruct an entire three-dimensional (3D) profile of the circuit; however, the IC is again destroyed in the process, and there are also complications due to different etch rates in different material types.

Transmission x-ray microscopy offers important capabilities that complement the above by allowing one to examine whole unetched ICs. The mean free paths of 10-keV x rays in silicon are about 6 mm for elastic and 40 mm for inelastic scatterings [5,6], so neither multiple elastic nor inelastic scattering should affect the quality of the images of circuit features in 0.2–0.4-mm-thick silicon wafers. These advantages of x-ray microscopy for imaging integrated circuits have long been clear, and x-ray microscopes have been used to image electromigration-induced failures in thinned circuitlike structures [7,8] as well as actual circuits [9]. These demonstrations used Fresnel zone plate optics with a spatial resolution of about 30–40 nm. Although higher-resolution optics have been demonstrated [10], extention to the resolution required for modern integrated circuits while maintaining high efficiency and throughput at multi-keV energies is challenging due to limitations in high aspect ratio electron-beam nanofabrication.

X-ray ptychography offers an alternative approach whereby a focusing optic is used to provide a small coherent beam spot through which the IC is scanned, and a pixelated x-ray detector is used to collect coherent diffraction patterns over an angle well beyond the numerical aperture of the focusing optic [11,12]. When using iterative phase retrieval methods [13], the overlap of the successive coherent illumination spots leads to robust reconstruction of the object from these diffraction patterns [14,15] at a resolution given not by the focusing optic but by the maximum scattering angle at which strong signal is recorded. This approach has been used for 40-nm resolution ptychographic imaging of integrated circuits of unspecified wafer thickness using 15.25-keV x rays [16,17]. High quality 40-nm resolution images of nearly millimeter-sized fields of view have been obtained using 6.2-keV x rays [18] on integrated circuit regions within which the silicon substrate was thinned down to 40 μm, and 2.15-keV x rays have been used for imaging $\sim$10-μm areas of micrometer-thick IC regions at 20-nm resolution [19]. However, thinning chips over larger areas presents challenges in fragility when handling an IC, and it compromises heat removal if the chip undergoes subsequent functional testing. Therefore it would be desirable to extend this approach to imaging unthinned wafers while also improving the spatial resolution to meet the challenges of ever-finer-linewidth IC fabrication. We demonstrate here the ability to image unthinned integrated circuits based on working at 10-keV x-ray energy and an improvement in spatial resolution to better than 20 nm.

In this paper, we first consider the theoretical relationship between exposure and resolution for imaging features in an IC in Sec. II. We then describe the experimental setup and parameters used for IC imaging in Sec. III. In Sec. IV, we describe our results for imaging a complementary metal-oxide semiconductor (CMOS) IC before and after its back surface has been mechanically polished, whereas in Sec. V we describe our results for imaging a dynamic random access memory (DRAM) chip where dimple polishing has been applied. We then end with concluding comments in Sec. VI.

II. CALCULATION OF REQUIRED PHOTON EXPOSURE

X-ray interactions at multi-keV energies are well described by a complex refractive index of $n = 1 - \delta - i\beta$ where the quantities δ and β can be calculated from well-established tabulations [20]. This refractive index leads to Lambert-Beer law attenuation of a beam by a factor of $1/e \simeq 0.367$ at a thickness of $\mu^{-1} = \lambda/(4\pi\beta)$. The strongest image contrast is provided by differences in the phase-shift part of the refractive index δ between silicon and other materials; this can be exploited in Zernike phase contrast [21], differential phase contrast [22], and coherent-scattering-based x-ray imaging methods, such as ptychography (as discussed above). For completeness, we also consider absorption contrast (abs) (which is weaker) in what follows.

To estimate the photon exposure required, we calculated the normalized image intensity I_f in areas containing feature material (20-nm-thick copper) versus the intensity I_b in areas containing background material (20-nm silicon), including absorption in an overlying thickness of silicon and copper as described in Fig. 1. The Zernike phase contrast image intensities were calculated [23] assuming a nonabsorptive phase ring. With these intensities and the assumption that limited photon statistics set the noise limit with a Gaussian approximation to the Poisson distribution, the number of photons $\bar{n}$ per pixel required for imaging a feature against a background with a given signal-to-noise ratio (SNR) [24] is found from

$$\bar{n} = \frac{\mathrm{SNR}^2 |I_f - I_b|^2}{I_f + I_b}. \tag{1}$$

It is conventional to use the Rose criterion of SNR = 5 based on studies of human image perception [25]. Calculations of this type have been widely used in x-ray microscopy with good correlation with experimental conditions.

In order to obtain an estimate of the number of x-ray photons $\bar{n}$ required for imaging fine features in an IC, we carried out a calculation using both phase and absorption contrasts and Zernike phase contrast. For absorption contrast (abs) in the thin specimen limit with the Rose criterion, Eq. (1) can be shown to lead to an expression of

$$\bar{n}_{\mathrm{abs}} \simeq \frac{25}{8\pi^2} \frac{\lambda^2}{t^2} \frac{1}{|\beta_f - \beta_b|^2} \exp[2\mu_{\mathrm{overlayer}} t_{\mathrm{overlayer}}], \tag{2}$$

where t is the thickness of a feature within a background material of the same thickness and the overlayer material is assumed to be uniform with no additional image contrast other than absorption. Similarly, an expression for Zernike phase contrast [23] (zpc) in the thin feature limit and ignoring absorption in the Zernike phase ring can be written as

$$\bar{n}_{\mathrm{zpc}} \simeq \frac{25}{8\pi^2} \frac{\lambda^2}{t^2} \frac{1}{|\delta_f - \delta_b|^2} \exp[2\mu_{\mathrm{overlayer}} t_{\mathrm{overlayer}}]. \tag{3}$$

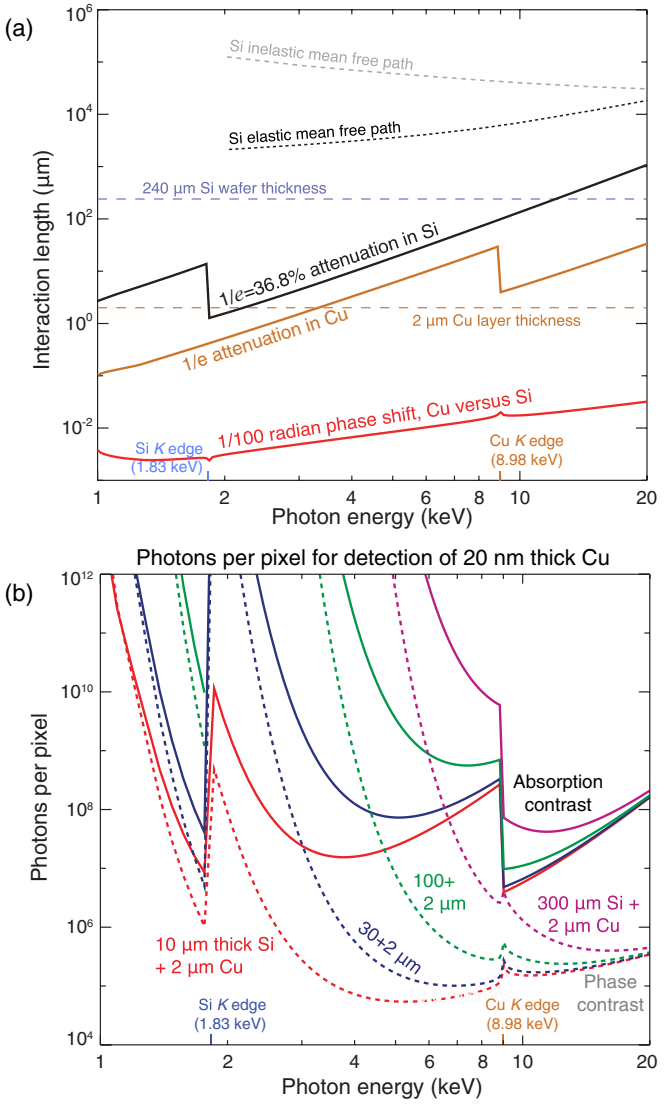

FIG. 1. Multi-keV x rays are well suited to image circuit features in whole unthinned silicon wafers. A plot (a) of the $1/e$ x-ray attenuation length μ^{-1} in silicon (Si) as well as in copper (Cu) shows that 10-keV x rays have reasonable transmission even through 240 μm of Si and 2 μm of Cu. This plot also shows the thickness $t_\phi = \lambda/(200\pi|\delta_f - \delta_b|)$ through which one obtains a 1/100 rad phase-shift difference (detectable in phase contrast imaging methods); this is given for the phase-shifting parts of the x-ray refractive index of δ_f for the feature (Cu) and δ_b for the background material (Si), respectively. Finally, the mean free paths for elastic and inelastic scattering of x rays in silicon are shown at the top, indicating that neither multiple elastic scattering nor inelastic scattering should affect image quality through 200–300-μm-thick silicon wafers. At the bottom (b) an estimate of the number of photons required per resolution element if one is trying to image 20-nm-thick copper features in various overall thicknesses of silicon is shown, based on absorption and phase contrast imaging and a signal-to-noise ratio of 5:1. As can be seen, x-ray photon energies of 6–15 keV offer high contrast and sufficient penetration with 10–15 keV being favored for silicon wafer thicknesses of 200 μm or more.

Although these thin-specimen-approximation limit estimates are useful, we carried out a numerical calculation with no approximations to obtain the results shown in Fig. 1(b) as a function of photon energy as well as wafer thickness. Given an overlayer material of 240-μm Si and 2-μm Cu, Eq. (1) gives a result of an 8.4×10^5 photons per resolution element required for phase contrast imaging of 20-nm Cu features using 10-keV x rays.

Taken together, the interaction length and exposure calculations shown in Fig. 1 suggest that x-ray photon energies of 6–15 keV offer attractive characteristics for IC imaging and that at 10 keV one should be able to image IC features through an entire unthinned silicon wafer thickness.

III. EXPERIMENTAL DETAILS

X-ray ptychography data were acquired using the Bionanoprobe (Zeiss, Inc.) at beamline 21-ID-D at the Advanced Photon Source (APS) at Argonne National Laboratory [26]. Figure 2(d) shows a schematic of our experimental approach. An undulator x-ray source was spectrally filtered using a double-crystal Si ⟨111⟩ monochromator and spatially filtered by the use of upstream apertures of 30-μm width at 37.8-m distance in the horizontal and 1000-μm height at 37.3-m distance in the vertical. This illumination spot was then focused using a Fresnel zone plate with an outmost zone width of 70 nm to produce a 100-nm radius coherent beam spot, and a Pilatus 300K detector (Dectris, Inc.) with 619 × 487 pixels of 172-μm pixel size was placed 2.0 m downstream to collect the coherent diffraction patterns. The zone plate had a diameter of 160 μm, and we estimate the transverse coherence width of the illumination at the plane of the zone plate to be about 156 μm so the zone plate is illuminated by a high degree of partial coherence. We also used a reconstruction algorithm that can account for partial coherence in the probe function as noted later in this section.

The ICs were scanned through the focus spot with continuous motion during each raster line for increased efficiency of beam utilization [27,28], and diffraction patterns were collected for every 70 nm of motion with an exposure time of 30 ms over that distance, yielding an areal exposure of 2.6×10^3 photons/nm^2. Since the calculation described in Sec. II estimated that 8.4×10^5 photons per resolution element would be required for imaging 20-nm Cu features with 240-μm Si and 2-μm Cu overall using 10-keV photons, scaling from Eq. (1) leads to an expectation that a spatial resolution of about $\sqrt{(8.4 \times 10^5 \text{ photons})/(2.6 \times 10^3 \text{ photons/nm}^2)} = 18$ nm could be achieved in these conditions.

In Figs. 2(a) and 2(b), we show the average diffraction patterns from the CMOS chip described in Sec. IV and the DRAM data-bit region described in Sec. V. The diffraction patterns suggest that there is measurable signal to spatial frequencies beyond 100 μm^{-1}, corresponding to half-period feature sizes of 5 nm or smaller. The azimuthal average power spectrum of the CMOS chip is shown in Fig. 2(c), which also indicates that there is a scattered signal out to an angle corresponding to a spatial-half-period distance of below 5 nm.

Starting from the set of acquired diffraction patterns, ptychographic image reconstructions were obtained using a computer code employing graphical-processing units for rapid data processing [29]. This code allows one to reconstruct

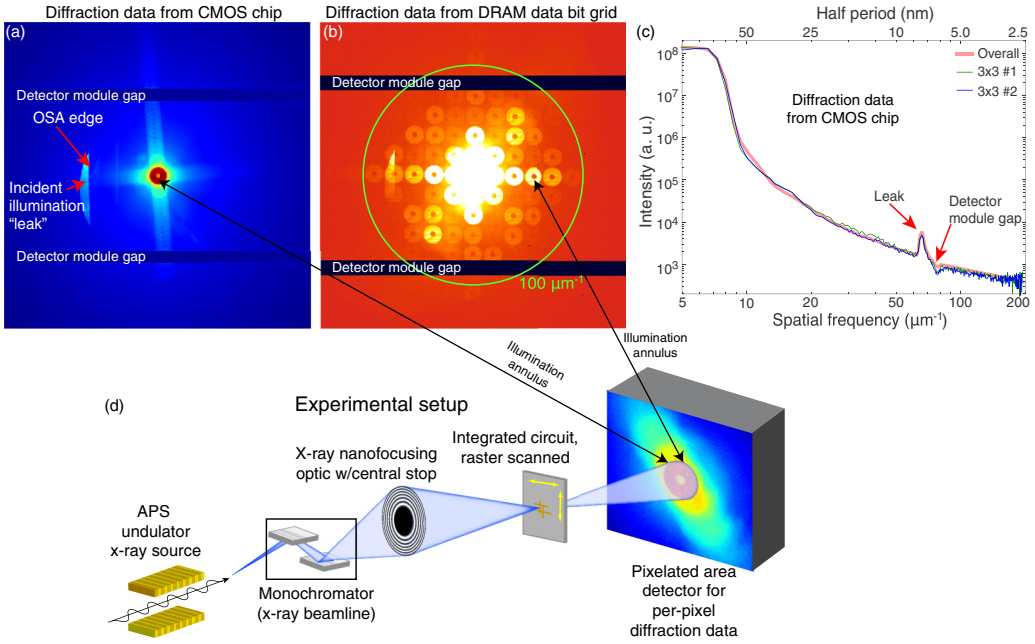

FIG. 2. X-ray ptychography involves the collection of x-ray-diffraction patterns from a scanned focused coherent beam and their reconstruction to yield an image with a resolution finer than the lens focus. In (d) we show a schematic of our experiment where 10-keV x rays were produced by an undulator at the APS at Argonne, monochromatized using Bragg diffraction from a pair of silicon crystals and focused by a Fresnel zone plate with a central stop at a 100-nm radius spot. The integrated circuit was scanned across this spot while coherent diffraction patterns were collected on a pixel array detector extending to an angle well beyond the numerical aperture of the Fresnel zone plate. (a) and (b) are the average diffraction patterns from a CMOS chip and a region of regularly spaced bit cells in a DRAM chip (see the inset of Fig. 5); one can see gaps between active pixel modules in the detector as well as a slight amount of illumination leakage caused by slight misalignment of an order sorting aperture placed between the zone plate optic and the specimen (not shown). The azimuthal average power spectrum of the CMOS chip is shown in (c), both from the average of all illuminated pixels and from two examples of 3×3 illumination spots, such as might overlap upon one specimen feature during our continuous scanning approach [28]. These power spectra suggest that there is measurable signal at spatial frequencies of about 100 μm^{-1}, corresponding to half-period feature sizes of 5 nm or smaller. This is corroborated in (b) where the annular illumination pupil function is replicated over many diffraction orders from the underlying data-bit array periodicity.

both the object and the several individually self-coherent but mutually incoherent probe functions or probe modes [30]. One can therefore obtain high quality images, even though the IC was in continuous motion [27,28,31]. The central 256×256 pixels of the detector data were selected for the reconstruction, yielding a reconstructed image pixel size of 5.6 nm. Because phase contrast is much stronger than absorption contrast at the x-ray energy used, all images shown are phase contrast images from the x-ray ptychographic reconstruction of the IC sample's complex transmission function.

IV. CMOS CHIP WITHOUT AND WITH MECHANICAL POLISHING

The first integrated circuit we examined was a nonproduction CMOS IC fabricated in a 65-nm technology with eight copper interconnect layers. This IC was first imaged with no further processing beyond removal from its IC packaging. As shown in Fig. 3(a), images obtained through the full 300-μm-thick Si wafer easily showed details of the circuit layers, but they also showed an overlay of contrast "stripes" which were elongated in one direction as well as fringes from features at a different plane than that reconstructed. (Ptychography, like other coherent diffraction imaging methods where one recovers an image from diffraction plane magnitudes, tends to reconstruct the optical exit wave at the depth-of-focus-deep plane of maximum contrast [32,33] or separability between the probe and the object functions, but that plane can include information from upstream planes propagated forward or downstream planes propagated backwards).

In order to test the assumption that these stripes were due in part to scratches on the silicon wafer, leading to changes in projected thickness and thus phase contrast, we then mechanically polished the backside of a singulated die to an optical finish. Upon completion of this process, 60 μm of silicon substrate was removed, and the total thickness of the remaining chip was measured to be 240 μm. The IC was then imaged again, leading to the result shown in Fig. 3(b). The image in this case is free of the large stripes shown in Fig. 3(a) so that one can more clearly see a range of wider and finer features in the circuit layer. Note that at 240-μm thickness, after polishing, enough silicon remains for the IC to be quite robust in handling and in heat transfer.

V. DRAM CHIP WITH DIMPLE POLISHING

The second IC we examined was an 8-Gbit SK Hynix DRAM chip which was fabricated on a 32-nm technology node with an initial wafer thickness of 130 μm. In DRAM technology, nodes are defined as one-half the minimum circuit

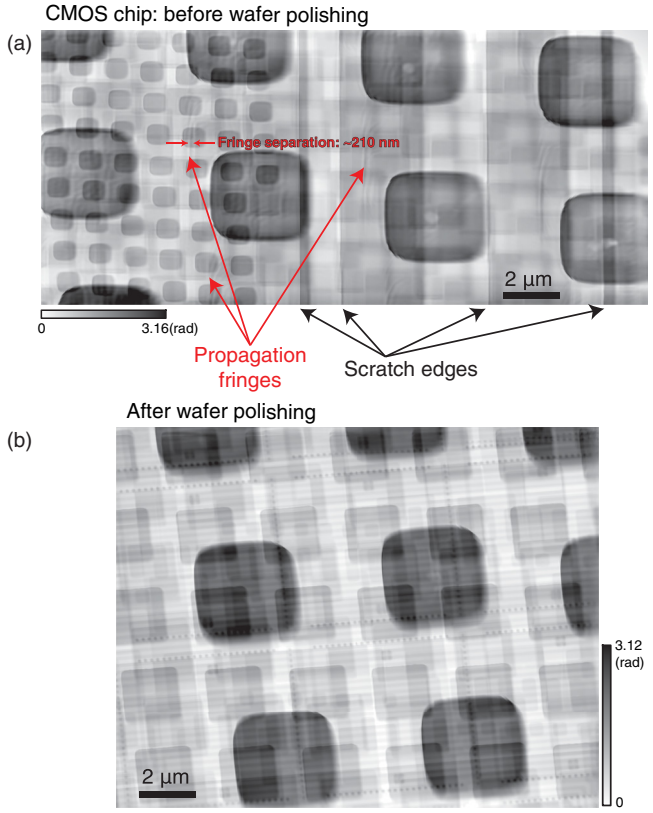

FIG. 3. Ptychographic images of a nonproduction CMOS IC fabricated in 65-nm technology. The image (a) is of this IC as directly removed from its packaging with a wafer thickness of 300 μm. In this case, the image shows an overlay of features at the chip wiring and gate level, along with variations in the overall wafer thickness which are presumably due to scratches on the surface of the wafer. The image also shows some fringes from out-of-focus features at depth planes far from that of the circuit layer; with a 300-μm separation between the front and the back surfaces of the wafer, one would expect these fringes to have a separation scaling, such as $\sqrt{\lambda z} = 193$ nm, which is consistent with what we observe. The image (b) is of a nearby region of the same IC after which it was polished to remove all light-microscope-visible surface scratches; this process reduced the overall wafer thickness to 240 μm but allowed for more straightforward visualization of fine circuit features.

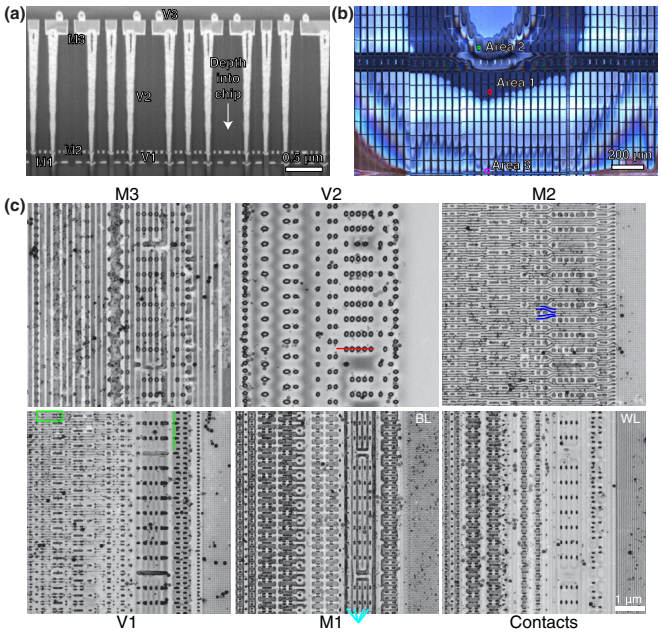

FIG. 4. Light and electron micrographs of a Hynix DRAM IC used for the x-ray ptychographic imaging in Fig. 5. In (a) we show a scanning electron micrograph of a cross-sectional cut into an IC chip; it shows the various metallization layers $M1$, $M2$, and $M3$ as well as the interlayer connection vias $V1$, $V2$, and $V3$. In (b) we show a visible light micrograph of a chip that has undergone a rotation polishing process to remove varying top layers until the bare silicon area was reached (top); the regions imaged using x-ray ptychography (Fig. 5) are indicated with areas 1–3. SEM views of the various layers are shown in (c). Specific features that also are seen in x-ray ptychography (Fig. 5) are indicated with colored markings; the far right area shows word lines (WLs), and the same area also contains bit lines (BLs) for addressing specific DRAM storage bit cells.

unit size so that the word lines in the memory bit cell array have a contact pitch of 64 nm. Figure 4(a) shows a cross-sectional view of the peripheral logic of one of the bit cell arrays from this IC type. The cross sectioning was performed using focused ion-beam milling on a FEI Helios Nanolab Dualbeam system, and the imaging was performed using the SEM column in the same system. In this cross section, one can see that IC has six layer structures: beginning from the bottom, layers $M1$, $M2$, and $M3$ contain metal in-plane wiring, whereas via levels ($V1$, $V2$, and $V3$) connect the metallic lines.

In order to validate our imaging approach, we undertook a comparison of x-ray ptychography with scanning electron micrographs acquired using this SEM. In this case, a D500i Dimpler system from South Bay Technology was used to polish off the top few metal/dielectric layers of the DRAM to expose all the layers locally in one array. The Dimpler uses a felt pad and a polishing slurry (1-μm colloidal silica) to form a gradual depression as can be seen in the visible light micrograph of Fig. 4(b). The various exposed layers were then imaged using the same FEI Helios Nanolab SEM, leading to the views of various metal layers shown in Fig. 4(c).

We selected three regions for x-ray ptychographic imaging: Area 1 contains all but the $M3$ and $V3$ layers, area 2 only contains thin layers which are very close to the silicon substrate, whereas area 3 contains the thicker $V2$ layer and probably some of the $M3$ layer. As can be seen in Fig. 5(a), x-ray ptychography provides an image that is the total projection through the remaining metallization layers so that it can be correlated with the individual layer SEM images of Fig. 4(c). As an example, the darkest spots (tungsten vias) labeled by a red line are from the $V2$ layer, whereas features labeled in blue are from the $M2$ metal layer. The DRAM array region in Fig. 5(a) also shows the overlay between vertical WLs and horizontal BLs used to address individual DRAM bits. The reconstruction from a thinner area (area 2) shows word lines which have a pitch of 64 nm or an individual linewidth of about 32 nm [see Fig. 5(b)]. A subregion was selected from area 3, and the x-ray reconstruction was refined by using additional iterations between the object and the far-field planes with its result shown in Fig. 5(d).

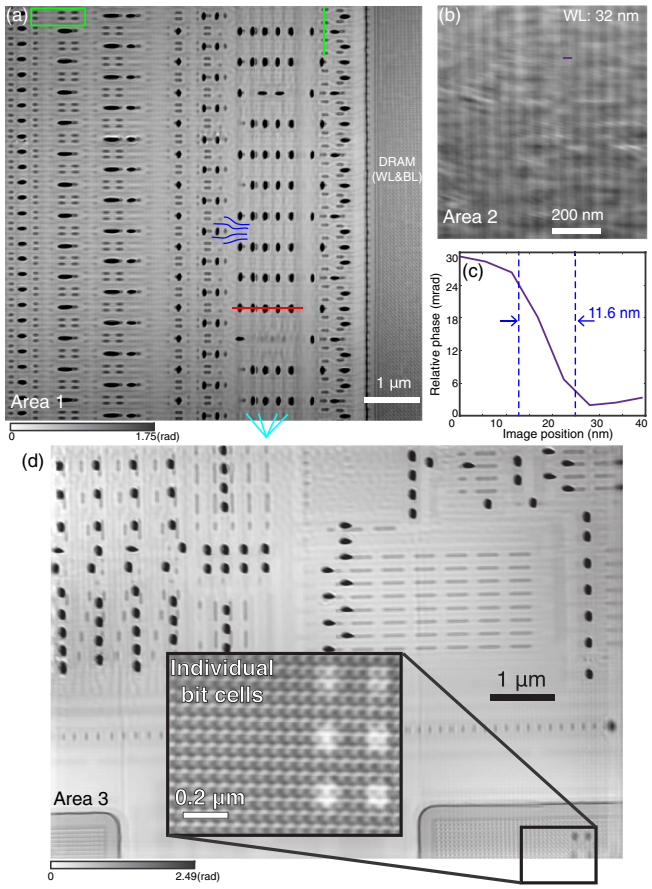

FIG. 5. Continuous-motion scanning ptychography of a Hynix DRAM integrated circuit using 10-keV x rays. In (a), we show a region corresponding to area 1 in the light micrograph of Fig. 4(b), with specific circuit features marked with colored lines to match the equivalent features shown in Fig. 4(c). The region at right shows WLs and BLs used to address specific DRAM memory bit cells. The reconstruction on area 2 that only contains thin layers leads to the image (b) of word lines at a 64-nm pitch or about a 32-nm linewidth. The line profile across an example word line shown in (c) has an edge response (10%–90%) of 11.6 nm, suggesting an image resolution of about $\Delta x = 11$ nm which is consistent with the diffraction data shown in Fig. 2. Note that the reconstructed optical phase change of about 30 mrad is consistent with the expected phase change of $\Delta\varphi = 2\pi(\delta_{\mathrm{Cu}} - \delta_{\mathrm{Si}})\Delta t/\lambda = 29$ mrad for $\Delta t = 50$ nm at 10 keV. Image (d) shows the reconstruction from the region corresponding to area 3 in Fig. 4(b) with individual memory bit cells shown at the bottom; the inset shows a refined reconstruction of that subregion [where the diffraction data are shown in Fig. 2(b)] with individual bit cells visible in transmission through the bottom layers of the whole integrated circuit.

One robust method for evaluating image resolution is to acquire two independent images of the same object and then use a Fourier ring correlation approach to measure the consistence in phase as a function of spatial frequencies within the images [34–36]. Unfortunately, we did not have sufficient allocated experimental time at the APS to acquire two such independent images of the same IC region. However, as indicated in Fig. 2 we observed x-ray diffraction from thin IC features in the DRAM bit region extending out in most angles to spatial frequencies of about 100 $\mu\mathrm{m}^{-1}$, corresponding to half-feature sizes of 5 nm or smaller (the detector module gap in Fig. 2 limits the signal at spatial frequencies of about 80 $\mu\mathrm{m}^{-1}$ in the vertical direction or half-periods of about 6 nm; the incident illumination leak shown in Fig. 2(a) is constant at all scan positions, so it would not lead to an erroneous position-dependent image signal). In addition, as noted in Sec. III the areal exposure we used would lead to an expected resolution of about 18 nm. We note that photon statistics noise can affect the achieved spatial resolution in iterative phase retrieval [37] but simulation studies have shown a consistency between the length scale at which one has an acceptable signal-to-noise ratio and spatial resolution [38]. An alternative direct measure of resolution is obtained by examining the sharpness of specific features in the image. As shown in Fig. 5(c), we were able to see 10%–90% intensity changes from the edges of several word lines in the Hynic DRAM IC over a distance of about 2 pixels; since the reconstruction pixel size is 5.6 nm (as given by the ptychography detector's angular extent) and this suggests a spatial resolution of about $\Delta x = 11$ nm. Combining this measurement with the overall orientation-independent resolution of the x-ray diffraction signal shown in Fig. 2, we can state with confidence that our achieved spatial resolution is better than 20 nm.

The images shown here are only single two-dimensional projections through integrated circuits which show much complexity in 3D. Because x-ray ptychography reconstructs an exit wave that captures both absorption and phase contrast, it is very successful at reconstructing the electron density in the sample with an accuracy of ±5% [39]. Thus, it can be used to distinguish between many of the materials of interest in modern ICs for both metal and nonmetal structures. To untangle the 3D structure of an IC, one can acquire a set of images while the IC is rotated, yielding a set of phase contrast projections which can then be supplied to a standard x-ray tomography algorithm for 3D reconstruction. Such a procedure has been used for x-ray ptychographic tomography with an isotropic spatial resolution of 16 nm [40], although only small regions have been imaged thus far due to both depth of focus limitations (the ptychographic image provides an in-focus pure projection image only through depth volumes equal to a depth of focus limit of about $5(\Delta x)^2/\lambda$ or about 6 μm in our case) and due to the fact that at high tilts one will need to adjust the ptychographic plane focus across the projection. One possible approach for 3D imaging is to start with a 3D model of the IC through which one simulates the x-ray ptychographic tomographic imaging process and adjust the model using optimization techniques. This will be computationally challenging, but it involves well-known physics.

VI. CONCLUSION

We have shown here that x-ray ptychography can be used to image circuit features at sub-20-nm resolution in unthinned integrated circuits ranging up to 240 μm in thickness. This allows one to image chips with no fragility and heat transport limitations imposed by thinning, thus preserving the opportunity for follow-on electrical testing. Because the spatial resolution in x-ray ptychography should in principle improve

with increases in photon exposure because there are no optics-imposed resolution limits and because the x-ray wavelength used is so small ($\lambda = 0.124$ nm in the work shown here), this approach should be able to be extended to image details in future generations of finer-linewidth integrated circuits.

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