Towards Boolean operations with thermal photons

Philippe Ben-Abdallah[*]

Laboratoire Charles Fabry, UMR 8501, Institut d'Optique, CNRS, Université Paris-Sud 11, 2,
Avenue Augustin Fresnel, 91127 Palaiseau Cedex, France
and Université de Sherbrooke, Department of Mechanical Engineering, Sherbrooke, PQ J1K 2R1, Canada

Svend-Age Biehs[†]

Institut für Physik, Carl von Ossietzky Universität, D-26111 Oldenburg, Germany

The Boolean algebra is the natural theoretical framework for a classical information treatment. The basic logical operations are usually performed using logic gates. In this Rapid Communication we demonstrate that NOT, OR, and AND gates can be realized exploiting the near-field radiative interaction in N-body systems with phase change materials. With the recent development of a photon thermal transistor and thermal memory, this result paves the way for a full information treatment and smart solutions for active thermal management at nanoscale with photons.

Controlling heat exchanges at nanoscale is a tremendous challenge for the development of numerous future technologies. During the last decade, thermal analogs of diodes, memories, and transistors have been introduced [1,2] in order to control (switch, modulate, store, and even amplify) the flow of heat and energy carried by phonons in solid elements networks in the same manner as the flow of electrons is controlled in electric circuits. In 2007, thermal logic gates [3] have been proposed to build up thermal logic calculations using the transport of acoustic phonons in lattices of nonlinear solid elements. Recently, to overcome the problems linked to the relatively small speed of acoustic phonons and due to the presence of localized Kapitza resistances inside these lattices, radiative analogs of diodes [4–8], transistors [9,10], memories [11], splitters [12,13], and even electric wire [14] have been proposed for controlling radiative heat currents both in near- and far-field regimes in complex architectures of solids out of contact opening the way to contactless thermal analogs of basic electronic devices. Some of these theoretical concepts—the diode and the memory—have been verified experimentally very recently [15,16].

In this Rapid Communication we introduce the concept of photonic thermal logic gates which use thermal photons instead of electrons to make logical operations. This element is the basic building block for future thermal circuits which implement Boolean functions by performing logical operations on single or several logical inputs in order to produce a single logical output. In a thermal logic gate, a power is supplied to some points of the device which function as inputs to keep them at specific temperatures and to bring another point of the device which functions as the output to a certain temperature level. By defining temperature levels which serve as thresholds to define logical "0" or "1", a truth table can be associated to the inputs and the output to define specific logical operations.

To start, let us consider the simplest logic gate, the NOT gate which implements a logical negation. This operation can be performed by using a three-body system as sketched in Fig. 1(a). It has been shown that this system consists of a thermal reservoir acting as the heat source, an intermediate gate layer made of an insulator-metal transition (IMT) material [17,18], and a second reservoir which serves as a heat drain—a thermal transistor [10]. It has been demonstrated by us [10] that due to the ability of the gate layer to qualitatively and quantitatively change its optical properties through a small change of its temperature around a critical temperature, T_c, the heat flux towards the drain can be switched, modulated, and even amplified. In order to operate the thermal transistor as a NOT gate the temperature of the source is maintained at a fixed temperature T_S. Throughout this Rapid Communication we use $T_S = 360$ K. Then, the intermediate layer functions as the input of the NOT gate and the drain as the output. That means the temperature T_G of the gate layer which is assumed to be smaller than T_S sets the Boolean input of the NOT gate. Here we define the thermal state with $T_G < T_c$ as "0" and the thermal state with $T_G > T_c$ as "1". This state can be set from outside by adding or removing heat from the intermediate gate layer. Finally, since T_S and T_G are fixed by an external reservoir there will be a radiative energy flux Φ_D from the source and the gate towards the drain until T_D has reached a value such that

$$\Phi_D(T_S, T_G, T_D) = 0, \tag{1}$$

i.e., the drain is in its local thermal equilibrium and the system has reached the steady state. Now, we can read out the output temperature T_D which defines the Boolean output of the NOT gate. Here we define the thermal state "0" as the state where $T_D < T_{min}$ and the thermal state "1" as the state where $T_D > T_{max}$ introduces two thresholds T_{min} and T_{max} with $T_{min} < T_{max}$. Here we choose $T_{min} = 342$ K and $T_{max} = 343$ K.

In order to verify if the transistor operates as a NOT gate we need to determine T_D for different input values of T_G by evaluating the roots of Eq. (1). For a system operating in near-field regime (i.e., far-field exchanges with the surrounding can

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*pba@institutoptique.fr

†s.age.biehs@uni-oldenburg.de
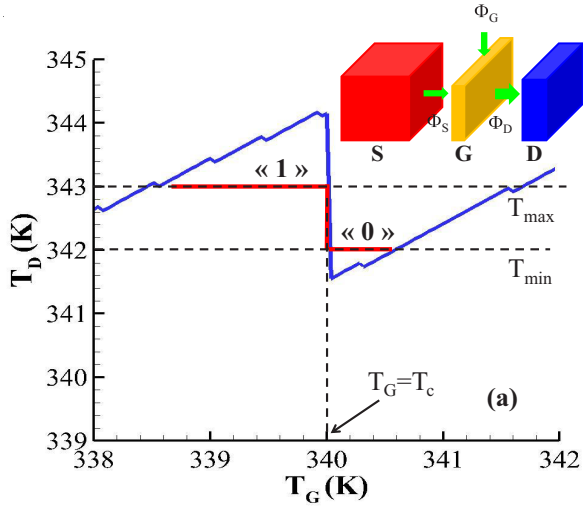
FIG. 1. (a) Radiative NOT gate made with a SiO$_2$/VO$_2$/SiO$_2$ plane thermal transistor. The source (S) is assumed semi-infinite, while the gate (G) and the drain (D) have a thickness of 100 nm. The separation distances are $d = 100$ nm. The temperature T_G of the gate defines the input and the drain temperature sets the gate output. In the operating range of the gate around the critical temperature T_c of the gate, if $T_D < T_{\min}$ the gate is in the thermal state "0". On the contrary, when $T_D > T_{\max}$ the gate is in the state "1". The rectangular function represents the ideal response of the gate in its operating range. (b) Truth table for the ideal NOT gate.

be neglected) the flux received by photon tunneling by the drain reads [19]

$$\Phi_D = \int_0^\infty \frac{d\omega}{2\pi} \, \phi_D(\omega, d), \tag{2}$$

where the monochromatic heat flux is given by

$$\phi_D = \hbar\omega \sum_{j=\{s,p\}} \int \frac{d^2\boldsymbol{\kappa}}{(2\pi)^2} \big[n_{SG}(\omega) \mathcal{T}_j^{S/G}(\omega, \boldsymbol{\kappa}; d) $$
$$+ n_{GD}(\omega) \mathcal{T}_j^{G/D}(\omega, \boldsymbol{\kappa}; d) \big]. \tag{3}$$

Here $\mathcal{T}_j^{S/G} \in [0,1]$ and $\mathcal{T}_j^{G/D} \in [0,1]$ denote the efficiencies of coupling of each mode $(\omega, \boldsymbol{\kappa})$ between the source and the gate and between the gate and the drain for both polarization states $j = s, p$; $\boldsymbol{\kappa} = (k_x, k_y)^t$ is the wave vector parallel to the

surfaces of the multilayer system. In the above relation n_{ij} denotes the difference of Bose-distribution functions n_i and n_j (with $n_{i/j} = [\exp(\frac{\hbar\omega}{k_B T_{i/j}}) - 1]^{-1}$) at the frequency ω; k_B is Boltzmann's constant and $2\pi\hbar$ is Planck's constant. According to the N-body near-field heat transfer theory presented in Ref. [19], the transmission coefficients $\mathcal{T}_j^{S/G}$ and $\mathcal{T}_j^{G/D}$ of the energy carried by each mode written in terms of optical reflection coefficients $\rho_{E,j}$ ($E = $ S,D,G) and transmission coefficients $\tau_{E,j}$ of each basic element of the system and in terms of reflection coefficients $\rho_{EF,j}$ of couples of elementary elements [19]

$$\mathcal{T}_j^{S/G}(\omega, \kappa, d) = \frac{4|\tau_{G,j}|^2 \mathrm{Im}(\rho_{S,j})\mathrm{Im}(\rho_{D,j})e^{-4\gamma d}}{|1 - \rho_{SG,j}\rho_{D,j}e^{-2\gamma d}|^2 |1 - \rho_{S,j}\rho_{G,j}e^{-2\gamma d}|^2},$$

$$\mathcal{T}_j^{G/D}(\omega, \kappa, d) = \frac{4\,\mathrm{Im}(\rho_{SG,j})\mathrm{Im}(\rho_{D,j})e^{-2\gamma d}}{|1 - \rho_{SG,j}\rho_{D,j}e^{-2\gamma d}|^2} \tag{4}$$

introducing the imaginary part of wave vector normal to the surfaces in the multilayer structure $\gamma = \mathrm{Im}(k_z) = \sqrt{\kappa^2 - \omega^2/c^2}$; c is the velocity of light in vacuum. For the detailed expressions of the reflection coefficients we refer to Ref. [19].

By solving the transcendental equation (1) using expression (2) we obtain the results shown in Fig. 1(a). The configuration of the NOT gate used in the numerical calculation is as follows: both source and drain are made of silica [20] where the source is assumed to be semi-infinite and the drain is assumed to have a thickness of 100 nm. The intermediate 100-nm-thick gate layer is made of vanadium dioxide (VO$_2$), an IMT material which undergoes a first-order transition (Mott transition [17]) from a high-temperature metallic phase to a low-temperature insulating phase [18] at a critical temperature T_c which is close to room temperature. Here we assume for convenience that the phase transition happens abruptly at $T_c = 340$ K, which means that we are neglecting the phase transition region between the two phases. As demonstrated in previous works [21–23] below its critical temperature, i.e., for $T_G < T_c$, VO$_2$ supports surface phonon polaritons in the same frequency range as silica. On the contrary, in its metallic phase VO$_2$ does not support surface wave resonances anymore so that the near-field interaction between each element in the system is strongly reduced for $T_G > T_c$. Hence, the coupled silica-VO$_2$ system behaves like a thermal switch [7,10]. This "switching" ability can be seen in Fig. 1(a) when the temperature T_D makes a sudden jump at $T_G = T_c$. Finally, we can see in Fig. 1(a) that for $T_G < T_c$ we have a region where $T_D > T_{\max}$, which means that the input state "0" results in the output state "1". Similarly, for $T_G > T_c$ we have a region where $T_D < T_{\min}$, which means that the input state "1" results in the output state "0". Hence, the here introduced device functions indeed as a NOT gate with the truth table shown in Fig. 1(b). The performance of the here introduced NOT gate is close to the idealized NOT gate performance sketched by the red line in Fig. 1(a).

As a second example we sketch the realization of an OR gate using once again a simple gate thermal transistor. However, contrary to the NOT gate, we choose here phase change materials for both the source and the gate layer and silica for the drain layer. The temperatures of these two elementary parts of the transistor are used as inputs, while the drain
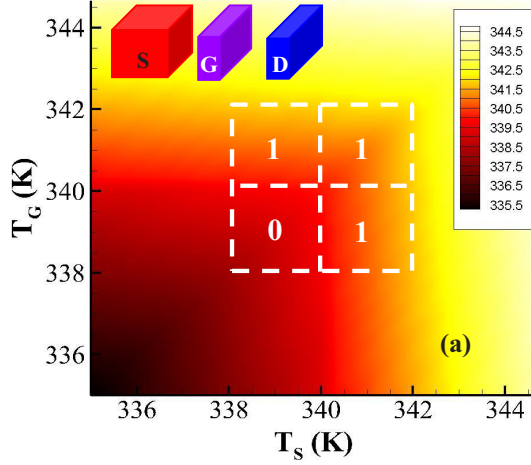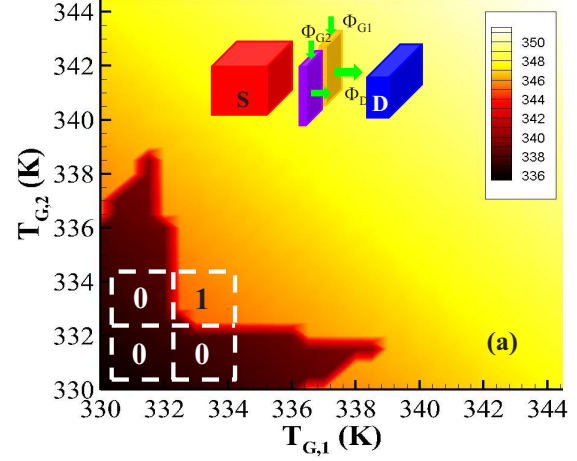
Inputs		Output
T_S	T_G	T_D
$T_S < T_c \leftrightarrow 0$	$T_G < T_c \leftrightarrow 0$	$T_D < T_{min} \leftrightarrow 0$
$T_S < T_c \leftrightarrow 0$	$T_G > T_c \leftrightarrow 1$	$T_D > T_{max} \leftrightarrow 1$
$T_S > T_c \leftrightarrow 1$	$T_G < T_c \leftrightarrow 0$	$T_D > T_{max} \leftrightarrow 1$
$T_S > T_c \leftrightarrow 1$	$T_G > T_c \leftrightarrow 1$	$T_D > T_{max} \leftrightarrow 1$

(b)

FIG. 2. (a) Radiative OR gate made with a VO₂/VO₂/SiO₂ thermal transistor. The source (S) is assumed semi-infinite, while the gate (G) and the drain (D) have a thickness of 100 nm. The separation distances are $d = 100$ nm. The two temperatures T_S and T_G define the inputs and the drain temperature sets the gate output. The operating range of the OR gate is delimited by a dashed rectangular domain centered at $(T_S, T_G) = (T_c, T_c)$ with $T_c = 340$ K. The threshold temperatures are $T_{min} = 337.4$ K and $T_{max} = 339.3$ K (b) Truth table for the ideal OR gate.

temperature sets the output of the logic gate. The temperature evolution of the drain with respect to the temperatures of the source and the gate is plotted in Fig. 2(a). We see that around the point $(T_S, T_G) = (T_c, T_c)$ with $T_c = 340$ K where the phase change occurs both in the source and the gate, the temperature of the drain undergoes a significant variation. If T_S and T_G are both smaller than the critical temperature T_c, then these two elementary blocks behave like a dielectric so that the temperature of the drain is small. On the contrary, if either the source or the gate undergo a phase change, then the temperature of the drain increases abruptly. Hence, by conveniently introducing two suitable threshold temperatures T_{min} and T_{max} it is clear that we can associate to the drain two different thermal states with respect to the temperatures T_S and T_G around the region $(T_S, T_G) = (T_c, T_c)$. Therefore, this transistor behaves like an OR gate with the truth table given in Fig. 2(b). By reversing the definition of thermal states in the drain, it is also clear that this system mimics a NOR gate.

Inputs		Output
T_{G1}	T_{G2}	T_D
$T_{G1} < T_l \leftrightarrow 0$	$T_{G2} < T_l \leftrightarrow 0$	$T_D < T_{min} \leftrightarrow 0$
$T_{G1} < T_l \leftrightarrow 0$	$T_{G2} > T_l \leftrightarrow 1$	$T_D < T_{min} \leftrightarrow 0$
$T_{G1} > T_l \leftrightarrow 1$	$T_{G2} < T_l \leftrightarrow 0$	$T_D < T_{min} \leftrightarrow 0$
$T_{G1} > T_l \leftrightarrow 1$	$T_{G2} > T_l \leftrightarrow 1$	$T_D > T_{max} \leftrightarrow 1$

(b)

FIG. 3. (a) Radiative AND gate made with a double SiO₂ gate thermal transistor, the source being made in SiO₂ and the drain in VO₂. The source (S) is assumed semi-infinite, while both gates (G1, G2) and the drain (D) have a thickness of 250 and 500 nm, respectively. The separation distances are $d = 100$ nm and the gates are assumed isolated one from the other. The color map represents the output T_D with respect to the two input temperatures T_{G1} and T_{G2}, the temperatures of two gates. The operating range of the AND gate is delimited by a dashed rectangular domain centered at $(T_{G1}, T_{G2}) = (T_l, T_l)$ with $T_l = 332.2$ K. (b) Truth table for the ideal AND gate.

Now, we sketch the realization of an AND gate. This double input device is shown in Fig. 3(a). It is a double gate thermal transistor made with two silica gates and a silica source. Contrary to the NOT gate it is the drain which is made of a phase change material. The temperature of both gates sets the two inputs of the logic gate. We assume that the temperature of two gates can now be controlled independently making the assumption, for convenience, that they are thermally insulated one from the other so that we can express the heat flux received by the drain just as the mean value of two NOT gates, i.e., we have

$$\phi_D = \frac{\hbar\omega}{2} \sum_{j=\{s,p\}} \int \frac{d^2\boldsymbol{\kappa}}{(2\pi)^2} \left[n_{SG1}(\omega) \mathcal{T}_j^{S/G1}(\omega, \boldsymbol{\kappa}; d) \right.$$
$$+ n_{G1D}(\omega) \mathcal{T}_j^{G1/D}(\omega, \boldsymbol{\kappa}; d) + n_{SG2}(\omega) \mathcal{T}_j^{S/G2}(\omega, \boldsymbol{\kappa}; d)$$
$$\left. + n_{G2D}(\omega) \mathcal{T}_j^{G2/D}(\omega, \boldsymbol{\kappa}; d) \right]. \tag{5}$$
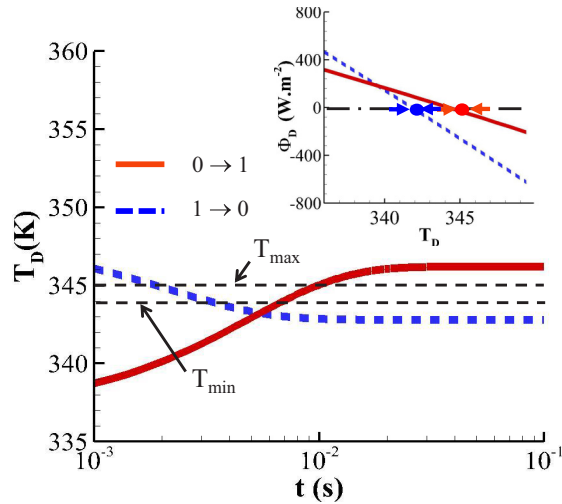
FIG. 4. Thermal relaxation of the drain in a $SiO_2/VO_2/SiO_2$ NOT gate with the geometrical parameters identical as in Fig. 1. The red solid (respectively, blue dashed) line shows the time evolution of the drain temperature from the state "0" (respectively, "0") to the state "1" (respectively, "0") when the initial temperature is $T_D(0) = 337$ K [respectively, $T_D(0) = 348$ K]. The gate temperature is assumed fixed at $T_G = 343$ K (respectively, $T_G = 337$ K) and the consign temperatures are $T_{min} = 344$ K and $T_{max} = 345$ K. The inset shows the stability diagram of solutions for both transitions between the state "0" and the state "1".

Here the transmission coefficients are given by the same expressions as in a single gate transistor. In Fig. 3(a) we show the equilibrium temperature T_D of drain with respect to the gates temperatures T_{G1} and T_{G2}. In the central region around $(T_{G1}, T_{G2}) = (T_l, T_l)$ with $T_l = 332.2$ K we see that T_D can undergo a sudden variation after a short change in the gate temperatures. By introducing two critical temperatures T_{min} and T_{max} we can associate to the drain two thermal states "0" or "1" with respect to the relative value of the drain temperature with respect to these thresholds. As clearly shown in Fig. 3(a) this double gate system behaves as a digital AND gate with the truth table given in Fig. 3(b). Note that by reversing the definition of thermal states "0" and "1" the AND gate becomes a NAND gate.

To finish we evaluate the time required for these gates to switch from one state to another. To this end we study the relaxation process for the drain (100 nm thick) in the $SiO_2/VO_2/SiO_2$ NOT gate described in Fig. 1. The time evolution of the drain temperature from an initial state [set with two different values for $T_D(t = 0 \text{ s})$ corresponding to "0" and "1"] is determined by the nonlinear dynamic

equation

$$\rho C d_D \dot{T}_D = \Phi_D(T_S, T_G, T_D), \tag{6}$$

where ρ, C, and d_D denote the mass density, the heat capacity, and the thickness of the drain, respectively. In Fig. 4 we show the transition dynamic from the state "0" to the state "1" (from the state "1" to the state "0") with an initial temperature $T_D(0) = 337$ K [$T_D(0) = 348$ K] and a gate at fixed temperature $T_G = 343$ K ($T_G = 337$ K). The inset shows the sign of the power received by the drain with respect to its temperature showing, given initial conditions, whether the drain is going to cool down or heat up. The overall time the NOT gate takes to switch from state "0" to state "1" (state "1" to state "0") is a few milliseconds. Note that this switching time is relatively large compared to the operating speed of electric logic gates because of the thermal inertia. For even thicker drains this switching time will increase. Also, generally speaking, the flux exchanged between the different elements in the gates is much more important in the near-field regime than in the far-field regime where the flux is bounded by the blackbody limit. Hence, the working dynamic of gates is much faster in near field than in far field.

To summarize, we have introduced the concept of logic gates for heat radiation by discussing in some detail a realization of NOT, OR, and AND gates operating in the near-field regime. In this work we have limited ourselves to demonstrating the achievability of logical operations with thermal photons in an ideal situation where the phase transition takes place at a fixed temperature. Further works will be needed to properly define the operating range of basic logic gates when the transition occurs over a finite temperature range. The same concepts could obviously be applied in the far-field regime, that is, for separation distances much larger than the thermal wavelength. However, in this regime the magnitude of heat flux is much lower so that the thermalization process is much slower. The main advantage of radiative thermal logic gates is probably not the possibility of some kind of numerical calculation using heat currents instead of electrical currents, because the operation speed is relatively low even in the near-field regime, but rather the possibility to actively control temperature distributions and heat flux in dense complex networks made of solid elements which are out of contact. The implementation of more complex Boolean operations will require, according to the famous De Morgan's law, one to combine various logical gates. However, in the near-field regime this combination cannot be sequential, generally, because of many-body effects which make the heat transport throughout the structure nonadditive. This creates a demand for the development of a general many-body theory in arbitrary solid networks.

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