Electrical tuning of Rashba spin-orbit interaction in multigated InAs nanowires

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Indium arsenide nanowires (NWs) are a promising platform to fabricate quantum electronic devices, among other advantages they have strong spin-orbit interaction (SOI). The controlled tuning of the SOI is desired in spin-based quantum devices. In this study we investigate the possibility of tuning the SOI by electrostatic fields generated by a back gate and two side gates placed on the opposite sides of the NW. The strength of the SOI is analyzed by weak anti-localization effect. We demonstrate that the strength of the SOI can be strongly tuned up to a factor of 2 with the electric field across the NW, while the average electron density is kept constant. Furthermore, a simple electrostatic model is introduced to calculate the expected change of the SOI. Good agreement is found between the experimental results and the estimated Rashba-type SOI generated by the gate-induced electric field.

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I. INTRODUCTION

Recently III-V semiconductor nanowires (NWs) have attracted increasing attention in the field of quantum electronics. The strong spin-orbit interaction (SOI) is an attractive property of indium arsenide (InAs) and indium antimonide (InSb) NWs: it results in a large g-factor, which leads to a large Zeeman-splitting [1–4], it allows us to effectively address spins by electric fields (EDSR) [5,6], furthermore to define new types of quantum bits, so-called spin-orbit qubits [7–9], where the quantum information is stored by coupled spin and orbital degrees of freedom. Very recently, theoretical proposals suggested [10–16] that these one-dimensional NWs are an ideal platform to induce topological superconductivity, and they may host pairs of so-called Majorana bound states, which are key building blocks for topological quantum computation. The strong SOI is also a key ingredient of these Majorana wires. The models assume a Rashba-type SOI, which in combination with a magnetic field leads to the essential locking of the spin and the momentum in the 1D band structure. Several groups have reported the signature of these elusive particles [17–21] as a presence of a zero bias anomaly. Since the experimental conditions needed to reach this topological superconducting state are challenging, it would be highly desirable to have further experimental control parameters to analyze and tune the Majorana wires, e.g., a tunable Rashba SOI strength could give a better insight.

In this paper we demonstrate the tunability of the Rashba SOI strength by means of local gating. We have fabricated InAs NW devices with pairs of local side gates (SGs) [see Figs. 1(a) and 1(b)]. By applying voltages with opposite sign on these two SGs an electrostatic field can be generated. The influence of the electrostatic field on the strength of the SOI is studied via weak antilocalization (WAL) measurements.

WAL arises from interference effects [22,23,23–27], where the time-reversed electron path pairs interfere destructively in zero magnetic field leading to an enhanced conductance. The length of the contributing paths is limited from above by the infimum of the decoherence lengths, such as the phase coherence length or the spin relaxation length. Breaking the time-reversal symmetry of the system, i.e., by applying a magnetic field, suppresses the interference term of the conductance, resulting in a negative magnetoconductance (MC).

If the spin relaxation dominates the phase decoherence, the WAL provides us a tool to study the former effect. The electrons propagating in the presence of an electric field ($\boldsymbol{E}$) sense a wave number ($\boldsymbol{k}$)-dependent effective magnetic field, $\boldsymbol{B}_{\mathrm{SO}}(\boldsymbol{k}) \propto \boldsymbol{E} \times \boldsymbol{k}$ as well, around which the spins of the electrons precess. During each elastic scattering the wave number of the electron and so the effective magnetic field randomly changes, leading to a random-like walk of the spin on the surface of the Bloch-sphere [26]. The characteristic length after which the spin becomes fully randomized is defined as the spin relaxation length [28]. Here we will assume that the SOI-induced spin relaxation dominates the other spin relaxation processes, so the WAL is a measure of the SOI.

WAL has been used to extract the strength of the SOI in InAs and InSb NWs [29–36]. In most of the studies the WAL signal has been investigated in field effect transistor (FET) configuration, where a global back gate (BG) electrode is placed under a silicon oxide layer, which changes the electron density and the electrostatic field in the NW at the same time [29–34]. Other studies introduced a top gate, besides the BG, separated from the NW by a solid electrolyte, PMMA [35], or a HfO_2 layer [36].

The strength of the SOI was also studied in self-assembled InAs quantum dots [37,38] and in quantum dots defined in InAs nanowires [2,5,7,8,39] by measuring the splitting of the anticrossings of the quantum dot levels in magnetic field and by studying the dynamics of electrically driven spin resonance.

Here we report our results on InAs NWs using a new geometry where two SGs are added besides the BG. In this way, similar to the FET structure the BG serves to change the electron density, while the SGs can be used to induce a transverse electric field in the wire by applying opposite voltages without changing the overall electron density.

Here we show that the total SOI strength can be enhanced by a factor of 2, only by applying an electric field in the NW. Furthermore, a simple electrostatic model is introduced which shows that this tuning is consistent with the external field-induced Rashba-type SOI.

II. DEVICE AND METHODS

The InAs NWs were grown by molecular beam epitaxy [40]. After growth, they were deposited onto a thermally oxidized, degenerately doped n-Si substrate from a 2-propanol dispersion. The thickness of the SiO_2 layer is 400 nm and the underlying doped Si layer serves as the global BG electrode. The source (S), drain (D), and SG (SG1 and SG2) electrodes were defined in a two-step e-beam lithography process and were deposited by UHV e-beam evaporation (Ti/Au 10/90 nm), after an Ar ion beam etching to remove the native oxide from the surface of the NW. A false color SEM image of the sample is shown on Fig. 1(a). The SG separation is 220 nm, the separation of the S and D electrodes is $L = 1$ μm, and the diameter of the NW is $W = 77$ nm. Figure 1(b) shows the cross section of the device perpendicular to the NW at the center of the SG electrodes on Fig. 1(a).

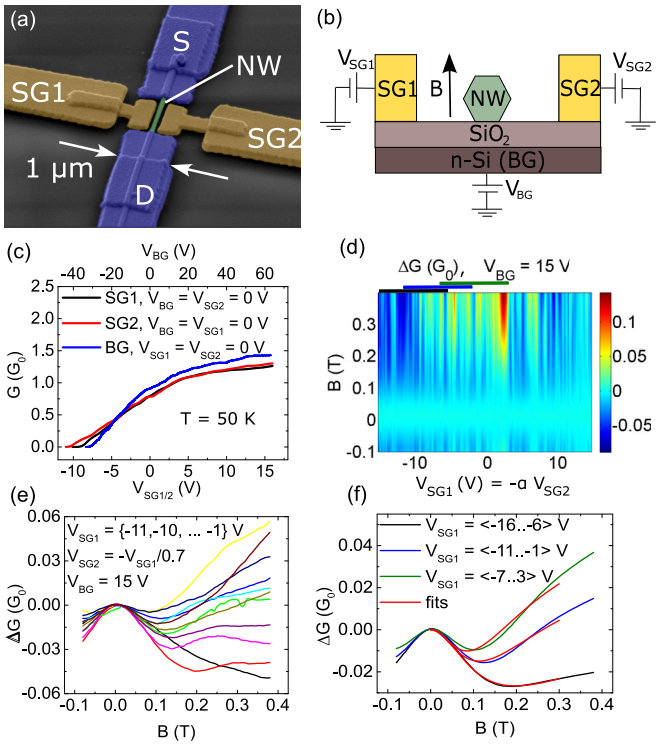

FIG. 1. (a) False color SEM image of a representative device. (b) Cross section of the device, perpendicular to the nanowire (NW) axis along the center of side-gate electrodes. Two side gates (SG1 and SG2) and a back-gate (BG) electrode can be used to apply an electric field on the NW. In addition a magnetic field perpendicular to the substrate and NW was used. (c) The conductance of the NW as a function of different gate voltages at $T = 50$ K. Note that the horizontal axis for the BG and the SG curves are different. (d) Variation of the magnetoconductance (MC), i.e., $\Delta G(B) = G(B) - G(B = 0)$ as a function of the asymmetric SG voltage. For the value of α, see Eq. (2). (e) Typical MC curves, vertical cuts from panel (d). All curves show a peak around zero magnetic field due to the weak antilocalization (WAL) and oscillations at higher B fields due to the universal conductance fluctuation (UCF). (f) Averaged MC curves in a 10 V wide-gate voltage window. Here $< . >$ indicates the gate range of averaging. The effect of the SG-induced electric field can be seen. As stronger electric fields are applied, the minimum of the WAL curve shifts to higher B field values and decreases, which indicates a shorter l_{SO}, stronger SOI. Red curves are fits with theory of the WAL [see Eq. (1)].

In contrast to previously used top-gated geometries, an important advantage of the side-gated sample is that the gate electrode is not in direct contact with the NW. This way the formation of charge traps at the interface of the NW and the top-gate electrode is prevented. A further advantage is that an electric field can be induced in the NW without significant change of the conductance by applying opposite voltages on the SGs.

Low-temperature transport measurements were performed in a liquid helium cryostat with variable temperature insert system, which is equipped with a superconducting magnet. Prior to cool-down, the sample was pumped overnight at room temperature to remove the water contamination from the surface of the NW.

The conductance of the NW, G follows a typical n-type FET characteristics, as it is shown on Fig. 1(c) at $T = 50$ K. Both the SGs and the BG can individually increase the conductance up to 1.5 G_0 ($G_0 = 2e^2/h$ is the conductance quantum), with a saturation-like tendency, and can completely deplete the NW, i.e., quench the conductance, while the other gates are kept at zero potential. The transconductance curves measured as a function of V_{SG1} and V_{SG2} [black and red curves on Fig. 1(c)] are practically overlapping, which indicates that the capacitive coupling to the SGs are almost equal. The SGs have a four times stronger effect than the BG due to the closer spacing to the NW (70 nm, 400 nm, respectively). Note that different horizontal axes are used for the BG and the SGs.

To determine the strength of the spin relaxation, the MC of the device was measured in various gate settings at $T = 4.2$ K. The magnetic field was perpendicular to the substrate [see Fig. 1(b)]. In the used gate geometry with 70-nm spacing between the NW and the SG electrodes, SG voltages (V_{SGi}) up to 20 V and difference of 30 V between V_{SG1} and V_{SG2} could be applied without an electric breakdown.

Changes of the MC in low magnetic fields contains the WAL signal related to the spin relaxation; therefore, we focus on the variation of the conductance from its value in zero magnetic field, i.e., $\Delta G = G(B) - G(B = 0\ \mathrm{T})$. Figures 1(d) and 1(e) show a typical set of measurements of ΔG as a function of B and gate voltages. The MC curves show two general features: first, every curve has a local maximum around zero magnetic field, which is a signature of WAL; second, at higher magnetic fields ($B > 0.1$ T), further oscillations appear in ΔG, which depend on the gate voltages in a random fashion. This random fluctuation (called universal conductance fluctuation, UCF) appears due to the variation of the interference condition of coherent electron paths as B or the gate voltage is changed.

The WAL signal allows us to extract important transport parameters, like the phase coherence length and the spin relaxation length [22,24]. To relieve the WAL signal from UCF, the MC curves were averaged for the gate voltage in a moving window [32] with a width of 10 V. Three averaged MC curves are shown in Fig. 1(f), the corresponding gate voltage windows are indicated with colored bars in Fig. 1(d), above the upper horizontal axis. Due to the averaging, the strongly varying features at high magnetic fields disappear and only a characteristic peak around $B = 0$ T remains with a dip and a

monotonic increase toward higher B fields. This line shape is a characteristic WAL signal.

At first we have investigated the temperature dependence of the WAL signal in a different device. With increasing temperature the height of the peak around zero magnetic field is strongly reduced (see Fig. 4 in Appendix A), which is the signature of decreasing phase coherence length, in agreement with previous studies [29,31,33–35].

The averaged MC curves are fitted with the theoretical formula of the WAL in one-dimensional systems [22,24,25,34],

$$\Delta G(B) = -\frac{2e^2}{hL}\left[\frac{3}{2}\left(\frac{1}{l_\phi^2}+\frac{4}{3l_{SO}^2}+\frac{1}{l_B^2}\right)^{-1/2} - \frac{1}{2}\left(\frac{1}{l_\phi^2}+\frac{1}{l_B^2}\right)^{-1/2}\right], \quad (1)$$

where l_ϕ is the phase coherence length, l_{SO} is the spin relaxation length, $L = 1\ \mu$m is the separation of S and D electrodes, h is the Planck constant, e is the electron-charge, and

$$l_B^2 = \frac{8\hbar^2}{e^2B^2W^2\sqrt{3}},$$

where B is the magnetic field and W is the diameter of the NW. Note that the geometrical factor (i.e., the area of the cross section), W^2 in Refs. [22,24] has been replaced by $\frac{3\sqrt{3}}{8}W^2$ to adapt the formula to the hexagonal cross section of the NW, following the idea in Ref. [34].

This formula is valid in the dirty limit, i.e., the elastic scattering length, l_e is much smaller than the wire diameter, and in the low magnetic field limit, i.e., $l_m = \sqrt{\hbar/eB} >> W$. Our sample is close to fulfilling the first condition, since the diameter of the NW is $W = 77$ nm, and the elastic scattering length is $l_e \approx 10$–20 nm, determined from transconductance measurements [34,41]. The second inequality implies a $|B| < 0.1$ T condition for the fitting. The MC curves were fitted in the $0 < B < 0.3$ T interval, since it is needed to contain the minimum of the WAL curve for a reliable fitting. The formula has two fitting parameters, the phase coherence length (l_ϕ) and the spin relaxation length (l_{SO}). Assuming that the SOI dominates the spin relaxation, l_{SO} can be used to measure the strength of SOI [23,42]. According to Eq. (1) a signature of an enhanced SOI (i.e., reduced l_{SO}) is the shift of the minimum of the WAL curve to higher B values.

The three experimental curves presented in Fig. 1(f) show a clear shift of the minimum of the WAL signal as the asymmetric SG voltage is increased. It is in agreement with the expected enhancement of the SOI as higher electric fields are induced by larger gate voltages. In order to extract l_ϕ and l_{SO} these curves were fitted by Eq. (1). The fitted MC curves are shown with red lines in Fig. 1(f). There is a reasonable agreement between the measured and the fitted curves, even though the magnetic field window used for the fit is somewhat wider than the validity of the model. The extracted l_{SO} parameters for the three plotted measurements are 175, 144, and 92 nm (from top to bottom), showing an enhancement of SOI in increasing electrostatic fields. In the following, using the fitting procedure described above, l_ϕ and l_{SO} are extracted from averaged MC traces measured at different gate settings. We present our results measured on one particular device, but similar effects were observed on several other devices.

III. RESULTS

In our geometry [see Figs. 1(a) and 1(b)] there are three gate electrodes that can induce an electric field inside the NW. In the following, the influence of two different electric field profiles on l_{SO} is studied. In the first case an asymmetric potential is applied on the SGs, while the BG voltage is fixed. In the second case a finite voltage is applied only on the BG, while the SGs are grounded. In this section, we show that the applied external electric fields can strongly enhance the SOI in both cases.

A. Tuning with in-plane electric fields

In the standard FET geometry the BG voltage can be used to induce an electric field in the NW; however, V_{BG} changes the strength of the electric field and the electron density at the same time [see Fig. 1(c)]. The main advantage of the three-gate-configuration is that it allows us to generate an electrostatic field, *without* changing the conductance and the average electron density in the NW, by applying opposite voltages on the two SGs [see Fig. 2(a), inset]. This asymmetric

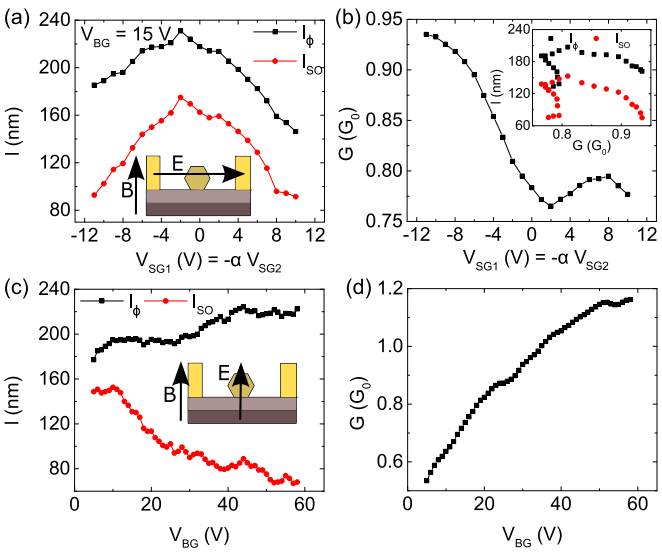

FIG. 2. (a) The fitted l_{SO} and l_ϕ values as a function of the asymmetric side-gate (SG) voltage. For the value of α see Eq. (2). The peak-like reduction of l_{SO} on the red curve indicates the tuning of the SOI with a factor of 2, which is due to the electric field across the nanowire (NW). (inset) The geometry of the measurement with the direction of the electric and magnetic fields. (b) The conductance of the NW at $B = 0$, extracted from the averaged MC data, changes less than 20% while the asymmetric SG voltage is tuned. (Inset) Combined data of (a) and (b), l_{SO} and l_ϕ values as a function of the NW conductance. The lack of correlation of the conductance and the fitting parameters indicates that the tuning is not the result of the change of the conductance. (c, d) Same as (a, b) for the back-gate (BG) tuned measurement. At high positive BG voltages the electric field results in the reduction of l_{SO} by a factor of 2, while the conductance and so the electron density is strongly increased.

gating induces an electric field parallel to the substrate plane, perpendicular to the NW axis.

In order to keep the conductance of the NW constant while the electrostatic field was increased, the asymmetric SG voltages were swept in the following way: $V_{SG1} = -\alpha V_{SG2}$, where

$$\alpha = \begin{cases} 0.7 & \text{if } V_{SG2} > 0\text{V} \\ 1/0.7 & \text{if } V_{SG2} < 0\text{V}, \end{cases} \tag{2}$$

i.e., on the negatively charged SG electrode a voltage smaller by a factor of 0.7 was applied because of the nonlinear gate-dependance of the conductance [see Fig. 1(c)].

In the measurement, shown on Figs. 2(a) and 2(b), V_{SG1} was swept between −16 and 15 V, but on the voltage axis the data is plotted in the $[-11V, 10V]$ interval, since it was averaged in a window of 10 V. The BG voltage was fixed at 15 V to maintain the conductance above 0.5 G_0, which ensures the visibility of the WAL signal. Figure 2(b) shows the conductance at $B = 0$ T extracted from averaged MC measurements as a function of the asymmetric SG voltages applied according to Eq. (2). The conductance was kept close to constant within 0.2 G_0.

On the main panel of Fig. 2(a) l_ϕ and l_{SO}, determined by fitting the averaged MC curves with Eq. (1), are shown. At zero SG voltages the spin relaxation length is about 170 nm, which is comparable with earlier results [29,30,32,35]. By applying the asymmetric voltage on the SGs, and thus generating an electric field perpendicular to the NW, l_{SO} can be significantly reduced to 90 nm. The MC data shown in Figs. 1(d), 1(e), and 1(f) also correspond to this measurement.

The conductance also varied slightly with the applied SG voltages. However, plotting l_ϕ and l_{SO} as a function of the conductance [Fig. 2(b), inset], no clear trend is visible, which refers to the lack of correlation between the conductance and the fitting parameters. It indicates that the reduction of l_{SO} is not the result of the change of the conductance.

The phase coherence length is reduced for large asymmetric SG voltages [see the black curve in Fig. 2(a)], but similarly to l_{SO} its trend is not correlated with the conductance. One can attribute the reduction of l_ϕ to an increased scattering, which can be induced by the surface-roughness of the NW or residual contamination, as the electron density is dominantly pushed to the surface of the NW (see Sec. IV).

Investigating other devices the highest reduction factor of l_{SO} was 3 for $V_{SG1} = 18$ V.

B. Tuning with perpendicular electric fields

In the previous section it was shown that l_{SO} can be strongly tuned by an in-plane electric field generated by asymmetric SG voltages. In order to have a comparison, in a second set of measurements the BG was used as the source of the electric field, while the SG electrodes were grounded. This setting is similar to the standard FET-like gating [29–34]. The main difference compared to the case of asymmetric SG voltages is that in addition to the strength of the electrostatic field, the electron density also changes with V_{BG}, resulting in the change of the conductance, as it is shown in Fig. 2(d). Note that the conductance here is extracted from the averaged MC data. Also note that the transconductance curve is shifted to higher V_{BG} values compared to the blue curve on Fig. 1(c), since the high BG voltages (up to 60 V), required to achieve high electrostatic fields across the NW, caused the filling of charge traps in the SiO_2 in the close proximity of the NW, which screens the effect of the BG. The rearrangement of these static charges results in a difference between the extracted physical quantities at the same gate configuration for the two different sets of measurements.

The corresponding fitted l_ϕ and l_{SO} parameters are plotted in Fig. 2(c). l_{SO} shows a clear tendency as a function of V_{BG}. At small gate voltage values l_{SO} is around 150 nm, while for larger V_{BG} and thereby enhanced electrostatic field l_{SO} monotonically decreases. Applying a BG voltage of more than 60 V, l_{SO} is reduced even to 70 nm.

In some of the previous studies investigating the SOI via WAL in standard FET geometry in InAs and InSb NWs no tuning was observed [32], while in others a tuning effect up to 30% was reported [29,30]. All of these studies used smaller gate voltage ranges than us. A strong tuning, comparable with our results has only been observed in devices using a top gate [36] or an electrolyte gate [35]. Our measured l_{SO} values at low gate voltage values are in a good agreement with these studies.

The change of the phase coherence length is not significant, as in the used range of BG voltage l_ϕ increases less than 20% from 180 to 220 nm. Interestingly, its tendency is just opposite to the case of asymmetric SGs [see Fig. 2(a)]. The enhancement induced by the BG voltage can be explained with the reduction of electron-electron interaction at higher carrier densities (higher conductance).

IV. SIMULATION

In the previous section it was shown that by applying an electric field on the NW with gate electrodes, the SOI can be enhanced by a factor of 2. In this section a simple electrostatic model is introduced, which is employed to calculate the electrostatic field [$\boldsymbol{E}(\boldsymbol{r})$] profile inside the NW and to estimate the electric field-induced Rashba SOI. A good agreement was found between the numerical results for l_{SO} and the measured values presented in the previous section.

For simplification, the measured device is modeled with its two-dimensional cross section shown in Fig. 1(b) and discussed in Sec. II. The NW is modeled by a hexagon with edge length of 40 nm (which corresponds to $W = 80$ nm). From an electrostatic viewpoint a single conduction band is assumed with parabolic dispersion, along with a hard-wall confinement potential. The Fermi level pinning at the surface of the NW gives rise to a band bending [43,44], which for simplicity is neglected in our model. Furthermore, we fixed the Fermi energy at the edge of the conduction band for zero gate voltages.

In the simulation the electric potential, $V(\boldsymbol{r})$ was calculated by solving the Poisson-equation,

$$\Delta V(\boldsymbol{r}) = \frac{\rho(\boldsymbol{r})}{\epsilon_0 \epsilon_r^i}, \tag{3}$$

where, ϵ_r^i is the relative dielectric constant of medium i ($\epsilon_r^{SiO_2} = 3.9, \epsilon_r^{InAs} = 15.15$), ϵ_0 is the vacuum permittivity, and $\rho(\boldsymbol{r}) = -en(\boldsymbol{r})$ is the electron charge density, which is only nonzero within the NW. The electron density of the NW, $n(\boldsymbol{r})$ is given by the bulk density of states (DOS) of the InAs at zero

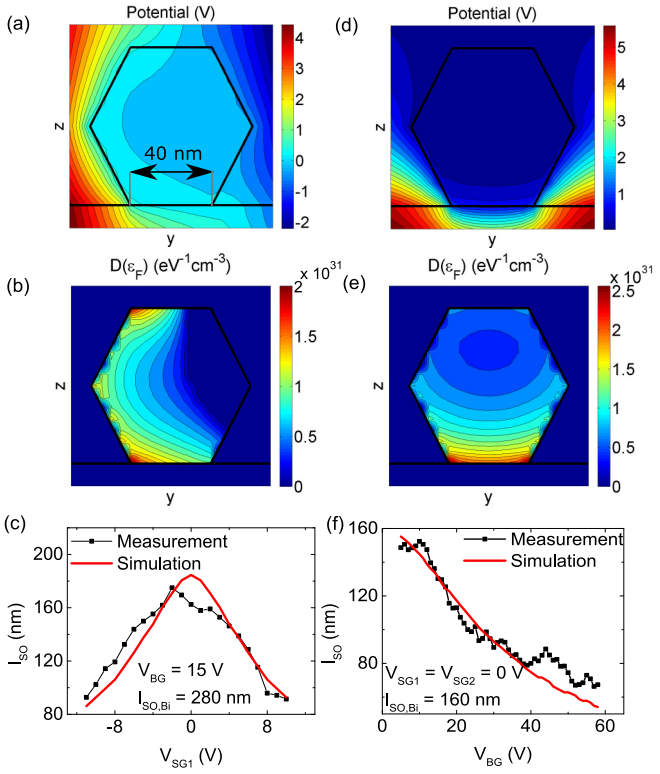

FIG. 3. Results of the numerical simulation. (a, b) The electric potential and the density of states (DOS) at the Fermi energy, respectively, in the vicinity of the nanowire (NW), for $V_{SG1} = 11$ V, $V_{SG2} = -7.7$ V, $V_{BG} = 15$ V. The black lines mark the NW/SiO_x/vacuum boundaries. The low DOS values at the surface of the NW is the result of the relatively coarse resolution of the grid (5 nm). (c) The spin relaxation length in the asymmetric side gate configuration, the measurement data is the same as in Fig. 2(a) (black squares), and the result of the numerical calculation (red curve). (d, e) Same as (a, b), for the BG-tuned measurement with $V_{SG1} = V_{SG2} = 0$ V, $V_{BG} = 58$ V. (f) Same as (c), for tuning with BG.

temperature,

$$n(\boldsymbol{r}) = \frac{3}{4\pi^2}\left(\frac{2m^*}{\hbar^2}\right)^{3/2}[eV(\boldsymbol{r})]^{3/2}, \tag{4}$$

where e is the electron charge, $\hbar = h/2\pi$ is the Planck constant, $m^* = 0.023m_e$ is the effective mass of the electrons in the conduction band, and m_e is the free electron mass. In the simulation, Eqs. (3) and (4) are solved self-consistently in an iterative manner. The details of the simulation can be found in Appendix B.

The calculated electric potential and the DOS at the Fermi energy for the two types of measurements are shown in Figs. 3(a), 3(b) and 3(d), 3(e). The black lines represent the NW/SiO_2/vacuum interfaces, the scale is shown in Fig. 3(a). The SG and BG electrodes are not shown on the graphs, the SG1 (SG2) is on the left (right) 70 nm away from the edge of the NW, the BG is 400 nm below the NW/SiO_2 interface.

Figures 3(a) and 3(b) correspond to the asymmetric SG measurement with gate voltage values of $V_{SG1} = 11$ V, $V_{SG2} = -7.7$ V and $V_{BG} = 15$ V. The electron density [which can be directly calculated from the DOS with Eqs. (B1) and (B2)] is concentrated to the left side of the NW, as a result of the attractive force of the positively charged SG1 electrode. For this gate configuration the numerical calculation yields an average electric field of 20 mV/nm inside the NW.

Figures 3(d) and 3(e) correspond to the BG measurement with grounded SG electrodes with $V_{SG1} = V_{SG2} = 0$ V and $V_{BG} = 58$ V gate voltage values. The electron density is concentrated to the bottom part of the NW. The average electric field within the NW is about 25 mV/nm for this gate configuration.

The small areas of low DOS values at the surface of the NW in Figs. 3(b) and 3(e) are artifacts arising from the grid of the simulation (5 nm).

The spin relaxation length associated to the external field-induced Rashba SOI can be calculated from the magnitude of the electric field supplied by the simulation with the following formula [45]:

$$l_{SO,R} = \frac{\hbar^2}{m^*\alpha_0 e\langle E\rangle}, \tag{5}$$

where $\alpha_0 = 1.17$ nm^2 for InAs. $\langle E\rangle$ is the spatially averaged electric field within the NW, weighted with the DOS at the Fermi energy [see Eq. (B4)]. The formula connects the strength of the SOI, $\alpha_R = \alpha_0 e\langle E\rangle$, with the spin relaxation length, which is the distance covered by the electron, while its phase changes by unity due the SOI Hamiltonian.

In the measurements, l_{SO} was finite at zero gate voltages, which indicates that other sources of spin relaxation are present. To take them into account, we introduce the built-in spin relaxation length, $l_{SO,Bi}$. The built-in spin relaxation processes may originate from breaking the inversion symmetry of the system by the crystal structure, the confinement potential, or scattering centers. For the sake of simplicity we assume that these processes are independent from the external gate voltages. For the different spin relaxation contributions the following sum rule was used:

$$l_{SO}^{-2} = l_{SO,Bi}^{-2} + l_{SO,R}^{-2}. \tag{6}$$

The value of $l_{SO,Bi}$ was chosen such that the measured and the calculated l_{SO} values coincide with each other at zero asymmetric SG/BG voltage in the two demonstrated measurements. The simulation contains no further fitting parameters.

The measured and the simulated l_{SO} curves are shown in Figs. 3(c) and 3(f) for the two different electrostatic field profiles. The measured l_{SO} curves are the same as in Figs. 2(a) and 2(c). In both cases the simulated curves reproduce well the main findings of the measurement, i.e., the SOI is enhanced by increasing electric fields. Furthermore, despite the simplicity of the model and the low number of model parameters fairly good quantitative agreement was found.

In both cases l_{SO} tends to saturate at higher voltages, which is the result of electrostatic screening by electrons. As it can be seen from the DOS graphs in Figs. 3(b) and 3(e), the electron density can reach high values in the NW close to the positively charged gate electrode. At higher electron densities the screening is more efficient, in agreement with the static screening theory, which leads to the decreasing enhancement of the SOI as the gate voltages are further increased. To

quantify the screening effect we estimate the screening length in the framework of the Thomas-Fermi model [46]. In this model the screening length is given by

$$r_{\mathrm{TF}} = \left(\frac{e^2 D(\varepsilon_F)}{\epsilon_0 \epsilon_r} \right)^{-1/2}.$$

With a typical value of DOS at the Fermi level, $D(\varepsilon_F) = 1 \times 10^{31}$ eV^{-1}cm^{-3}, for InAs ($\epsilon_r^{\mathrm{InAs}} = 15.15$) the screening length is $r_{\mathrm{TF}} \approx 10$ nm, which is consistent with the simulated electric potential profiles [see Figs. 3(a) and 3(d)].

We have shown that the introduced electrostatic model can explain our experimental results with an external field-induced Rashba SOI, assuming another, constant source of spin relaxation.

Comparing our values of l_{SO} with previous measurements on InAs quantum dots, we found comparable values (100–170 nm) [2,5,39], although the electronic confinement is different in the case of quantum dots. Other studies describe the strength of the SOI with the energy splitting of different spin states due to the SOI. They report values in the range of $\Delta_{\mathrm{SO}} = 50$–$200$ μeV [37–39], although its value depends on, e.g., the orientation of the magnetic field. In Ref. [39] the authors calculated an l_{SO} of 127 nm from $\Delta_{\mathrm{SO}} = 230$ μeV.

Following the standard framework of the WAL [29] we assume that the SOI is the main mechanism of the spin relaxation and the measured spin relaxation length gives a good measure of the strength of the SOI. Using Eq. (5) and the measured l_{SO} values, one can estimate the strength of the SOI, $\alpha_R = \hbar^2/m^* l_{\mathrm{SO}}$, which is reasonable at high external fields, when the induced Rashba SOI dominates the built-in contribution. Tuning l_{SO} from 150 to 70 nm corresponds to $\alpha_R \approx 2 \times 10^{-11}$ eVm and 4.3×10^{-11} eVm, respectively.

In a very recent work of van Weperen *et al.* [36], a more realistic model of the WAL theory is presented, which takes the 3D structure of the NW into account more precisely and allows us to extract the spin-orbit induced spin relaxation length, $l_{\mathrm{SO,R}}$, and the Rashba spin-orbit coupling parameter, α_R, more accurately. However, the parameter range of the model does not cover the condition of our measurements since for our sample W/l_e is around 4–8. We believe that additional model calculation would be desired in order to give an accurate estimation of the SOI strength α_R, which goes beyond some simplifications: as the source of the spin relaxation mechanism most models consider a simple Rashba type SOI induced by a uniform electrostatic field in the entire NW. In our device the electrostatic field is not uniform, and in addition other SOI terms, such as D'yakonov-Perel has to be taken into account due to the lack of inversion symmetry of the wurtzite NW structure. Nevertheless, it does not influence our finding that l_{SO} can be tuned by the gate voltages even if the conductance and the average density is kept constant.

V. CONCLUSION

The SOI of InAs NWs has been studied by WAL measurements in a side-gated geometry. We have shown that the strength of the SOI can be enhanced by up to a factor of 2 by applying an electric field across the NW. The tuning has been demonstrated at a nearly constant conductance with asymmetric voltages applied on opposite SGs. Furthermore, a similarly large tuning was observed applying a high BG voltage, which strongly changed the electron density as well.

An electrostatic model has been introduced to calculate the strength of the Rashba SOI induced by the external electric fields. A good agreement has been found between experiments and numerical calculations. It supports our claim that the Rashba SOI is the origin of the gate-induced changes of the WAL signal. The possibility to tune the Rashba SOI strength *in situ* without changing the electron density of the device is highly promising for various quantum electronic devices.

In order to gain a better insight into the SOI in NWs, a more realistic model calculation would be desired, which takes into account the inhomogeneous electrostatic field in the NW, the presence of the NW confinement potential, the band bending at the interface, the SOI term caused by the internal inversion asymmetry of the wurtzite crystal structure, the quantized conductance channels of the NWs, and the significant Zeeman splitting due to the large g-factor of the semiconducting NWs [47]. Such a more realistic theory could shine light on the limits of the validity of the simple 1D Rashba SOI Hamiltonian for the description of the spin physics in semiconductor NWs.

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APPENDIX A: TEMPERATURE-DEPENDENT DATA

We have investigated the temperature dependence of the WAL signal on a different device. The corresponding averaged curves are shown on Fig. 4 between 2.17 and 30 K with grounded SGs. While the width of the WAL curve is barely changing with the temperature, the height of the peak at

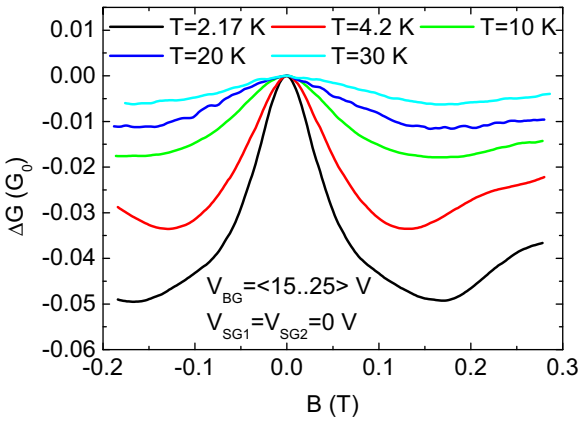

FIG. 4. Temperature dependence of the WAL signal. The reduction of the WAL peak at zero magnetic field indicates the reduction of the phase coherence length with increasing temperature.

zero magnetic field is strongly reduced as the temperature is increased, which indicates the reduction of the phase coherence length. Indeed, l_ϕ is reduced from 270 to 105 nm as the temperature was increased up to 30 K, in agreement with previous studies [29,31,33–35].

APPENDIX B: SIMULATION

In this section the details of the electrostatic simulation are discussed.

The thickness of the SG electrodes is 100 nm, their separation is 220 nm. The thickness of the oxide layer is 400 nm. The boundary of the geometry is defined by a 1 μm $\times$ 1 μm square, whose lower edge corresponds to the BG. The potential of the upper edge is fixed at zero potential. The potential of the right and the left edges below (above) the SG electrodes are defined by a linear interpolation between the potential of the BG and SGs (SGs and upper edge). A square grid with 5-nm resolution is used in the simulations.

The NW is modeled with the properties of bulk InAs with the three-dimensional DOS,

$$D(\varepsilon) = \begin{cases} \frac{1}{2\pi^2}\left(\frac{2m^*}{\hbar^2}\right)^{3/2}\sqrt{\varepsilon} & \text{if } \varepsilon \geqslant 0 \\ 0 & \text{if } \varepsilon < 0 \end{cases}, \tag{B1}$$

with a hard-wall confinement potential, neglecting the band bending.

During the simulation the Poisson-equation [Eq. (3)] and electron-filling,

$$n(\boldsymbol{r}) = \int_0^\infty D(\varepsilon) f(\varepsilon) d\varepsilon, \tag{B2}$$

were calculated iteratively, where $f(\varepsilon)$, the Fermi-function, was approximated with its zero temperature form, the Heaviside step-function.

To assure the convergence of the algorithm for both the electron density and the potential, the weighted average of the last two iteration step was used as new value, i.e.,

$$\begin{aligned} n^{(i)} &\to (1-\eta_n) n^{(i-1)} + \eta_n n^{(i)}, \\ V^{(i)} &\to (1-\eta_V) V^{(i-1)} + \eta_V V^{(i)}. \end{aligned} \tag{B3}$$

In the simulations $\eta_n = \eta_V = 0.2$ was used.

To the calculation of the SOI the electric field is calculated from the potential within the NW. Since only electrons at the Fermi-surface contribute to the conductance, the electric field is averaged with respect of the DOS at the Fermi-level,

$$\langle E \rangle = \frac{\int d^2 r |\boldsymbol{E}(\boldsymbol{r})| D[eV(\boldsymbol{r})]}{\int d^2 r D[eV(\boldsymbol{r})]} \tag{B4}$$

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