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Single-electron tunneling with slow insulators

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The usual paradigm in the theory of electron transport is related to the fact that the dielectric permittivity of the insulator is assumed to be constant, with no time dispersion. We take into account the "slow" polarization dynamics of the dielectric layers in the tunnel barriers in the fluctuating electric fields induced by single-electron tunneling events and study transport in the single-electron transistor (SET). Here "slow" dielectric implies a time scale that is slow compared to the characteristic time scales of the SET charging-discharging effects. We show that for strong enough polarizability, such that the induced charge on the island is comparable to the elementary charge, the transport properties of the SET substantially deviate from the known results of transport theory of the SET. In particular, the Coulomb blockade is more pronounced at finite temperature, the conductance peaks change their shape, and the current-voltage characteristics show the memory effect (hysteresis). However, in contrast to SETs with ferroelectric tunnel junctions, here the periodicity of the conductance in the gate voltage is not broken; instead, the period strongly depends on the polarizability of the gate dielectric. We uncover the fine structure of the hysteresis effect where the "large" hysteresis loop may include a number of "smaller" loops. Also we predict the memory effect in the current-voltage characteristics $I(V)$, with $I(V) \neq -I(-V)$.

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I. INTRODUCTION

The single-electron transistor (SET) is one of the most studied nanosystem [1–7]. This is possibly the simplest device in which strong electron correlations and the quantum nature of electrons can be directly observed. It consists of two electrodes known as the drain and the source, connected through tunnel junctions to one common electrode with a low self-capacitance, known as the island. The electrical potential of the island can be tuned by a third electrode, known as the gate, capacitively coupled to the island; see Fig. 1 for an equivalent circuit.

For decades there was nearly a paradigm in the theory of electron transport at the nanoscale that when calculating dc current, the permittivity of dielectric layers in tunnel nanojunctions may be taken to be constant, without any frequency dispersion [4,5,8–10]. However, this paradigm is not always true. A number of physical processes contribute to the polarization of a dielectric. Some of them are fast, and some are slow compared to the time scales of the electric field change in the nanojunctions [11–20]. There has been progress in the development of dielectric materials with a strong and, at the same time, quite slow response to the external electric field [19,21,22]. The SET is a perfect laboratory device to study this physics: charging-discharging effects in the SET are controllable and have well-defined time scales.

The Coulomb blockade suppresses electron transport except for values of the gate voltage where electrons sequentially tunnel one by one through the SET from the source to the drain. Electric fields in the tunnel junctions change in time while electrons tunnel through the island. Dielectric layers in the tunnel junctions are polarized at finite electric field. The usual assumption in the theory of SETs is that the polarization of any dielectric layer in the tunnel barrier instantly follows the electric field in time: $\mathbf{P}(t) = \hat{\chi}\, \boldsymbol{\mathcal{E}}(t)$, where the constant $\hat{\chi}$ is the dielectric permittivity (tensor) of the dielectric layer [4,10]. It follows from the last expression that the capacitance C of any tunnel junction in the SET is related to the geometric capacitance $C^{(0)}$ as $C = \epsilon\, C^{(0)}$, where for a flat capacitor with isotropic dielectric $\epsilon = (1 + 4\pi\chi)$ [23]. This is the only place where the polarization appears in the "classical" theory of SETs. However, these relations have limited applicability. In general, the polarization of the dielectric is nonlocal in time: $\mathbf{P}(t) = \int_{-\infty}^{t} \hat{\chi}(t-\tau)\boldsymbol{\mathcal{E}}(\tau)d\tau$, where $\hat{\chi}(t)$ is the dynamical electric permittivity. (Here we assume the linear response regime.) The time dependence of $\hat{\chi}(t)$ implies that tuning the dielectric polarization $\mathbf{P}(t)$ by an electric field cannot be done arbitrarily fast. This happens, for example, in dielectric materials with polarization due to the shift of heavy and inert ions [12,18,20].

The response of polarization $\mathbf{P}(t)$ to the external field is characterized by the time scale τ_{P}, the decay time of $\hat{\chi}(t)$. The second characteristic time scale in the problem is the time of the electric field correlation $\tau_{\mathcal{E}}$. For $\tau_{P} \ll \tau_{\mathcal{E}}$ the polarization has the form $\mathbf{P}(t) \approx \hat{\chi}_0 \boldsymbol{\mathcal{E}}(t)$, where $\hat{\chi}_0 = \int_{-\infty}^{\infty} \hat{\chi}(\tau)d\tau$. In the opposite case, $\tau_{\mathcal{E}} \ll \tau_{P}$, the polarization $\mathbf{P}(t)$ does not follow the electric field $\boldsymbol{\mathcal{E}}(t)$ instantaneously, and it has the form

$$\mathbf{P}(t) \approx \hat{\chi}\, \langle \boldsymbol{\mathcal{E}} \rangle, \tag{1}$$

where $\langle \boldsymbol{\mathcal{E}} \rangle$ is the electric field averaged over the time scale τ_{P}. It follows from Eq. (1) that the simple relation for capacitance, $C = \epsilon\, C^{(0)}$, is not valid. Therefore the theory of single-electron tunneling in the SET should be modified, and that is the main goal of our paper.

The characteristic time of charge relaxation in the SET is $\tau_{\mathcal{E}} = R_{\Sigma} C_{\Sigma}$, where R_{Σ} is of the order of the bare tunnel resistance of the left and right tunnel junctions and C_{Σ} is the

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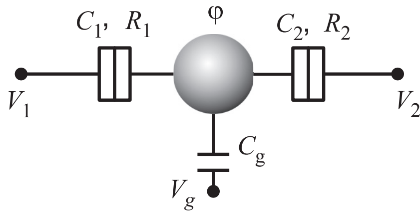

FIG. 1. The equivalent scheme of a single-electron transistor [4].

sum of all the capacitances (see Fig. 1). The time scale τ_ε is in the range of dozens of nanoseconds to picoseconds, depending on the system geometry and materials. The switching time of a dielectric material τ_P is in the range of seconds to femtoseconds, depending on the material and the particular physical process behind the polarization phenomena [18,20].

Therefore the regime of a "slow" insulator, $\tau_\varepsilon \ll \tau_P$, is very important for SET devices. However, there is paradigm in which the existing theories with $\tau_P \ll \tau_\varepsilon$ satisfactorily explain most experiments with SETs. What is the justification for a new theory? The answer is simple: the effects discussed in this paper are especially pronounced in SETs when, on average, the polarization of a dielectric tunnel junction in the SET is strong enough, meaning that the charge induced on the grain by the polarized dielectric is of the order of the electron charge. This condition can be reached only for large enough dielectric permittivity ϵ. We will discuss how large that is below.

Recently, we have found a number of transport effects in the SET with a slow ferroelectric in the capacitors (see Refs. [6,7]). In particular, we investigated the memory effect in this SET. Here we uncover distinct physical phenomena and report on the memory effect (hysteresis) where conductance periodicity in the gate voltage is not broken. Instead, the period strongly depends on the polarizability of the gate dielectric due to the linear dependence of the polarization on the external field in the dielectric. Also, we uncover the unusual fine structure of the hysteresis effect, where "large" hysteresis loop may include a number of "smaller" loops. We predict that the memory effect exists in the current-voltage characteristics, meaning that $I(V) \neq -I(-V)$ for a given hysteresis branch even at $V_g = 0$. The last two effects may exist in the ferroelectric SET; however, neither of them has been found before. These results are important: a SET device with hysteresis may be promising for the "shuttle" of charge [24–26] free from moving nanomechanical degrees of freedom: cycling the gate voltage along the hysteresis loop might allow transfer of several charge quanta through the SET. Other promising applications include transistors [4] and memory cells. For example, the memory effect in $I(V)$ and $G(V_g)$ might help in writing data in and reading data from the polarization state.

This paper is organized as follows. In Sec. II we discuss the general properties of a SET with slow dielectric and the methods for investigating transport properties. In Sec. III we investigate the SET with a slow dielectric located in the gate electrode at zero bias voltage, $V_2 - V_1$. In Sec. IV we consider the case with the slow dielectric in the left and right tunnel barriers of the SET and uncover the memory effect in the current-voltage characteristics $I(V)$. Finally, in Sec. V we discuss the validity of our approach and the requirements for slow dielectric materials which are necessary to observe the effects predicted in this paper. In the same section we show that the Coulomb blockade in the SET with slow dielectrics is less affected by temperature.

II. ELECTRON TRANSPORT THROUGH A SET WITH SLOW TUNNEL BARRIERS

A. Model

Consider the single-electron transistor depicted in Fig. 1. Two side electrodes serve as the transistor source and drain. Electric current flows through the transistor channel, which is the metal island placed between leads and connected to the source and drain by the tunnel junctions. The bottom gate electrode controls electron transport through the channel. Current does not flow through the gate electrode (similar to the field effect transistors). The theory of a "classical" SET is developed in Refs. [2–5]. The essential feature of the SET discussed here is related to the fact that the gate capacitor and/or tunnel junction capacitors are filled with a dielectric material with some special properties. This dielectric material has a very long response time, leading to the essential time dispersion of the capacitor. As a result, the electric polarization of the gate capacitor should be considered in a special way.

In the following it is convenient to distinguish between the geometrical junction capacitances $C_i^{(0)}$ and the low-frequency capacitances C_i that include the slow dielectric response. The difference between them, aside from the unimportant geometrical factor, is

$$\Delta C_i = C_i - C_i^{(0)} = \alpha_i S_i / d_i, \tag{2}$$

where α_i is the dielectric polarizability of the ith junction ($i = 1,2,g$), S_i is the junction surface area, and d_i is the effective electrode-island distance. Here α_i so defined includes all the demagnetization factors related to the geometry of the capacitors and effects related to nonuniform and anisotropic dielectric layers [23]. For a flat capacitor with an isotropic dielectric, $C^{(0)} = S/4\pi d$ and $\alpha = \chi$.

We assume that the electrodes are biased with the voltages $V_1 = -V/2$, $V_2 = V/2$, and V_g. The grain potential $\phi(n)$ at a given number of excess electrons n can be found by balancing the induced charges:

$$n\,e = \sum_i C_i^{(0)}[\phi(n) - V_i] + \sum_i \Delta C_i(\langle\phi\rangle - V_i), \tag{3}$$

$$\langle\phi\rangle = \sum_{n'=-\infty}^{\infty} p_{n'}\phi(n'), \tag{4}$$

where p_n is the probability to find n excess charges on the grain. Two terms originate in (3) because we distinguish between the electric field produced by the capacitance $C_i^{(0)}$ and the contribution due to the polarized dielectric with a slow response. So the terms proportional to the coefficient ΔC_i in Eq. (4) can be considered charges induced on the grain by the polarized dielectric layers that are constant in tunneling events.

The probability distribution p_n in the steady state can be found using the detailed balance equation [2–5]

$$p_n \Gamma^{n\to n+1} = p_{n+1}\Gamma^{n+1\to n}, \tag{5}$$

where the rate $\Gamma^{n\to n+1}[V_i,n,\langle\phi\rangle]$ describes the change in the grain charge from n to $n+1$ electrons. The electric current has the form

$$I = e\sum_{n=-\infty}^{\infty} p_n\left[\Gamma_s^{n\to n-1} - \Gamma_s^{n\to n+1}\right]. \tag{6}$$

Here the lower index of Γ refers to the tunneling rate corresponding to the particular tunnel junction, $s = 1$ or 2, and the rate Γ in Eq. (5) is equal to $\Gamma_1 + \Gamma_2$. Solving Eqs. (3)–(5) self-consistently, we find the current-voltage characteristics of the SET using Eq. (6).

We use the "orthodox" theory [2–5] to calculate the Coulomb-blockade peaks in the differential conductance of the SET. It implies that the tunnel junction resistances $R_{1,2}$ are much larger than the resistance quantum $R_q = h/e^2$: this condition ensures perfect quantization of the excess charge on the island. The temperature T must be much smaller than the charging energy (it is of the order of electrostatic energy of one excess electron on the island); see Sec. V D for a discussion of the correct definition of the charging energy. Also the electron level spacing on the island should be smaller than the temperature (see Sec. V).

In the leading order the probability per unit time to change the island occupation number from n to $n\pm 1$ through the first junction is given by Fermi's golden rule:

$$\Gamma^{(1)}_{n\to n\pm 1} = \frac{1}{e^2 R_1}\Delta F_1^{n\to n\pm 1} N_B\left(\Delta F_1^{n\to n\pm 1}\right), \tag{7}$$

where $N_B(\omega) = 1/[\exp(\omega/T) - 1]$ is the Bose function [4,27], R_1 is the tunnel junction resistance, and $\Delta F_1^{n\to n\pm 1}$ denotes the free-energy change, with Q_0' being the effective charge,

$$\Delta F_1^{n\to n\pm 1} = \Delta U_n^{\pm} \mp W_1, \tag{8}$$

where $\mp W_1$ is the work done by the leads and the gate to transfer an electron to/from the grain through the first tunnel junction. The calculation of Γ rates requires knowledge of the difference in the electrostatic energies when the number of excess charges on the grain differs by one elementary charge: $\Delta U_n^{\pm} = U(n\pm 1) - U(n)$. If the polarization in dielectric layers on electron jumps follow ϕ adiabatically, $P_i = \alpha_i(\phi - V_i)/d_i$, we have $\Delta U_n^{\pm} = E_c(1\pm 2n)$, where $E_c = e^2/2C_\Sigma$ with all the capacitances $C_\Sigma = \sum_i C_i$ being properly renormalized, $C_i = C_i^{(0)}(1 + 4\pi\alpha_i)$. However, for slow dielectric layers the polarization $P_i = \alpha_i(\langle\phi\rangle - V_i)/d_i$ stays constant during the tunneling, and for the energy difference we find (see Appendix A)

$$\Delta U_n^{\pm} = E_c^{(0)}\left(1 \pm 2n \mp 2\sum_i P_i S_i/e\right), \tag{9}$$

where $E_c^{(0)} = e^2/2C_\Sigma^{(0)}$, $C_\Sigma^{(0)} = \sum_i C_i^{(0)}$, and $P_i S_i = \Delta C_i(\langle\phi\rangle - V_i)$.

The work done by the leads and the gate to transfer an electron to/from the grain remains the same as in the orthodox theory [2–5], except for the fact that only the geometrical capacitances $C_i^{(0)}$ should be taken into account:

$$W_1 = \frac{e\left(\left[C_g^{(0)} + C_2^{(0)}\right]V_1 - C_2^{(0)}V_2 + Q'\right)}{C_\Sigma^{(0)}}, \tag{10}$$

$$W_2 = \frac{e\left(\left[C_g^{(0)} + C_1^{(0)}\right]V_2 - C_1^{(0)}V_1 + Q'\right)}{C_\Sigma^{(0)}}, \tag{11}$$

where the effective gate-induced charge Q' is

$$Q' = -C_g^{(0)}V_g + \sum_i \Delta C_i\left(\langle\phi\rangle - V_i\right). \tag{12}$$

This in particular implies that for temperature $T\to 0$ the effective ground-state free energy is defined as

$$F_0 = E_c^{(0)}\min_n (n - Q'/e)^2. \tag{13}$$

Below we use the notation $Q = -C_g V_g$ for the traditional gate-induced charge. We show that although the effects of slow polarization are far from being a simple renormalization of capacitances $C_i^{(0)} \to C_i$, the conductance periodicity in Q holds and maintains its period $|e|$ for any values of the parameters ΔC_i.

B. Nature of the memory effect: Analytical estimates

The detailed balance equation (5) can be solved analytically for the set of voltages V_g near the "degeneracy points," where the ground-state energy of the SET changes from n to $n\pm 1$ excess charges. The last condition requires the effective charge Q' to be close to $e(n+1/2)$. In this case only the two probabilities p_n are finite, while the other probabilities are exponentially suppressed by the factor $e^{-E_c^{(0)}/T}$. In order to illustrate the origin of the memory effect, we will focus on the degeneracy point between $n = 0$ and $n = 1$ at $V_{1,2} = 0$. Using Eqs. (3) and (4), we find for the average potential $\langle\phi\rangle$

$$n_F\left[(1 - 2Q'/e)E_c^{(0)}\right] = e\langle\phi\rangle/2E_c^{(0)} + Q'/e, \tag{14}$$

where n_F is the Fermi function. Equation (14) has one or three solutions for a given gate voltage Q. The latter case is shown in Fig. 2. The presence of three distinct solutions for the average potential $\langle\phi\rangle$ at a given parameter Q indicates the memory-effect instability. Using the graphical solution of Eq. (14), we estimate the criterion for the memory-effect instability, $\sum_i \Delta C_i/C_\Sigma^{(0)} \gtrsim 2T/E_c^{(0)}$. This criterion corresponds to the critical value of ΔC_Σ when the memory effect just appears; see Eq. (36) below for the exact expression.

III. SET WITH A SLOW INSULATOR IN THE GATE CAPACITOR

A. Numerical study of electron transport through a SET

Here we study electron transport through a SET numerically. We consider the SET with a slow dielectric layer in the gate capacitor. This setup is the most favorable for experiment since in this case there is no electron tunneling through the gate electrode and it can be arbitrarily thick, allowing a wide choice of dielectric materials. Moreover, as we will show in Sec. IV, at $V = 0$ by considering the gate capacitor we still preserve all the qualitative effects introduced by slow dielectrics in a general case.

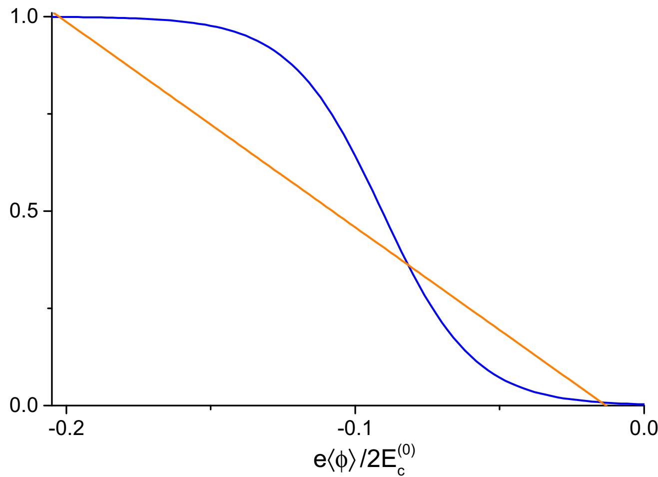

FIG. 2. (Color online) Graphical solution of Eq. (14) showing three possible solutions for an average grain potential $\langle\phi\rangle$ at a given gate voltage V_g. Parameters are $Q = -0.07|e|$, $C_g^{(0)} = 0.5C_\Sigma^{(0)}$, $\Delta C_g/C_\Sigma^{(0)} = 0.5$, and $T = 0.4\,E_c^{(0)}$. The three distinct solutions for $\langle\phi\rangle$ at a given Q_0 correspond to the memory effect instability.

Thus, for a time, we assume that the only nonzero ΔC is ΔC_g.

For $\Delta C_g = 0$ the conductance is a periodic function of the effective gate voltage Q; see the gray curve in Fig. 3. The conductance peaks are well fitted by the orthodox theory, in which, near the peak maximum, the conductance is

$$G^{(0)}(\delta Q^{(0)}) \approx \frac{e\,\delta Q^{(0)}/C_\Sigma^{(0)}T}{2(R_1+R_2)\sinh\left(e\delta Q^{(0)}/C_\Sigma^{(0)}T\right)}. \quad (15)$$

Here $\delta Q^{(0)}/e = \min_k[-C_g^{(0)}V_g/e - (2k+1)/2] \ll 1$.

At finite but small ΔC_g, when the induced charge on the island due to polarization is smaller than the elementary charge, the conductance peaks change their shape but preserve their amplitude and position (see Fig. 3).

The opposite case, with dielectric polarization being strong enough to induce a charge on the island of the order of the elementary charge or larger, is more interesting. In this case the conductance peaks show the hysteresis, and their shape depends on the direction of Q evolution (see Fig. 4). The hysteresis appears for $\Delta C_g \gtrsim C_\Sigma^{(0)}2T/E_c^{(0)}$ [see Eq. (29)]. Despite the memory effect the conductance remains periodic in the renormalized gate voltage $Q = -(C_g^{(0)} + \Delta C_g)V_g$, with the same period $|e|$ for any ΔC_g. This behavior is in striking contrast to the SET with a ferroelectric in the gate, where due to the nonlinearity of the polarization–electric-field dependence the periodicity of the conductance is broken (see Ref. [7]).

Now we discuss the structure of the memory effect. Above the critical value of ΔC_g there are many branch solutions of the self-consistency equation for the average grain potential, Eq. (4), for the given temperature, bias, and gate voltage. The question is, How do we choose the right branch? Figure 5 provides an answer to this question. According to the branching theory [28], the jumps occur at the "branching points," where the observable has an infinite derivative in parameter Q. On the other hand, the branch should correspond

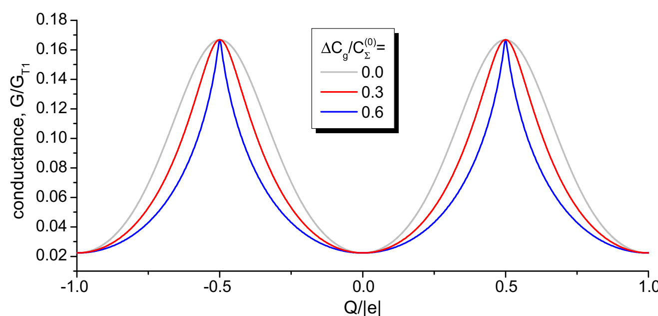

FIG. 3. (Color online) Conductance peaks for $\Delta C_g/C_\Sigma^{(0)} = 0, 0.3, 0.6$. The unit of conductance G_{T1} is the conductance of the first tunnel junction of the SET. Parameters are capacitances $C_1^{(0)} = 0.3C_\Sigma^{(0)}$, $C_2^{(0)} = 0.5C_\Sigma^{(0)}$, and $C_g^{(0)} = 0.2C_\Sigma^{(0)}$ and temperature $T = 0.2E_c^{(0)}$. The slow dielectric in the gate capacitor modifies the shape of the conductance peaks but preserves the periodicity in parameter Q, in contrast to the SET with a ferroelectric in the gate capacitor [7].

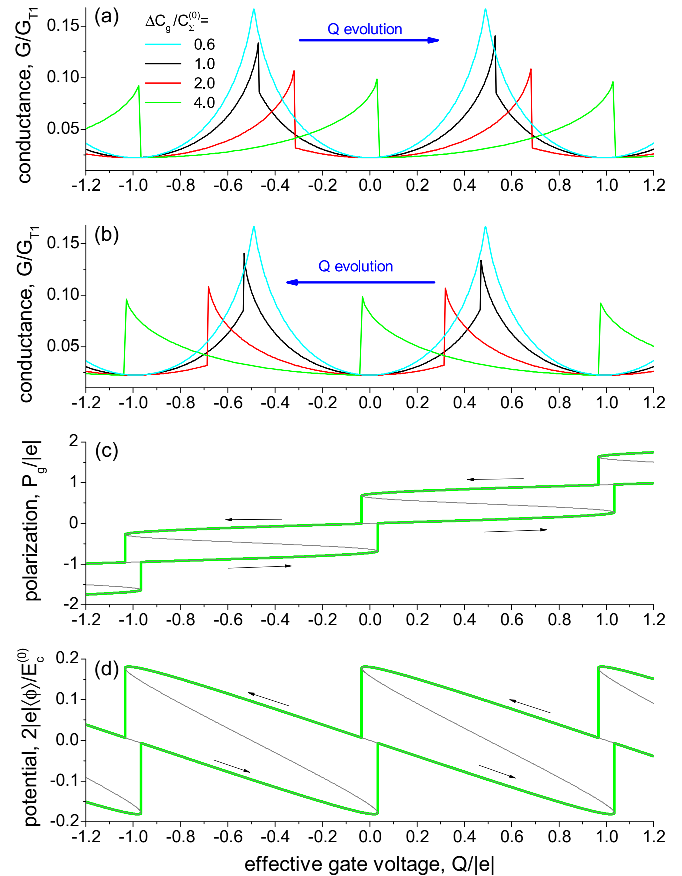

FIG. 4. (Color online) Memory effect instability in the SET with a slow insulator in the gate capacitor. (a) and (b) The conductance branches corresponding to increasing and decreasing Q, respectively, and $\Delta C_g/C_\Sigma^{(0)} = 0.6, 1, 2, 4$, (c) polarization, and (d) the average grain potential (arrows show the direction of Q evolution for a given branch) for $\Delta C_g/C_\Sigma^{(0)} = 4$. Gray lines show stable and unstable branches of polarization and the average potential. Parameters are capacitances $C_1^{(0)} = 0.3C_\Sigma^{(0)}$, $C_2^{(0)} = 0.5C_\Sigma^{(0)}$, and $C_g^{(0)} = 0.2C_\Sigma^{(0)}$ and temperature $T = 0.2E_c^{(0)}$ as in Fig. 3.

FIG. 5. (Color online) Memory effect: (a)–(d) and (f) the conductance for $\Delta C_g/C_\Sigma^{(0)} = 1.3, 3.3, 5.3, 10, 20$ for stable and unstable branches of Eq. (4) for the average grain potential. (e) The polarization for $\Delta C_g/C_\Sigma^{(0)} = 10$. Arrows indicate the positions of hysteresis jumps for a particular branch with increasing Q. All plots are shown at fixed temperature $T = 0.2E_c^{(0)}$.

to the minimum of some effective energy functional. In our case (no bias) the effective energy,

$$F = -T \ln Z, \qquad Z = \sum_n \exp\left(-\frac{E_c^{(0)}(n - Q'/e)^2}{T}\right). \tag{16}$$

For zero temperature it reduces to the free energy F_0 discussed above.

The plots of the free energy have a dependence on the parameter Q similar to that of the zero-bias conductance G. To illustrate this point we show in Fig. 6 the free energy for $\Delta C_g/C_\Sigma^{(0)} = 0.6, 1.3$. Figure 5(b) shows that the conductance branch between points A and B is metastable: the free energy for this curve is larger than the free energy for the branch below. However, during the adiabatically slow increase of parameter Q the system does not switch to the lowest branch at point A; instead, it may go up to the metastable branch. The external perturbation can drive the system outside of the metastable branch before the bifurcation point. Usually, this "perturbation" plays the role of the Langevin forces induced by

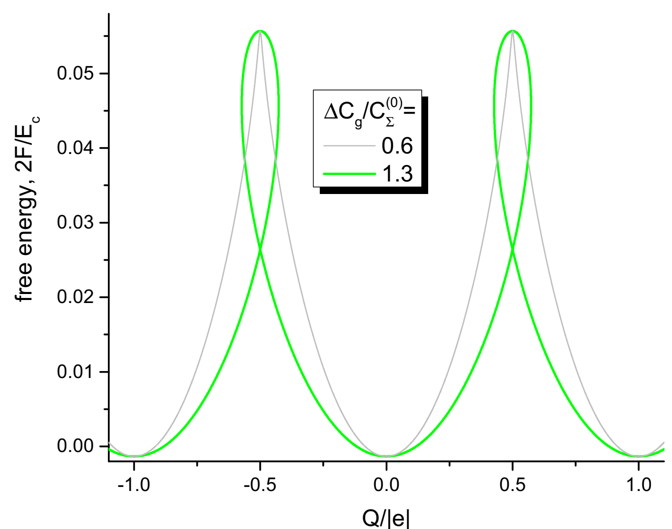

FIG. 6. (Color online) Free energy in Eq. (16) for $\Delta C_g/C_\Sigma^{(0)} = 0.6, 1.3$ and temperature $T = 0.2E_c^{(0)}$. The shape of the free-energy plot is similar to that of the conductance $G(Q)$ plot in Fig. 5(a).

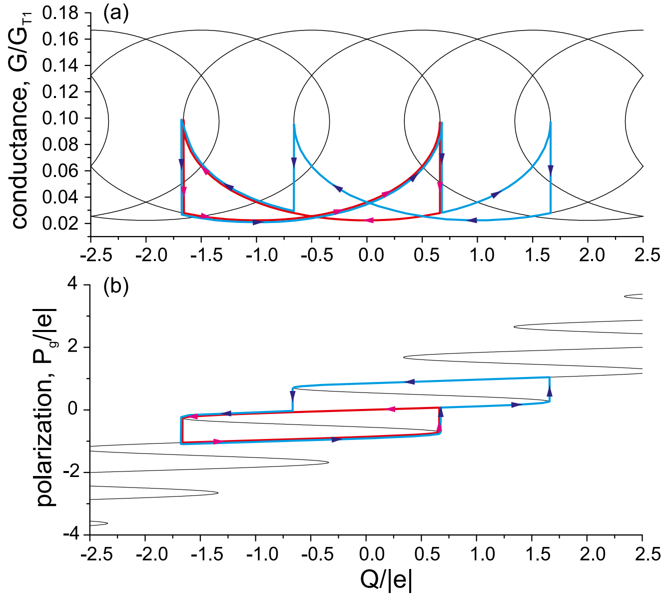

FIG. 7. (Color online) Memory effect in (a) the conductance and (b) the polarization of the gate insulator. The red hysteresis loop corresponds to the back and forth change of parameter Q in the interval $(-2,1)$, while the blue curve corresponds to the $(-2,2)$ interval. Parameters are $\Delta C_g = 7.5 C_\Sigma^{(0)}$, $T = 0.2\, E_c^{(0)}$, while $C_i^{(0)}$, $i = 1,2,g$ and R_j, $j = 1,2$, similar to Fig. 3.

the thermostat. In this case the jumps occur randomly within the same region before the bifurcation point. This scenario is typical for any hysteresis.

Intuitively, one may suppose that if conductance "jumps" from one branch to another, the final branch should have the lowest possible free energy for the parameter Q corresponding to the jump. Indeed, this is the case in Figs. 5(a)–5(c). However, in Figs. 5(d) and 5(f), this rule is violated. The system could jump, for example, to the point marked by the red ball in Fig. 5(d), instead of finishing at the point marked by the gray ball, which has a larger free energy. However, this energetically favorable transition is "forbidden": while continuously changing the polarization in such a process, the system would have to pass the energy barrier of approximately $E_c^{(0)}/4$ (free-energy maximum). Thus the higher-order jumps (over the average charge difference) are suppressed by the factor $\exp(-E_c^{(0)}/4T)$.

B. The fine structure of the memory effect

Performing numerical studies of the memory effect, we assumed that Q increases (or decreases) monotonically from minus to plus infinity (or vice versa). However, for large enough ΔC_g, when polarization induces more than one electron on the grain, the hysteresis loop depends on the interval where the parameter Q changes. This is shown in Fig. 7 with two possible hysteresis loops: The red hysteresis loop corresponds to a back and forth change of Q in the interval $(-2,1)$, while the blue curve corresponds to the interval $(-2,2)$. In the second case the larger hysteresis loop includes smaller loops. As a result, the understanding of the memory effect at finite intervals of Q evolution requires consideration of all branches of the SET observables such as conductance and polarization.

C. Analytical description of the conductance peaks and the memory effect

Here we present the analytical description of transport properties of a SET. At $V = 0$ and within the two-state approximation the form of the conductance peaks $G(Q)$ can be found using Eq. (15) with the proper substitution $Q^{(0)} \to Q'$, where Q' is defined in Eq. (12): with this substitution we have for conductance $G(Q) = G^{(0)}(Q')$. For the average potential, generalizing Eq. (14), we obtain

$$\langle \phi \rangle = \frac{e}{C_\Sigma^{(0)}} \left[\frac{1}{2} \tanh\left(\frac{E_c^{(0)}}{T} \frac{\delta Q'}{e} \right) - \frac{\delta Q'}{e} \right], \tag{17}$$

where $\delta Q'/e = \min_k [Q'/e - (k + 1/2)]$. Combining Eqs. (17) and (12), we find

$$\delta Q' \frac{C_\Sigma}{C_\Sigma^{(0)}} - \frac{e}{2} \frac{\Delta C_g}{C_\Sigma^{(0)}} \tanh\left(\frac{E_c^{(0)}}{T} \frac{\delta Q'}{e} \right) = \delta Q, \tag{18}$$

where $\delta Q = Q - (k + 1/2)e$ is the deviation of Q, k is the same as for $\delta Q'$, and $C_\Sigma = C_\Sigma^{(0)} + \Delta C_g$. It should be noted that the above equations are valid for any δQ as long as $\delta Q' \ll 1$.

1. *Small polarization*

Here we discuss the limit of small polarization, meaning that the induced charge on the island is small compared to the elementary charge e. Using the small parameter, $\Delta C_g / C_\Sigma^{(0)} \ll 1$, we expand Eq. (18) up to the second order,

$$(\delta Q')_0 = \delta Q \frac{C_\Sigma^{(0)}}{C_\Sigma}, \tag{19}$$

$$(\delta Q')_1 = (\delta Q')_0 + \frac{e}{2} \frac{\Delta C_g}{C_\Sigma} \tanh\left(\frac{E_c^{(0)}}{T} \frac{(\delta Q')_0}{e} \right). \tag{20}$$

The conductance now may be found by substituting $\delta Q^{(0)}$ with $(\delta Q')_{0,1}$ in Eq. (15):

$$G(\delta Q) = G^{(0)}(\delta Q'). \tag{21}$$

The numerical calculations in Fig. 8(a) show that the first-order approximation, Eq. (20), describes well the peak shape for small parameter $\Delta C_g / C_\Sigma^{(0)} \approx 0.1$, while the zero-order approximation is not sufficient. We note that $\Delta C_g / C_g^{(0)}$ and thus the renormalization of the conductance period over V_g can be arbitrary in this approximation.

2. *Amplitude and form of the conductance peak in the hysteresis regime*

The solution of Eq. (18) becomes ambiguous for large values of ΔC_g, where conductance $G(Q)$ acquires hysteresis. In this case the form of conductance peaks becomes non-symmetric, and the conductance $G(Q)$ has a maximum at the branching (bifurcation) point corresponding to the jump of the polarization. The bifurcation points in Eq. (18) can be found as follows:

$$\frac{d}{dQ'} \left[\delta Q' \frac{C_\Sigma}{C_\Sigma^{(0)}} - \frac{e}{2} \frac{\Delta C_g}{C_\Sigma^{(0)}} \tanh\left(\frac{E_c^{(0)}}{T} \frac{\delta Q'}{e} \right) \right] = 0, \tag{22}$$

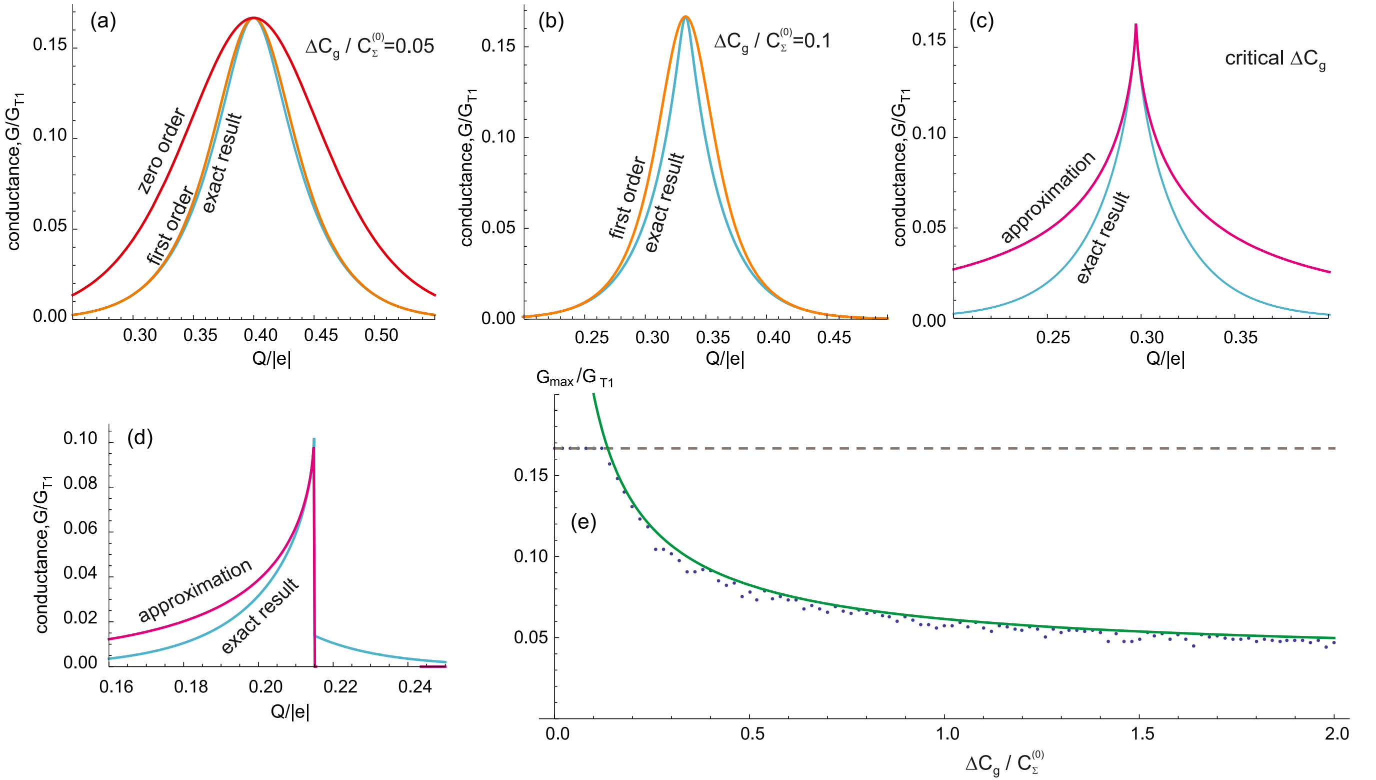

FIG. 8. (Color online) (a) Numerical solution for the conductance peak for $\Delta C_g/C_\Sigma^{(0)} = 0.05$ (blue line); the orange line is the zero-order solution from Eq. (19), and the red line is the first-order solution from Eq. (20). (b) Numerical and analytical solutions of conductance for $\Delta C_g/C_\Sigma^{(0)} = 0.1$. The first order approximates well the conductance peak at small ΔC_g. (c) Conductance at critical ΔC_g, where hysteresis appears. (d) Conductance hysteresis. (e) Amplitude of conductance peak vs ΔC_g. Points represent the numerical solution, the dashed curve is $G_{\max} = 1/2(R_1 + R_2)$, and the green solid curve shows Eq. (24) for $G_{\max}$. Parameters are $T = 0.06\, E_c^{(0)}$, while $C_1^{(0)}$, $C_2^{(0)}$, $C_g^{(0)}$, and $R_{1,2}$ are the same as in Fig. 3.

which reduces to

$$\cosh^2\left(\frac{E_c^{(0)}}{T}\frac{(\delta Q')_{\max}}{e}\right) = \frac{E_c^{(0)}}{2T}\frac{\Delta C_g}{C_\Sigma}. \tag{23}$$

The two solutions of Eq. (23) correspond to the increasing and decreasing evolution of Q (solutions with $\delta Q' < 0$ and $\delta Q' > 0$, respectively). These two solutions result in mirror-reflected shapes for the peaks, so we focus only on decreasing Q. For the conductance maximum we find

$$G_{\max} = \frac{1}{2(R_1+R_2)}\frac{\operatorname{arccosh}\left(\sqrt{\frac{E_c^{(0)}}{2T}\frac{\Delta C_g}{C_\Sigma}}\right)}{\sqrt{\frac{E_c^{(0)}}{2T}\frac{\Delta C_g}{C_\Sigma}\left(\frac{E_c^{(0)}}{2T}\frac{\Delta C_g}{C_\Sigma}-1\right)}}. \tag{24}$$

The predicted conductance maximum amplitude variation is shown in Fig. 8. One can see that the curve breaks at the critical value of ΔC_g, indicating the start of the hysteresis regime.

We note that since, within the scope of the two-state approximation and for ΔC_g above the critical value, Eq. (24) gives the exact maximum, its applicability depends only on temperature. At finite ΔC_g the conductance maximum does not exactly correspond to a degeneracy point $\delta Q' = 0$, but still $\delta(Q')_{\max} \ll 1$ for $T \ll E_c^{(0)}$. For example, for temperature $T = 0.06E_c^{(0)}$ and $\Delta C_g \to \infty$ we have $\delta(Q')_{\max}/|e| \approx 0.1 \ll 1$, meaning that our consideration is valid (see Fig. 8).

Now we find the form of the conductance peaks. Expanding Eq. (18) up to the second order near $\delta(Q')_{\max}$, we obtain

$$A_0 + A_2[\delta Q' - \delta(Q')_{\max}]^2 = \delta Q, \tag{25}$$

where

$$A_0 = \frac{eT}{E_c^{(0)}}\frac{C_\Sigma}{C_\Sigma^{(0)}}\operatorname{arccosh}\left(\sqrt{\frac{E_c}{2T}\frac{\Delta C_g}{C_\Sigma}}\right) - \frac{e}{2}\frac{\Delta C_g}{C_\Sigma^{(0)}}\sqrt{1-\frac{2T}{E_c^{(0)}}\frac{C_\Sigma}{\Delta C_g}} \tag{26}$$

and

$$A_2 = \frac{E_c^{(0)}}{eT}\frac{C_\Sigma}{C_\Sigma^{(0)}}\sqrt{1-\frac{2T}{E_c^{(0)}}\frac{C_\Sigma}{\Delta C_g}}. \tag{27}$$

It follows from Eqs. (25) and (21) that the conductance derivative in δQ diverges as $1/\sqrt{x}$ near its maximum value.

3. The peak form at the bifurcation point

To find the conductance peak at the critical value of ΔC_g we expand the hyperbolic tangents in Eq. (18) up to the third order. As a result, we obtain

$$\delta Q'\left[1 - \frac{\Delta C_g}{C_\Sigma^{(0)}}\left(\frac{E_c^{(0)}}{2T} - 1\right)\right] + \frac{e\Delta C_g}{6C_\Sigma^{(0)}}\left(\frac{E_c^{(0)}}{T}\frac{\delta Q'}{e}\right)^3 = \delta Q. \tag{28}$$

The linear term equals zero at the critical point. For critical polarizability of the gate insulator we find

$$\Delta C_g^{(c)} = C_\Sigma^{(0)}\left(E_c^{(0)}/2T - 1\right)^{-1}. \tag{29}$$

Also we find that

$$\delta Q' = \frac{eT}{E_c^{(0)}}\sqrt[3]{6\frac{\delta Q}{e}\left(\frac{E_c^{(0)}}{2T} - 1\right)}. \tag{30}$$

Using Eq. (21), we find that the peak maximum can be approximated with the function $1/(1+x^{2/3})$ (here $x \propto \delta Q$), while the derivative diverges at the conductance maximum as $1/\sqrt[3]{x}$. As follows from Fig. 8(c) and Eq. (30), this approximation for conductance works well only near its maximum value.

IV. SINGLE-ELECTRON TUNNELING THROUGH A SLOW DIELECTRIC LAYER

A. Conductance peaks with slow dielectrics in all capacitors

Here we consider the general case, with slow dielectric layers in all capacitors with polarizabilities ΔC_1, $\Delta C_2, \Delta C_g$. Using Eq. (12), we find

$$Q' = Q + \Delta C_\Sigma \langle\phi\rangle(Q',V) - (\Delta C_2 - \Delta C_1)\frac{V}{2}, \tag{31}$$

where we introduce the parameter

$$\Delta C_\Sigma = \sum_{i=1,2,g} \Delta C_i. \tag{32}$$

Here we explicitly show that the functions Q' and $\langle\phi\rangle$ depend on voltage V. In general, this dependence results in an additional contribution to the conductance proportional to $\partial Q'/\partial V$:

$$G(Q,V) = \frac{\partial I^{(0)}(Q',V)}{\partial V} = G^{(0)}(Q',V) + \frac{\partial I^{(0)}(Q',V)}{\partial Q'}\frac{\partial Q'}{\partial V}, \tag{33}$$

where $I^{(0)}(Q,V)$ is the current in the orthodox theory, generally not limited by the two-state approximation. However, the current I is zero for zero bias voltage for any Q; therefore the last term can be omitted at $V = 0$. This explains why in a two-state approximation we can calculate the conductance by replacing Q by Q' in Eq. (15) for the orthodox theory.

For zero voltage, $V = 0$, Eq. (31) reduces to

$$Q' = Q + \Delta C_\Sigma \langle\phi\rangle(Q'). \tag{34}$$

Then

$$\delta Q'\left(1 + \frac{\Delta C_\Sigma}{C_\Sigma^{(0)}}\right) - \frac{e}{2}\frac{\Delta C_\Sigma}{C_\Sigma^{(0)}}\tanh\left(\frac{E_c^{(0)}}{T}\frac{\delta Q'}{e}\right) = \delta Q. \tag{35}$$

As we can see, the only distinction between Eqs. (35) and (18) is the replacement of ΔC_g with ΔC_Σ. It follows that for $V = 0$ the SET with slow insulators in tunnel junctions behaves qualitatively similar to the only $\Delta C_g > 0$ that was considered previously. The only difference is related to the fact that the slow dielectric in the gate capacitor renormalizes the period of the Q oscillations of conductance, while slow dielectrics in all other capacitors of the SET do not.

Now, we can generalize our results for positive $\Delta C_g > 0$ obtained earlier. In particular, the critical polarization, where the memory effect in the conductance $G(Q)$ first appears, becomes the integral quantity [see Eq. (32)] that includes properties of all the slow dielectric layers:

$$\Delta C_\Sigma^{(c)} = C_\Sigma^{(0)}\left(E_c^{(0)}/2T - 1\right)^{-1}. \tag{36}$$

The amplitude of the conductance peaks can be found using the substitution $\Delta C_g \to \Delta C_\Sigma$ in Eq. (24). The shape of the peaks can be obtained using the same substitution in the equations in Sec. III C 3, where still $\delta Q = -(C_g^{(0)} + \Delta C_g)V_g$.

B. Memory effect in current-voltage characteristics

Above we discussed the properties of a SET with slow dielectric barriers, related to the variation of the gate voltage V_g at bias $V = 0$. In this section we instead concentrate on the current-voltage characteristic $I(V)$ of a SET in the case of electron tunneling through a slow insulator in the left and the right capacitors (see Fig. 1). We neglect the gate to simplify the situation, thus putting $C_g = 0$. Such systems have been extensively studied in experiments over the last two decades. They can exhibit Coulomb blockade at room temperature [21,29–31], and their ease of fabrication makes a wide range of barrier materials available for experiments. Following Ref. [21], we consider the current-voltage characteristic of the SET in a wide range of bias voltages.

The typical current-voltage characteristics $I(V)$ are shown in Fig. 9; in Figs. 9(a)–9(c) the coefficients $\Delta C_2 = 0$ and ΔC_1 are finite. It follows that there is a memory effect in $I(V)$ at large enough ΔC_1, and this effect depends on the direction of the bias-voltage evolution. The jumps in Fig. 9(b) correspond to the regions of hysteresis, while the arrows show the evolution of the voltage. Figure 9(c) shows the hysteresis in $I(V)$ for $\Delta C_1/C_\Sigma^{(0)} = 3.5$. The current-voltage characteristics may have many hysteresis loops, depending on the amount of electron charge that the dielectric polarization may induce on the grain. The hysteresis in the current-voltage characteristics appears for the first time for ΔC_1 larger than $C_\Sigma^{(0)}$. This is the first critical value of polarization. For $\Delta C_1 \gtrsim 2C_\Sigma^{(0)}$ the second hysteresis loop appears in $I(V)$. Therefore this is the second critical value of ΔC_1. For larger values of ΔC_1 we expect a further increase in the number of hysteresis loops.

Two cases of current-voltage characteristics are compared in Figs. 9(d) and 9(e): (i) finite ΔC_1 and zero ΔC_2 and (ii) $\Delta C_1 = \Delta C_2$. In both cases the set of critical values of ΔC is the same, and for large bias voltage the current-voltage characteristics asymptotically coincide.

Figure 9 shows that the current-voltage characteristics of the SET strongly depend on the direction of bias voltage V. Moreover, for a given hysteresis branch

$$I(V) \neq -I(-V), \tag{37}$$

which happens in the absence of Q and is notably different from the result for a regular SET.

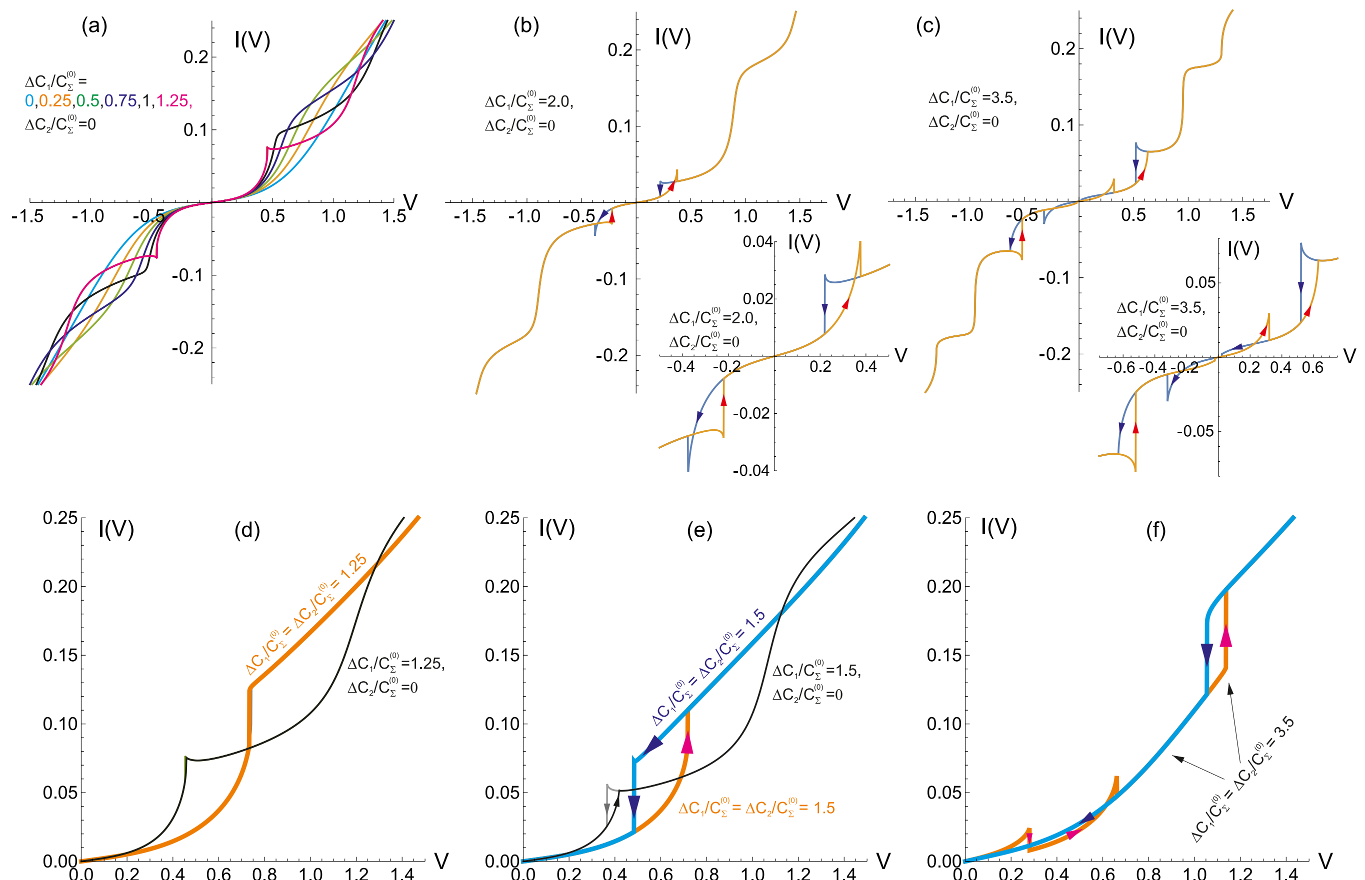

FIG. 9. (Color online) Current-voltage characteristics $I(V)$ of a SET with zero gate capacitance, $C_g = 0$. (a) $I(V)$ for $\Delta C_1/C_\Sigma^{(0)} = 0.0, 0.25, 0.5, 0.75, 1.0, 1.25$. Smoother curves correspond to smaller ΔC_1. (b) $\Delta C_1/C_\Sigma^{(0)} = 1.5$. The jumps in $I(V)$ in (b), (c), (e), and (f) correspond to the memory effect: the branch depends on the direction of the voltage change. (c) $I(V)$ for $\Delta C_1/C_\Sigma^{(0)} = 3.5$. The $I(V)$ curve can have many hysteresis loops depending on the amount of electron charge induced on the grain by the dielectric polarization. Insets in (b) and (c) show the details of the hysteresis. (d) $I(V)$ for $\Delta C_1/C_\Sigma^{(0)} = 1.25$, $\Delta C_2/C_\Sigma^{(0)} = 0$ (black curve) and $\Delta C_1/C_\Sigma^{(0)} = \Delta C_2/C_\Sigma^{(0)} = 1.25$ (orange curve); (e) graphs for $\Delta C_1/C_\Sigma^{(0)} = 1.5$, $\Delta C_2/C_\Sigma^{(0)} = 0$ (black curve) and $\Delta C_1/C_\Sigma^{(0)} = \Delta C_2/C_\Sigma^{(0)} = 1.5$ (orange and blue curves). (f) $I(V)$ for $\Delta C_1/C_\Sigma^{(0)} = \Delta C_2/C_\Sigma^{(0)} = 3.5$. Parameters are $T = 0.06\, E_c^{(0)}$, $C_1^{(0)} = 0.6 C_\Sigma^{(0)}$, $C_2^{(0)} = 0.4 C_\Sigma^{(0)}$, and R_i, $i = 1,2$, similar to Fig. 3. The unit of voltage is $E_c^{(0)}/|e|$, and the current is normalized to $E_c^{(0)}/|e| R_{T1}$.

C. Influence on the Coulomb staircase

By the Coulomb staircase in this section we mean a steplike behavior of $I(V)$ in the regime of Coulomb blockade. The Coulomb staircase is often used as an indication of Coulomb blockade (Refs. [21,29,32–34]). In the following we show how the slow polarization influences the shape of the staircase. Again, we take $C_g = 0$ and consider the conditions when the staircase is the most pronounced, i.e., $T = 0$ and strongly asymmetric barriers $R_1 \gg R_2$. At zero temperature tunneling may occur only in the direction of chemical potential drop, that is, from the first electrode to the second, assuming $V > 0$. Due to the relatively high tunneling rate through the second electrode, the number of excess electrons on the island almost always stays at the minimum energetically allowed number $n_{\min}$. It can be determined as the lowest n for which $\Delta F_2^{n+1\to n} < 0$ is true since $\Delta F_1^{n\to n+1} < 0$ holds for any $n < 0$. For a given $n_{\min}$ the current can be calculated as

$$I = \frac{1}{eR_1} \Delta F_1^{n_{\min}\to n_{\min}+1}, \tag{38}$$

where ΔF_1 is the free-energy change on tunneling through the first electrode. For a conventional SET the above formula leads to a staircase-shaped $I(V)$ characteristic with the step width

$$\Delta V_{\text{step}} = |e|/C_1^{(0)}, \tag{39}$$

jumps of the current between the steps

$$\Delta I_{\text{step}} = |e|/R_1 C_\Sigma^{(0)}, \tag{40}$$

and the $I(V)$ slope between the jumps

$$dI/dV = C_2^{(0)} V / C_\Sigma^{(0)} R_1. \tag{41}$$

Introducing slow dielectric into the tunnel junctions results in some new effects (for the details of the calculations see Appendix B). At $V > |e|/C_\Sigma^{(0)}$ slow polarization leads to the rescaling of the staircase, which may be described by substituting the capacitances in Eqs. (39)–(41) by the new values $C_i = C_i^{(0)} + \Delta C_i$, exactly like when dealing with a conventional fast dielectric [see Fig. 10(b)]. Contrary to the fast dielectric, the slow one shifts the staircase, making it

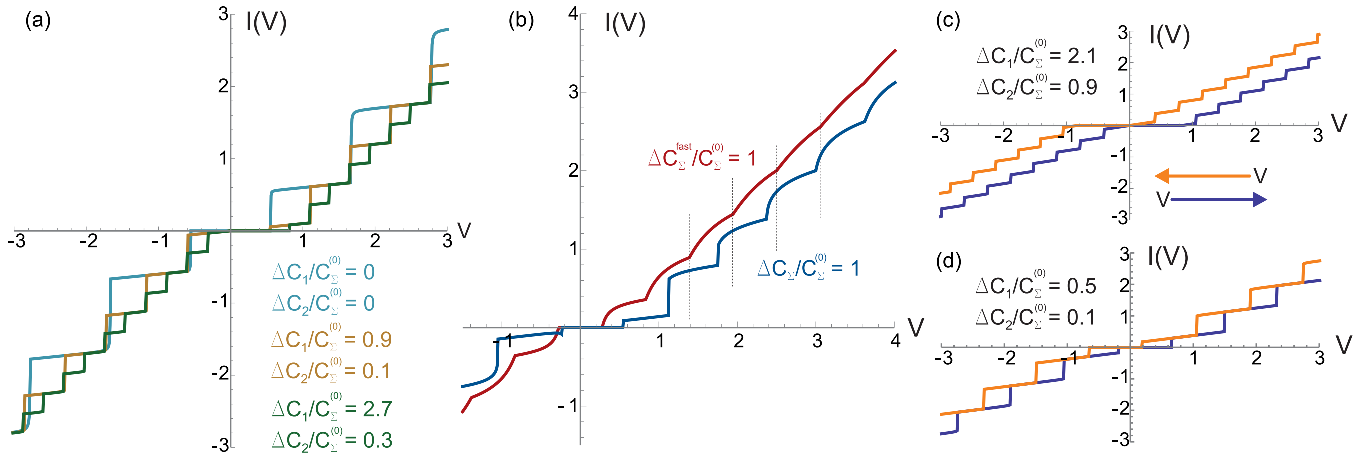

FIG. 10. (Color online) Current-voltage characteristics $I(V)$ of a SET demonstrating the Coulomb staircase at $T = 0$, $C_g = 0$. (a) $I(V)$ in the regime in which the scaling of the Coulomb staircase steps at large V is the same for slow and fast dielectric responses. Here $R_2/R_1 = 10^{-3}$, $C_1^{(0)} = 0.9C_\Sigma^{(0)}$, $C_2^{(0)} = 0.1C_\Sigma^{(0)}$. (b) The regime in which the periods of Coulomb staircases for slow (blue curve) and fast (red curve) dielectrics of the same static polarizabilities are different. $R_2/R_1 = 0.25$, $C_1^{(0)} = 0.9C_\Sigma^{(0)}$, $C_2^{(0)} = 0.1C_\Sigma^{(0)}$. (c) and (d) The shifts of the staircases arising from the hysteretic behavior of $I(V)$ for a SET with slow dielectrics. Arrows indicate the directions of voltage change for each curve. Here $R_2/R_1 = 10^{-3}$, $C_1^{(0)} = 0.7C_\Sigma^{(0)}$, $C_2^{(0)} = 0.3C_\Sigma^{(0)}$. The unit of voltage is $|e|/C_\Sigma^{(0)}$, and current is measured in $|e|/C_\Sigma^{(0)}(R_1 + R_2)$.

asymmetric and, moreover, dependent on the direction of the evolution of V, as illustrated in Figs. 10(c) and 10(d).

Interestingly, the shift in the $I(V)$ curve in experiments is a well-known effect. It is usually accounted for by assuming the presence of some additional spurious charge Q, induced on the grain (as in Refs. [21,33]). However, the shift that we predict is notably different, at least in one aspect: it reverses its sign with the direction of the evolution of V.

We stress that the described rescaling and shift of $I(V)$ take place only under specific conditions $V > |e|/C_\Sigma^{(0)}$ and $R_1 \gg R_2$. If R_2 are of the same order, the introduction of the slow dielectric may change the staircase steps in a more complex way. Such a situation is shown in Fig. 10(b), where the staircase period does not correspond to the one we would expect from the simple capacitance-renormalization consideration. If R_1/R_2 is even closer to unity, the slow dielectric barriers qualitatively change the current-voltage curve, as was discussed in the previous section (see Fig. 9).

V. DISCUSSION

Before we discuss the specific features of our SET model, here we briefly mention the limitations and a possible direction of further investigations. Metallic island is characterized by an important parameter: δE, the mean spacing of single-electron levels. Here we focus on a relatively large metallic island where δE is the smallest energy parameter: $\delta E \ll T \ll E_c^{(0)}$. However, if, for example, the diameter of the metallic island is 5 nm or smaller and $T \sim 300$ K, δE may already become comparable to T. (Semiconductor quantum dots achieve this limit for much larger diameters.) This case has been extensively debated for SETs [35]. Then solving the transport problem for a SET with an active dielectric, we should take into account the level statistics and calculate accordingly the statistics of the peak heights in the methods generalizing the Coulomb-blocked transport problem developed in Refs. [36–39]. We leave this calculation for a forthcoming paper.

A. Requirements for dielectric materials

Here we discuss several possible dielectric materials which can be considered slow insulators. At finite external electric field the localized electric charges are shifted, and the dielectric material is polarized. There are several physical processes contributing to the polarization: (1) the shift and deformation of the electron cloud, (2) the shift of ions in the lattice, and (3) the molecular and/or macrodipole reorientation. Electrons, ions, and dipoles can form a different polarization. The slowest polarization formation corresponds to the electrocaloric and migration (electron, ion, or dipole) mechanisms with the characteristic dispersion frequency being in the range 10^{-4}–10^{-1} and 10^{-3}–10^{3} Hz, respectively, at temperature $T = 300$ K. The electromechanical mechanism corresponds to frequencies of 10^5–10^8 Hz, while the thermal mechanism corresponds to 10^5–10^{10} Hz. The dielectrics for which the thermal mechanism is the largest are promising for applications in nanostructures and can be considered slow dielectrics.

Dithiol self-assembled monolayers (SAMs) have a static dielectric permittivity $\epsilon(\omega = 0) \sim 3$ and a characteristic relaxation frequency of $\sim 10^4$ Hz [22]. These materials are good candidates for slow dielectrics. Such dielectric layers have been used in double-junction SETs [21]. The hysteresis has not been observed in these experiments, but there was a considerable discrepancy between the values of the capacitances obtained from the fit of the experimental data with the orthodox model and the *ab initio* calculations.

Other promising materials to observe the hysteresis are polar crystal dielectrics, e.g., $BaTiO_3$ and potassium dihydrogen phosphate, with static dielectric permittivity $\epsilon(\omega = 0) \sim 10^3$ and a typical relaxation frequency $\omega_c \sim 10^6$ Hz.

B. Fast capacitances

Here we discuss the geometric capacitance $C_i^{(0)}$, $i = 1,2,g$. We assumed that these capacitances have an electrostatic origin. However, in a rigorous analysis they include the high-frequency dielectric permittivity ϵ_∞(usually between 1 and 10). Thus in our consideration the slow polarizability α_i is the difference between the low- and high-frequency α_i. As an example, for $BaTiO_3$ the difference between the high- and low-frequency permittivities ϵ is $\sim 10^3$. This difference is large enough.

C. Critical polarization

The effects of slow polarization are governed by the ratio of slow and fast capacitances $\Delta C_\Sigma/C_\Sigma^{(0)}$. If a capacitor is fully filled with a dielectric with permittivity $\epsilon(\omega)$, then $\Delta C_\Sigma/C_\Sigma^{(0)} = [\epsilon(0) - \epsilon(\infty)]/\epsilon(\infty)$. It follows from Secs. III and IV that at $\Delta C_\Sigma/C_\Sigma^{(0)} \sim 1$ the strong influence of slow polarization may be observed, thus requiring $\epsilon(0) \gtrsim 2\,\epsilon(\infty)$.

The latter requirement becomes even less strict at lower temperatures. In particular, the critical value of $\epsilon(0)^{(c)}/\epsilon(\infty)$ to observe the breakdown of conductance peaks goes to 1 as $T \to 0$ [see Eq. (36)]. For the conditions in Fig. 8(e) $\epsilon(0)^{(c)} \approx 1.14\,\epsilon(\infty)$.

D. Temperature dependence of the Coulomb-blockade effects

A well-known consequence of the orthodox theory of the SET is that in order to experimentally observe the Coulomb-blockade phenomenon, the temperature of the system should be lower than $E_c = e^2/2C_\Sigma$. Here the total capacitance C_Σ includes dielectric susceptibility of the barrier media. In contrast, our numerical calculations show that if the dielectric response is sufficiently slow, only the ratio $E_c^{(0)}/T$ should be taken into account when considering the blurring of the Coulomb effects due to finite temperature. This must result in a more pronounced blockade for a system with a slow dielectric at a given temperature and electrode geometry, as illustrated in Fig. 11.

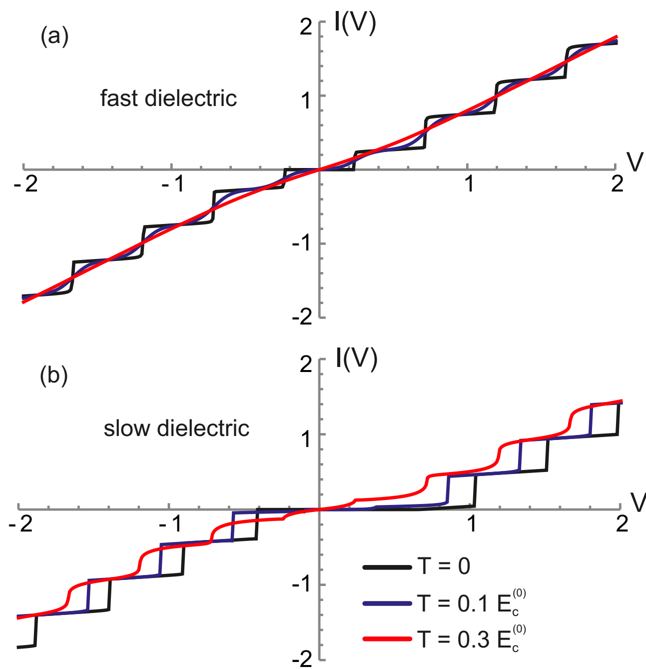

FIG. 11. (Color online) Temperature dependence of the Coulomb staircase in $I(V)$ characteristics of (a) a regular SET and (b) a SET with slow dielectrics in the tunnel barrier. In (b) the SET parameters are $C_1^{(0)} = 0.7C_\Sigma^{(0)}$, $C_2^{(0)} = 0.3C_\Sigma^{(0)}$, $\Delta C_1 = 1.4C_\Sigma^{(0)}$, $\Delta C_2 = 0$. In (a) $C_1 = 2.1C_\Sigma^{(0)}$ and $C_2 = 0.3C_\Sigma^{(0)}$. For both plots $R_2/R_1 = 10^{-3}$, and in (b) $I(V)$ is shown for increasing voltage V. The unit of voltage is $|e|/C_\Sigma^{(0)}$, and the current is measured in $|e|/C_\Sigma^{(0)}(R_1 + R_2)$.

VI. CONCLUSIONS

We showed that the dielectric materials at the nanoscale demonstrate distinct physical phenomena. As an example we studied the single-electron transistor. We found the memory effect in the conductance-gate voltage dependence and in the current-voltage characteristics of the SET. We uncovered the complex fine structure of the hysteresis effect, where the large hysteresis loop may include a number of smaller loops. We also found that in order to estimate the influence of temperature on the electronic transport one should compare T with $e^2/2C_\Sigma^{(0)}$, where in $C_\Sigma^{(0)}$ the slow part of the dielectric function is not included.

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APPENDIX A: CALCULATION OF THE COULOMB ENERGY CHANGE ON ELECTRON JUMPS

Here we show how the energy changes $\Delta U_n^\pm$ are calculated. If the number of electrons on the island changes from n to $n \pm 1$ in some process, then the electrostatic energy change is

$$\Delta U_n^\pm = \int_n^{n\pm1} \sum_i (\phi - V_i) dq_i = \int_n^{n\pm1} \sum_i (\phi - V_i)\big(C_i^{(0)} d\phi + S_i dP_i\big), \quad \text{(A1)}$$

where q_i are the charges of the capacitors and P_i are dielectric polarizations in barriers. For fast and slow dielectrics P_i behave differently during the process of electron jumps. If the dielectric response is fast, P_i follows ϕ, which results in capacitance renormalization. For slow dielectric layers the polarization cannot change on the electron-jump time scale,

and thus $dP = 0$, yielding

$$\Delta U_n^{\pm} = \frac{1}{2}\sum_i C_i^{(0)}(\phi - V_i)^2\Big|_{\phi(n)}^{\phi(n\pm 1)}. \quad \text{(A2)}$$

$\phi(n)$ are calculated using the charge balance equation (3),

$$\phi(n) = \frac{1}{C_\Sigma^{(0)}}\left[e\left(n - \sum_i P_i S_i/e\right) + \sum_i C_i^{(0)} V_i\right]. \quad \text{(A3)}$$

Here P_i are constant and do not depend on n. By inserting Eq. (A3) into (A2) we obtain Eq. (9).

APPENDIX B: THE SHAPE OF THE COULOMB STAIRCASE

At zero temperature the tunneling rates for the electron to and from the island are

$$\Gamma_{1,2}^{n\to n\pm 1} = \frac{1}{e^2 R_{1,2}}\left(-\Delta F_{1,2}^{n\to n\pm 1}\right)\Theta\left(-\Delta F_{1,2}^{n\to n\pm 1}\right), \quad \text{(B1)}$$

where n is the number of excess electrons on the island and tunneling happens through the first or second electrode. Free-energy changes $\Delta F_{1,2}$ on jumps are

$$\Delta F_1^{n\to n\pm 1} = \frac{e}{C_\Sigma^{(0)}}\left[\frac{e}{2} \pm (ne - Q') \pm C_2^{(0)} V\right], \quad \text{(B2)}$$

$$\Delta F_2^{n\to n\pm 1} = \frac{e}{C_\Sigma^{(0)}}\left[\frac{e}{2} \pm (ne - Q') \mp C_1^{(0)} V\right]. \quad \text{(B3)}$$

Consider $V > 0$. It follows from (B1) that tunneling occurs if for some n simultaneously $\Delta F_1^{n\to n+1} \leqslant 0$ and $\Delta F_2^{n+1\to n} \leqslant 0$ (there is no backward tunneling at $T = 0$). These conditions may be combined into

$$Q'/e - 1/2 + C_1^{(0)} V/e \leqslant n \leqslant Q'/e - 1/2 - C_2^{(0)} V/e. \quad \text{(B4)}$$

Since the tunneling from the first electrode to the island is much slower than that from the island to the second electrode ($R_1 \gg R_2$), the number of electrons on the island almost constantly stays at its lowest energetically allowed value $n_{\min}$. The current is then

$$I = -e\frac{\Gamma_1^{n\to n+1}\Gamma_2^{n+1\to n}}{\Gamma_1^{n\to n+1} + \Gamma_2^{n+1\to n}} \approx -e\Gamma_1^{n_{\min}\to n_{\min}+1}. \quad \text{(B5)}$$

What remains is to calculate $n_{\min}$. Since we neglect C_g, only the charge induced by the slow polarization gives rise to Q',

$$Q' = \frac{\Delta C_\Sigma}{C_\Sigma} n_{\min} e + \frac{\Delta C_1 C_2^{(0)} - \Delta C_2 C_1^{(0)}}{C_\Sigma} V. \quad \text{(B6)}$$

$n_{\min}$ can be determined from the equation

$$\left\lceil -\frac{1}{2} - \frac{n_{\min}}{1 + \Delta C_\Sigma / C_\Sigma^{(0)}} + \frac{C_1}{\left(1 + \Delta C_\Sigma / C_\Sigma^{(0)}\right)}\frac{V}{e}\right\rceil = 0, \quad \text{(B7)}$$

where $\lceil x \rceil$ denotes the lowest integer larger than x. It worth noting that Eq. (B7) predicts multiple solutions for $n_{\min}$ at V close to the current jump points if $\Delta C_\Sigma > 0$ [see Fig. 10(d)].

The calculation of I yields

$$I(V) = \frac{1}{R_1 C_\Sigma}\left(\frac{e}{2}\frac{C_\Sigma}{C_\Sigma^{(0)}} + n_{\min} e + C_2 V\right). \quad \text{(B8)}$$

The latter formula demonstrates the full renormalization of capacitances and a shift in the $I(V)$, as illustrated in Fig. 10(a).

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