Hard x-ray photoelectron spectroscopy and electrical characterization study of the surface potential in metal/Al_2O_3/GaAs(100) metal-oxide-semiconductor structures

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Hard x-ray photoelectron spectroscopy (HAXPES) has been used to study metal-oxide-semiconductor (MOS) structures fabricated with both high (Ni) and low (Al) work-function metals on 8-nm thick Al_2O_3 dielectric layers, deposited on sulfur passivated *n*- and *p*-doped GaAs substrates. A binding energy difference of 0.6 eV was measured between the GaAs core levels of the *n*- and *p*-doped substrates in the absence of gate metals, indicating different Fermi level positions in the band gap. Subsequent photoemission measurements made on the MOS structures with the different work-function metals displayed very limited change in the GaAs core level binding energies, indicating that the movement of the Fermi level at the Al_2O_3/GaAs interface is restricted. Using a combination of HAXPES measurements and theoretical calculations, the Fermi level positions in the band gap have been determined to be in the range of 0.4–0.75 eV and 0.8–1.11 eV above the valence band maximum for *p*- and *n*-type GaAs, respectively. Analysis of capacitance voltage (C-V) measurements on identically prepared samples yield very similar Fermi level positions at zero applied gate bias. The C-V analysis also indicates a higher interface defect density (D_{it}) in the upper half of the GaAs bandgap.

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I. INTRODUCTION

The recent increased interest in the nondestructive analysis of buried interfaces, such as those in metal oxide semiconductor (MOS) structures, has been facilitated by the development of a high energy variant of x-ray photoelectron spectroscopy (XPS) known as hard-XPS (HAXPES). The increase in the analysis depth, from 5–7 nm for conventional XPS up to 15–30 nm for HAXPES,[1–4] facilitates the measurement of core level signals from all the relevant layers in MOS structures which can also be electrically characterized by capacitance-voltage (C-V) techniques. The ability of HAXPES measurements to provide information on band bending at the semiconductor/dielectric interface and to detect the presence of a potential difference across the dielectric provides complementary information on the electronic structure of the MOS to that deduced from C-V measurements.[5] This is of particular interest in cases where it is difficult to extract definitive information from conventional C-V analysis due to high interface state densities, as is the case with GaAs.[6]

In this paper we report on a study exploring the application of HAXPES analysis to determine the surface Fermi level position in *n*- and *p*-doped GaAs MOS structures, where the oxide is an Al_2O_3 (8-nm) thin film deposited by atomic layer deposition (ALD). The samples studied included Al_2O_3/GaAs structures with no metal gates and samples capped with 5-nm thick high (Ni) and low (Al) work-function metals, to explore if the low and high work-function metal layers modulate the surface Fermi level position. Using a photon energy of 4150 eV in these investigations allowed the detection of photoemission signals from metal, oxide, and substrate core levels. The relatively wide band gap of GaAs (1.42 eV) increases the possibility of detecting differences in the binding energy (BE) of the *n*- and *p*-doped substrate core levels which directly reflect different Fermi level positions in the band gap.[7] The surface Fermi level positions obtained from the HAXPES analysis are compared to the reported location of the pinning positions in the GaAs band gap for *n*- and *p*-doped substrates from other studies.[8–10]

In conjunction with the HAXPES analysis, Al_2O_3/GaAs MOS samples with *n*- and *p*-doped GaAs substrates and Ni or Al gate contacts were examined using C-V analysis. The GaAs/oxide interface is known to display capacitance-voltage characteristics in MOS devices indicative of a high density of interface states, which restricts the movement of the Fermi level at the GaAs/oxide interface upon application of a gate voltage. To fully characterize the interfacial electronic properties in the high-κ/GaAs MOS system it is necessary to determine the energy distribution of the interface states. In the case of an MOS system with a high interface state density, such as GaAs, the conversion of the gate voltage in the C-V response to the corresponding energy position in the interface state analysis is an established problem.[11] It would be highly beneficial to the community working in the electrical characterization of III-V MOS interface states

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to have an independent method of evaluating the surface potential for a given gate voltage, as this would provide a higher degree of certainty for energy mapping of the interface states.

The results presented in this paper illustrate the ability of HAXPES to detect Fermi level positions at the GaAs/dielectric interface, and the presence of any potential differences across the dielectric layers. The results from the HAXPES analysis are also compared to the analysis of the C-V response, and a good agreement is obtained for the surface Fermi level position for the case of zero applied gate voltage (V_g).

II. EXPERIMENTAL

The n- (Si, 5×10^{17} cm^{-3}) and p- (Zn, 5×10^{17} cm^{-3}) doped GaAs samples consisted of 400-nm thick GaAs layers grown by metal organic vapor-phase epitaxy (MOVPE) on epi-ready GaAs substrates. The samples received a surface treatment using a 10% solution of $(NH_4)_2S$ in deionized water for 20 min at room temperature immediately prior to being transferred into the ALD chamber with less than 3 min air exposure.[12] The 8-nm Al_2O_3 was deposited by ALD at 300 °C using alternating TMA ($Al(CH_3)_3$) and H_2O pulses. The samples were split into three groups: A, B, and C, each containing one n- and one p-type GaAs sample. Group A was left without a metal gate, group B was capped with a 5-nm Ni blanket film, while group C was capped with a 5-nm Al blanket film. All metal deposition was achieved by electron beam evaporation. Additionally, two further groups, D and E were produced for C-V analysis in an identical fashion to that mentioned above, with group D samples capped with a 160-nm Al film, while group E samples were capped with a 70/90 nm Ni/Au film for electrical probing. The metal gate areas for the C-V characterization were defined by a lithography and lift-off process.

HAXPES measurements were carried out on the NIST beamline X24A at the National Synchrotron Light Source (NSLS) at Brookhaven National laboratory (BNL). A double Si (111) crystal monochromator allowed for photon energy selection in the range of 2.1–5.0 keV. An electron energy analyzer was operated at a pass energy of 200 eV giving an overall instrumental energy resolution of 0.52 eV at the chosen photon energy of 4150 eV. In order to ensure correct energy calibration throughout the experiment, metallic Ni Fermi edge reference spectra were acquired immediately before and after the acquisition of the Al_2O_3 and GaAs substrate core level peaks. The resultant error associated with this photon energy correction procedure is estimated to be no more than 50 meV. The maximum depletion region width for the 5×10^{17} cm^{-3} doped GaAs substrate is calculated to be 61 nm. The total sampling depth of the HAXPES measurement using a photon energy of 4150 eV is estimated to be 23 nm[13] which ensures the detection of photoemitted electrons from the 5-nm metal and 8-nm dielectric layers, as well as approximately 10 nm into the GaAs, which is obtained from the inelastic mean free path of the As $2p$ photoemitted electrons, which have kinetic energies of 2827 eV.[14] The XPS core level spectra were curve fitted, using Voigt profiles composed of Gaussian and Lorentzian line shapes in a 3:1 ratio with a Shirley-type background, to increase the accuracy of locating the peak centers.

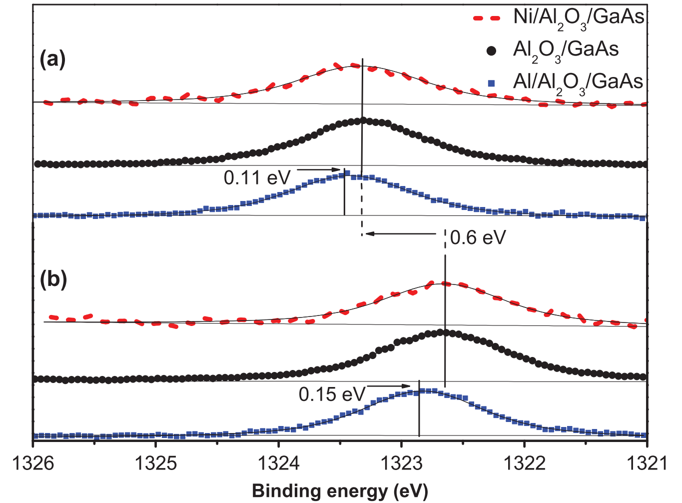

FIG. 1. (Color online) Normalized As $2p$ core level spectra acquired at a photon energy of 4150 eV for the uncapped Al_2O_3/GaAs, Ni (5 nm) capped and Al (5 nm) capped Al_2O_3/GaAs samples, showing the shifts in the core level after metal for (a) n-type, and (b) p-type GaAs substrates. The dotted lines show the energy separation between n- and p-type samples without metal gates.

III. RESULTS AND DISCUSSION

Figure 1 shows the As $2p$ core levels acquired at 4150 eV photon energy for both n- and p-doped GaAs with the 8-nm Al_2O_3 dielectric layer, with and without the presence of a metal overlayer. Measurements on the uncapped samples reveal that the binding energy position for the p-type GaAs peaks was found to be 0.6 eV lower than the n-type substrate consistent with the Fermi level residing closer to the valence band maximum. The difference is however less than the expected value of 1.34 eV, which is based on the calculated Fermi level position difference for n and p GaAs with a doping concentration of 5×10^{17} cm^{-3}, indicating that there is band bending at the Al_2O_3/GaAs interface for both dopant types, even in the absence of a metal contact.[15]

In order to determine whether the band bending displayed at the interface reflected Fermi level pinning, both high (Ni 5.01 eV) and low (Al 4.08 eV) work-function metal films 5-nm thick were deposited on the dielectric.[16] By ensuring electrical contact between the metal overlayer and the GaAs substrate, Fermi level equalization across the MOS structure resulting from the differences in work functions occurs. If the Fermi level at the Al_2O_3/GaAs interface is free to move, it would be expected to align with the metal work function resulting in a reduction in band bending (increase in core level binding energy) for the n-type substrate with the low work-function Al contact and an increase in the band-bending (reduction in core level binding energy) for the high work-function Ni contact. The same dependence of core level binding energy on metal work function would be expected for the p-type substrate, however, the magnitude of the shifts would differ, so for an Ni gate a much larger core level binding energy shift should be recorded for n type than for p type, while for an Al gate we would expect a larger shift for p type than for n type.

HAXPES measurements for samples with an Al gate show that the peaks shift 0.11 eV and 0.15 eV to higher BE, for

n- and p-type samples, respectively, with no detectable change for the Ni gate. The limited ability to move the Fermi level of either dopant type suggests high D_{it} at the Al_2O_3/GaAs interface. The small shift in the GaAs core levels following the deposition of the low work-function Al contact indicates that there is a limited ability of the Fermi level to move towards the conduction band. These combined results indicate that the band bending observed at the Al_2O_3/GaAs interface for the n- and p-doped substrates in the absence of a metal contact broadly reflects the position of the partially pinned Fermi level, as no significant Fermi level movements occurred following the deposition of metals with different work functions. The measurements also suggest that the partial Fermi level pinning for n- and p-doped substrates at different positions in the band gap are caused by different interface state defects consistent with previous studies.[9,17,18] This result is in agreement with the recent work of Caymax *et al.*[9] for electrical measurements on sulfur treated Al_2O_3/GaAs MOS capacitors on n- and p-doped substrates which reported different defect state distributions in the GaAs band gap and the limited ability of sulfur treatment to passivate the mid-gap defect states. The reduction in signal to noise apparent in the spectra for the GaAs substrate peaks following the metal deposition reflects an intensity attenuation of 84% in the case of the Al contact and a 91% reduction for the Ni contact which highlights the necessity for the large sampling depth and high brilliance capabilities of HAXPES measurements.

Following the work of Kraut *et al.*,[19] the position of the VBM in relation to a reference metallic Fermi level was determined by theoretically calculating the density of states (DOS) from first principles. The theoretical DOS is then weighted by the cross section of each atomic orbital, and convolved with a Gaussian curve, $\sigma = 0.5$ eV full width at half maximum, in order to accurately model the VB as measured by photoemission.[20] Figure 2 shows the good agreement

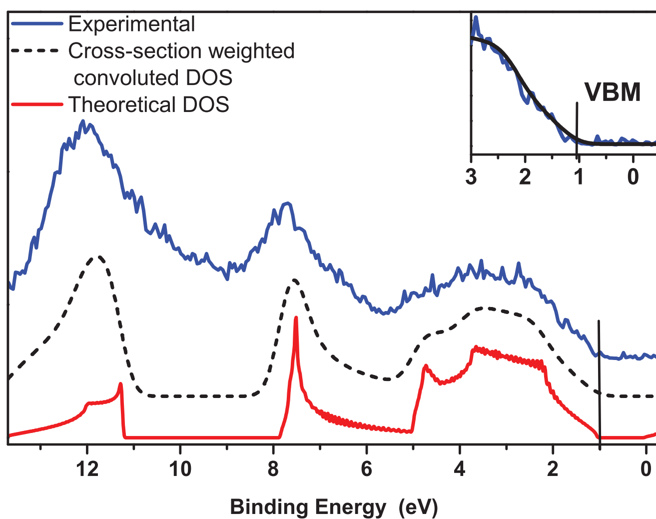

FIG. 2. (Color online) Total theoretical DOS, convolved cross section weighted DOS and experimental photoemission valence band spectra of n-type GaAs/Al_2O_3. A Gaussian of $\sigma = 0.5$ eV was used in convolution. The VBM position is indicated by the vertical line. The Ni Fermi edge was used to determine zero binding energy on this scale which reflects the Fermi level position.

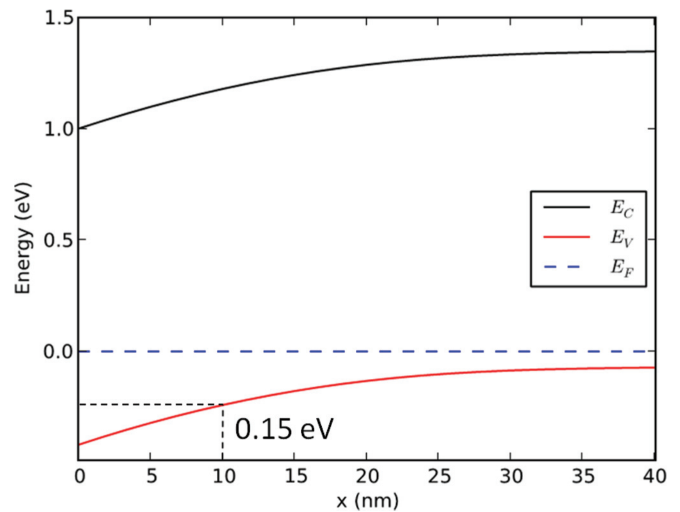

FIG. 3. (Color online) Simulation of the band bending in a p-type GaAs MOS structure based on 0.4-eV band bending as measured by HAXPES.

between the calculated DOS and the VB spectrum for n-type Al_2O_3/GaAs as measured by photoemission. The VBM for this n-doped substrate is determined to be approximately 1.0 ± 0.1 eV below the reference Fermi level, which would be at zero binding energy on the x axis, while the corresponding VBM for the p-type Al_2O_3/GaAs, determined using the same method, was 0.4 ± 0.1 eV below the Fermi level.

In order to assess the magnitude of the error in determining the Fermi level position from the HAXPES measurement, a simulation of the band bending for 5×10^{17} cm^{-3} doped p-type GaAs resulting from a 0.4-eV surface potential was performed by numerically solving Poissons equation. The resulting band-bending diagram shown in Fig. 3 indicates that for a sampling depth into the GaAs substrate of 10 nm, the error in determining the VBM position is a maximum of 0.15 eV. However, due to the exponential fall off in the weighting of the photoemitted electron contribution with depth, it would be reasonable to assume that the actual error is likely to be less than 0.1 eV. This analysis allows the determination of the Fermi level position for the p-type sample without a metal cap, or with an Ni cap, to be in the range of 0.4–0.5 eV above the VBM, while for the sample with the Al cap the Fermi level is 0.55–0.65 eV above the VBM. For the equivalent n-type sample, assuming a similar band-bending derived error, the Fermi level is in the range of 0.9–1.0 eV above the VBM for uncapped and Ni capped samples, and 1.01–1.11 eV for Al capped samples.

In order to quantify any surface photovoltage (SPV) related effect,[21] caused by the generation of electron hole pairs in the GaAs by a high incident photon flux, the following analysis has been undertaken. SPV effects are characterized by a rigid shift of both semiconductor substrate and metal derived peaks towards the flat band positions.[21] This has the effect on p-type substrates of shifting the metallic Fermi edge above the reference Fermi level by an amount equivalent to the band flattening cause by SPV, but no such shift was observed in this work. In addition, the relatively high doping density (5×10^{17} cm^{-3}), and the fact that measurements were

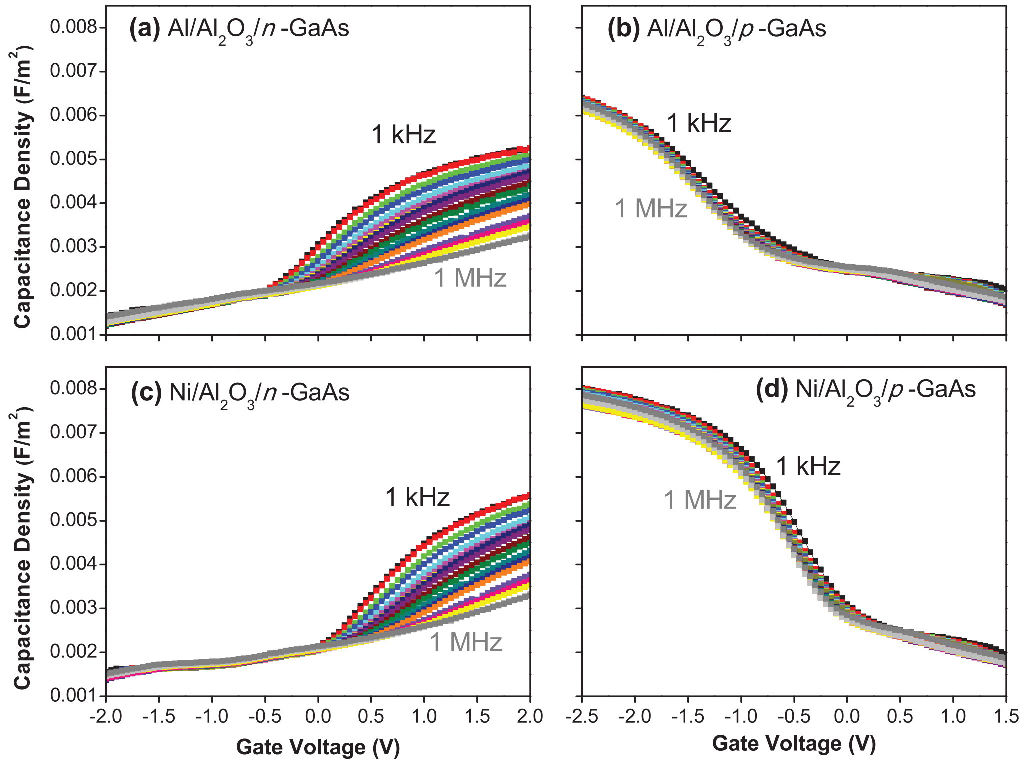

FIG. 4. (Color online) Multifrequency (1 kHz to 1 MHz) C-V response at room temperature (∼295 K) for (a) $Al/Al_2O_3/n$-GaAs, (b) $Al/Al_2O_3/p$-GaAs, (c) $Ni/Al_2O_3/n$-GaAs, and (d) $Ni/Al_2O_3/p$-GaAs MOS capacitors.

performed at room temperature both act to minimize any SPV effect.[22] Deriving similar Fermi level positions from both metal capped and uncapped samples also indicates that a significant SPV effect is not occurring, as the presence of a metal cap should act to reduce the SPV effect.[22] In any case, studies by Bauer *et al.*[22] would indicate that for the photon flux used in these measurements (maximum of 10^{11} photons/s) and the doping density of the GaAs substrates, an upper estimate of the SPV effect would result in no more than a 0.1-eV shift towards the flat band positions. Even taking these SPV-induced shifts into account, and adding this to the error as a result of the band bending, the results suggest that the Fermi level of the *p*-type sample is in the range 0.4–0.6 eV above the valence band maximum (VBM) for uncapped and Ni capped samples, and 0.55–0.75 eV for Al capped samples, above its calculated position of 0.04 eV above VBM. The corresponding analysis for the *n*-type Fermi level position is in the range 0.8–1.0 eV from the VBM for uncapped and Ni capped samples, and 0.91–1.11 eV for Al capped samples, below its calculated position of 1.38 eV above VBM, which agree with the *n*-*p* Fermi level separation of 0.6 eV as determined from the core level peak shifts. These Fermi level positions are in good agreement with those previously reported for *p*-type GaAs, 0.4–0.6 eV,[8] and 0.33 eV[23] above the VBM. However there is a greater discrepancy in the *n*-type Fermi levels, with previous values of 0.61 eV[23] and 0.7 eV.[24] The presence of two pinning positions close to the midgap is, however, consistent with the unified defect model (UDM), which explains the two pinning states as being related to acceptor (missing As atom) or donorlike (missing Ga atom) states which are due to missing atoms at the semiconductor/oxide interface.[9,25]

In order to fully characterize the presence of interface states at the dielectric-semiconductor interface, both high and low ac frequency C-V measurements are required. The C-V responses recorded at a range of ac signal frequency (1 kHz to 1 MHz) for the corresponding Al (160 nm) and Ni/Au (70/90 nm) gate $GaAs/Al_2O_3$ MOS capacitors for the *n*- and *p*-type GaAs are shown in Figs. 4(a)–4(d). A large frequency dispersion at positive gate voltages is observed in the C-V for the *n*-type GaAs, which is consistent with the high interface state density in the upper half of the GaAs band gap. The accumulation capacitance is not seen from the 1-MHz C-V, suggesting that the Fermi level is pinned at a fixed energy level at the Al_2O_3/GaAs interface for *n* type and cannot move towards the conduction band to accumulate electrons. The accumulationlike capacitance measured at 1 kHz is not only due to the differential capacitance (C_s) of the *n*-type GaAs but is a consequence of a capacitance contribution of an interface state capacitance (C_{it}) in parallel with C_s. As C_{it} is large compared to C_s and C_{ox}, according to the equivalent circuit of a MOSCAP with the presence of interface states,[15] a capacitance that approaches C_{ox} can be observed but does not indicate that accumulation is achieved. Because the Fermi level is pinned at the fixed energy level, all the additional gate charge is compensated by charging Al_2O_3/GaAs interface defects. A similar C-V response was also observed for a HfO_2/GaAs MOS capacitor at 295 K.[26] The multifrequency C-V response for the *p*-type GaAs MOS capacitors shows much smaller frequency dispersion at negative gate voltages, with a maximum capacitance that approaches C_{ox} at both 1 kHz and 1 MHz, implying that the interface state density is reduced in the lower half of the GaAs band gap in comparison to the

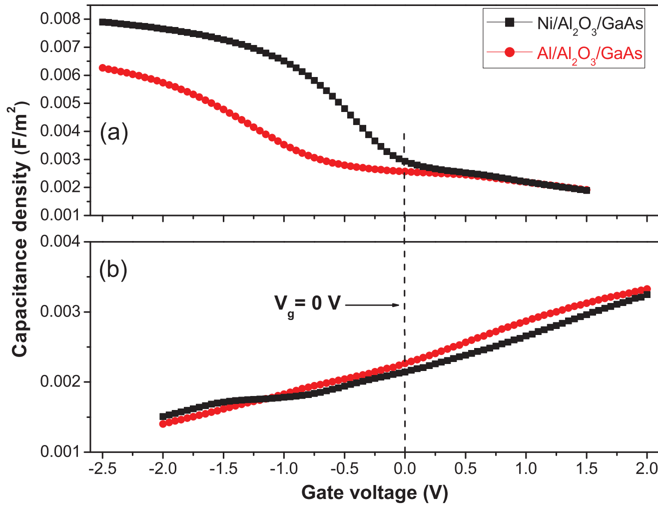

FIG. 5. (Color online) Comparison of 1-MHz C-V between Al and Ni gates for (a) p-GaAs and (b) n-GaAs.

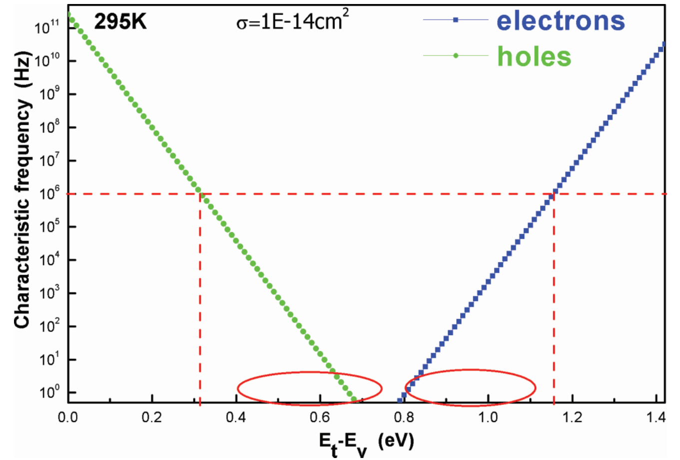

FIG. 6. (Color online) Simulation of trap response using the model by Brammertz *et al.*[6] associated with the measurement at 295 K, assuming a capture cross section of 1×10^{-14} cm^{-2}. The horizontal dashed line corresponds to the high frequency of 1 MHz in the C-V measurement and circled regions represent the energy levels of interface states (E_t) in the GaAs band gap measured by HAXPES, which are in the ranges 0.8–1.11 eV and 0.4–0.75 eV above VBM for the n and p type, respectively, in the absence of metal contacts and approximately the same after the deposition of the Al or Ni gate. For smaller values of capture cross section the region of the energy gap over which the interface states can respond is reduced.

upper half, thus the p type can more easily reach accumulation than the n type.

The work-function difference between Al and Ni on the MOS structures under investigation is estimated from the C-V at 1 MHz as shown in Figs. 5(a) and 5(b) for p- and n-type, respectively. In order to obtain the Fermi level position, the GaAs surface potential is calculated based on the measured capacitance at 1 MHz and zero gate voltage, as the HAXPES measurement is carried out without applying a gate voltage. It is crucial to do the calculation on the premise that a true high frequency capacitance is obtained at $V_g = 0$ V, otherwise the measured capacitance comprises a C_{it} term which leads to an incorrect surface potential. A model by Brammertz *et al.*[6] that determines the interface trap response at 295 K using a capture cross section of 1×10^{-14} cm^2 is shown in Fig. 6. It is evident that only the interface defects in the energy range E_v to $E_v + 0.31$ eV and $E_c - 0.27$ eV to E_c can respond to an ac frequency of 1 MHz. All the interface states outside this energy range will only affect the C-V though a stretch-out along the gate voltage axis without the addition of C_{it} to the total capacitance of the MOS capacitor. As discussed earlier, the HAXPES measurements indicate that the Fermi level is located in the range of 0.8–1.11 eV and 0.4–0.75 eV above the VBM for the n and p types, respectively. It is noted that these energy positions are in the region where interface states cannot respond, giving us confidence in calculating the surface potential using the 1-MHz capacitance at $V_g = 0$ V. In addition, it is worth highlighting that for GaAs, the capture cross section can vary over orders of magnitude.[27] The calculations for the model have been performed for capture cross sections which span 3 orders of magnitude (1×10^{-17} to 1×10^{-14} cm^2), which all show that no interface states at those energy levels can respond to 1 MHz at $V_g = 0$ V. From the C-V at 1 MHz the corresponding semiconductor depletion capacitance can be calculated from the total measured capacitance ($C_{it} = 0$) and an oxide capacitance value $C_{ox} = 9.5 \times 10^{-7}$ F/cm^2 assuming an Al_2O_3 layer with nominal thickness of 8 nm is formed during the ALD. This value can then be used to determine the surface potential and hence the surface Fermi level position with respect to the VBM. The C-V–based calculations indicate that for the n type the Fermi level is 0.86 eV and 0.78 eV above the VBM with Al and Ni gates, respectively, and for the p-type, it is 0.41 eV and 0.30 eV above the VBM with Al and Ni gates, respectively, which are in good agreement with the HAXPES measured Fermi level positions. The comparative HAXPES and C-V results ($V_g = 0$) for the surface Fermi level position are presented in Table I. The difference between the Fermi level position of Al and Ni is thus 0.08 eV over the n type and 0.11 eV over the p type, which is consistent with the Fermi level shift between Al and Ni from HAXPES over both the n

TABLE I. Comparison of Fermi level positions recorded by HAXPES and C-V measurements at $V_g = 0$ V. E_f is the Fermi level energy; E_v is the valence band energy.

Sample	E_f-E_v (Al_2O_3/GaAs)	E_f-E_v (Al/Al_2O_3/GaAs)	E_f-E_v (Ni/Al_2O_3/GaAs)	ΔE_f (Al-Ni shift)
n-type (C-V)	n/a	0.86 eV	0.78 eV	0.08 eV
n-type (HAXPES)	0.8 – 1.0 eV	0.91 – 1.11 eV	0.8 – 1.0 eV	0.11 – 0.31 eV
p-type (C-V)	n/a	0.41 eV	0.3 eV	0.11 eV
p-type (HAXPES)	0.4 – 0.6 eV	0.55 – 0.75 eV	0.4 – 0.6 eV	0.15 – 0.35 eV

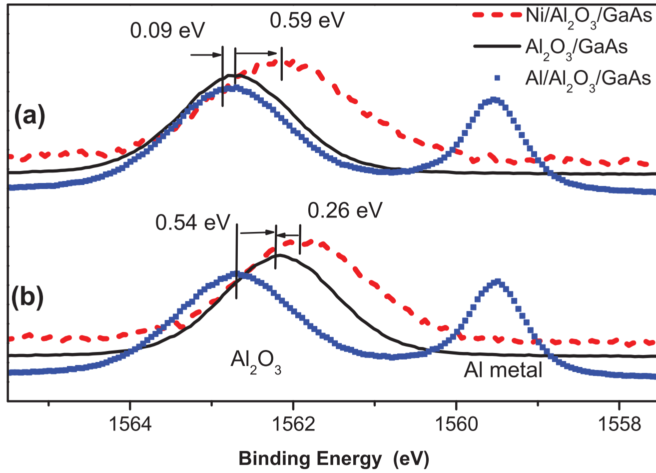

FIG. 7. (Color online) Al 1*s* spectra showing BE shift due to the changes in the potential across the Al_2O_3 layer caused by different work-function metals for (a) *n*-type and (b) *p*-type GaAs. The presence of a metallic Al 1*s* signal at 1559.5 eV binding energy originates from the metal cap.

type, of 0.11–0.31 eV, and *p* type, of 0.15–0.35 eV as shown in Table I.

Work-function differences between the metal and the pinned GaAs Fermi level should be reflected in a potential difference across the dielectric layer resulting in a binding energy shift, and broadening of the associated dielectric core levels.[3] These changes would be expected to be most apparent between the *n*-type GaAs and the Ni, or the *p*-type GaAs and the Al, as these both represent the largest potential difference, given the electron affinity of GaAs is 4.07 eV. Figure 7 shows the changes in binding energy of the Al 1*s* oxide peak (located at 1562 eV) for the *n*- and *p*-type GaAs substrate resulting from metal deposition. For the *n*-type sample the deposition of the low work-function Al results in a small increase in the Al 1*s* peak BE (0.09 eV), which is less than the work-function difference in the range of 0.3–0.5 eV. It is thought that this discrepancy is partly due to trapped charge in the Al_2O_3, which has previously been measured in the case of Al_2O_3/InGaAs systems.[28,29] If there is positive charge already present in the oxide then the potential field needed to equalize the metal work-function and Fermi level in the semiconductor is less in the case of an Al cap, and greater in the case of an Ni cap, which is the case in our results as shown in Table II. The presence of a metallic Al 1*s* signal at 1559.4 eV binding energy originates from the gate metal. For the Ni capped *n*-type sample, a significant decrease in the binding energy (−0.59 eV) of the Al 1*s* oxide peak reflects a potential difference of the opposite polarity across the dielectric caused by the high work-function Ni contact, as previously explained by Walsh *et al.*[5] and this shift agrees well with the theoretical work-function difference in the range from −0.52 to −0.32 eV. The corresponding binding energy shifts for the *p*-type sample were 0.54 eV to higher BE with the Al cap and −0.26 eV for the Ni cap, which agree well with the expected shifts of 0.66–0.86 eV and −0.12 to 0.08 eV, respectively.

TABLE II. Comparison of the calculated and measured shifts in the Al oxide peak due to the presence of a potential field across the oxide layer.

Sample	Calculated Al_2O_3 shift (eV)	Experimental Al_2O_3 shift (eV)
$Al/Al_2O_3/n$-GaAs	0.3 – 0.5	0.09
$Ni/Al_2O_3/n$-GaAs	−0.52 – −0.32	−0.59
$Al/Al_2O_3/p$-GaAs	0.66 – 0.86	0.54
$Ni/Al_2O_3/p$-GaAs	−0.12 – 0.08	−0.26

All of these changes are consistent with the difference in the polarity of the potential difference in the dielectric layer caused by the low and high work-function metals and further reflect the restricted nature of the Fermi level movement in the GaAs, as the work-function difference between GaAs and metal caps is manifest as a potential difference across the dielectric layer.[3] The Al 1*s* peak widths for the metal capped samples broaden when compared to the samples without metal gates reflecting the gradient in the potential across the dielectric layer. The small potential difference of 0.09 eV measured across the Al_2O_3 layer for the Al on *n* type results in negligible broadening while a full width half maximum (FWHM) increase of 0.36 eV for Ni on the *n*-type reflects the larger potential difference across the dielectric. In the case of the *p*-type sample, again negligible differences in FWHM were measured for the Al contact, but a 0.18- eV FWHM increase was found for the Ni capped sample. While these differences are smaller than would be expected, this can be partially accounted for by the limited extent to which these potential changes can be quantified by measuring photoemission peak line shapes.[30]

IV. CONCLUSIONS

In summary, the large sampling depth of HAXPES has been used to characterize band bending in metal/Al_2O_3/GaAs (MOS) structures fabricated with both high (Ni) and low (Al) work-function metals. The results are consistent with different Fermi level positions for *n*- and *p*-doped substrates which are largely independent of metal work function. Valence band measurements indicate that the Fermi level positions in the band gap are in the range of 0.4–0.75 eV and 0.8–1.11 eV above the valence band maximum for *p*-type and *n*-type GaAs, respectively. C-V analysis of near identical samples yield very similar surface Fermi level positions at zero gate voltage for the *n*- and *p*-type GaAs samples. The C-V responses also indicate an Al_2O_3/GaAs interface with a higher D_{it} in the upper half of the band gap. A potential difference across the Al_2O_3 layer consistent with the difference in metal work functions was also measured. The ability of HAXPES measurements to allow the extraction of Fermi level positions at buried metal/dielectric interfaces in the presence of metal capping layers facilitates the study of MOS structures which are difficult to analyze by C-V electrical characterization methods due to the limited Fermi level movement. The fact that HAXPES measurements can also provide information on chemical interactions makes it a powerful analytical tool for the investigation of MOS structures with layer thickness dimensions relevant to future semiconductor device technology nodes.

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