Electron-tunneling operation of single-donor-atom transistors at elevated temperatures

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Individual dopant atoms in silicon devices gain active roles as channel dimensions move into the nanoscale. A single donor can work as an atomic quantum dot, mediating single-electron-tunneling transport from source to drain. However, the tunneling operation of single-donor transistors has so far been reported only at low temperatures below ~15 K, while at high temperatures tunneling features are expected to be smeared out. For a higher-temperature single-electron-tunneling operation, the donor's tunnel barriers must be considerably higher than $k_B T$. Here, we use a special design of a nanoscale Si channel with a central stub region, in which a phosphorus donor's ground state becomes deeper due to the dielectric confinement effect. In these stub-channel devices, electron tunneling via one donor atom survives even at temperatures above 100 K. Results of *ab initio* atomistic simulations provide further insights into the fundamental properties of individual donors in ultrasmall nanopatterned structures.

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In Si nanoscale devices, dopant atoms gain an increasingly active role in the transport characteristics.[1–3] In conventional devices, dopants have played an essential role as free carrier sources because of their shallow energy levels, e.g., 45 meV below the conduction band edge for a phosphorus donor.[4] At low temperatures, beyond this classical function, an individual donor atom effectively works as a unique quantum dot accommodating only one electron.[4] [Although a second electron can also be accommodated (D^- state),[5] its binding energy is too small (1–2 meV) to be observed in transport except at extremely low temperatures, below 1 K.] Recent progress in silicon nanotechnology allowed electrical measurements of electron or hole tunneling through individual dopants in the channel of silicon transistors.[6–13] Results reported so far have been mostly obtained for transistors having channels without any special patterns.[6–8,10–13] In these studies, dopants maintain their shallow ground states and tunneling transport is reported only at low temperatures ($T < 15$ K). For most reports on single-dopant devices, the target application is quantum computing,[2,12] for which low temperatures are suitable because of a longer coherence time. Reports on tunneling operation via dopants at elevated temperatures are lacking, although, for applications toward complementary metal-oxide-semiconductor (CMOS)-based electronics, a higher tunneling-operation temperature is crucial. In order to observe single-electron-tunneling effects, the charging energy must be significantly larger than $k_B T$,[14] which is a first limiting factor for shallow dopants. Furthermore, at high temperatures, thermally activated transport may become quickly dominant. In this article, aiming at high-temperature operation of electron tunneling via a single donor, we study single-donor transistors with specially designed nanochannels in which the tunnel barrier height is enhanced due to dielectric confinement.

For comparative study, we fabricated two types of devices, i.e., without and with a stub structure in the center, as shown in Figs. 1(c) and 1(d). In stub-channel transistors, it is expected that a donor located within the stub region experiences a strong dielectric confinement effect, because it is mostly surrounded by SiO_2, unlike for the case of non-stub field-effect transistors (FETs). This results in deepening of the donor ground state or enhanced barrier height of the donor, which promotes electron-tunneling operation even at elevated temperatures, above 100 K.

We fabricated silicon-on-insulator field-effect transistors (SOI-FETs) having a structure schematically shown in Fig. 1(a). The top Si layer was *n*-type doped by thermal diffusion with phosphorus (P) to a concentration $N_D \cong 1 \times 10^{18}$ cm^{-3}, corresponding to an average distance between neighboring P donor atoms of ~10 nm. Figure 1(b) shows a transmission electron microscope (TEM) image taken across the ultrathin (~2 nm) SOI channel (shown in the zoomed-in image). From an analysis of TEM images for a large number of devices, no significant surface roughness was observed after doping. This was also confirmed by our Kelvin probe force microscope (KFM) observations on samples doped with the same process as the devices shown in this work. While the surface topography was maintained flat, the KFM measurements at low temperature revealed potential fluctuations consistent with the characteristics of individual ionized donors.[9,15,16] The top Si layer is finally surrounded by a thermally grown 14-nm-thick SiO_2 layer, before Al deposition for electrical contacts. Figures 1(c) and 1(d) show scanning electron microscope (SEM) images and a schematic representation of a possible donor distribution for the two types of devices investigated in this work, without and with a stub-shaped channel. The width W for stub channels is the width of the narrow constrictions [Fig. 1(d)], while the width across the stub region is designed to be $2W$. Figure 1(e) shows the electrical characteristics, i.e., drain current (I_D) versus top gate voltage (V_G), for a device with a nominally undoped channel and a device with a phosphorus-doped channel with similar structures. It can be noticed that sharp and irregular Coulomb oscillations can only be observed for the doped-channel device, consistent also with our previous report.[17] This supports the conclusion that single-electron-tunneling is mediated by dopant-induced quantum dots.

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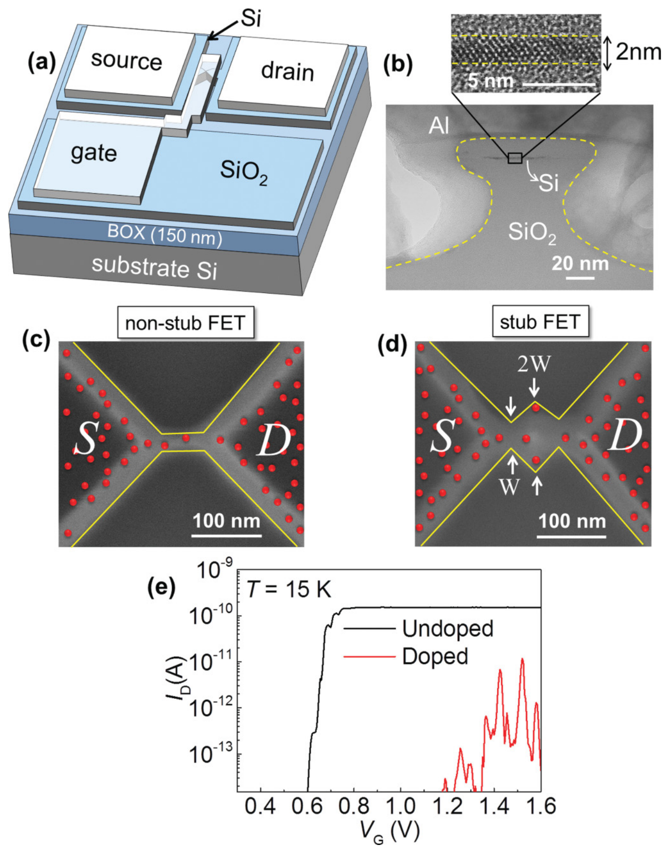

FIG. 1. (Color online) (a) Bird's eye view of the silicon-on-insulator transistor under study. (b) Cross-sectional transmission electron microscope (TEM) image taken across the device channel. Scanning electron microscope (SEM) images before final oxidation for the smallest devices with a (c) non-stub channel and (d) stub channel. The solid lines mark the edges of the channel. P donor atoms within the channel and adjacent source (S) and drain (D) pads are schematically shown as dots. (e) I_D-V_G characteristics measured at low temperature ($T = 15$ K) for a nominally undoped and a phosphorus-doped channel device with similar structures.

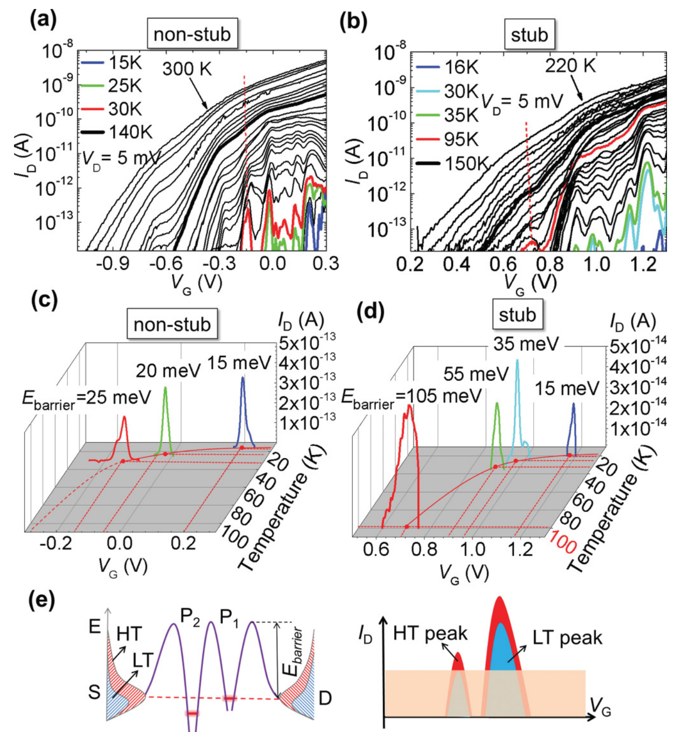

FIG. 2. (Color online) Temperature dependence of I_D-V_G characteristics ($V_D = 5$ mV) for the smallest devices with a (a) non-stub channel (15–300 K) and (b) stub channel (16–220 K). As temperature is increased, new current peaks at negatively larger V_G's become measurable. Emerging current peaks extracted as a function of temperature for transistors with a (c) non-stub channel and (d) stub channel. Each current peak corresponds to tunneling via a different P donor, with estimated barrier heights as indicated in the graph. Most remarkably, for the stub-channel transistor in (d), the last observable current peak (at $V_G \cong 0.7$ V) emerges at $T \cong 100$ K. (e) Schematic illustration of single-electron tunneling via a P donor atom (P_1). The peak due to transport via the deepest-energy P donor (P_2) cannot be detected at low temperatures (LT), but emerges at higher temperatures (HT) due to the broadening of the Fermi-Dirac distribution in the leads, as illustrated in the left panel.

For non-stub- and stub-channel FETs, I_D-V_G characteristics were measured at a small source-drain voltage, $V_D = 5$ mV. The temperature was changed as a parameter, from ~15 to ~300 K. Figures 2(a) and 2(b) show representative sets of I_D-V_G characteristics for the two smallest devices with different channel patterns. At the lowest temperatures (~15 K), the I_D-V_G characteristics exhibit a number of isolated current peaks, as seen in both Figs. 2(a) and 2(b). As argued above, these peaks are due to electron-tunneling transport through donor-induced quantum dots formed in the channel. By raising the temperature in the range of 20–100 K, several new current peaks successively emerge at smaller V_G's for both types of devices.

In Figs. 2(c) and 2(d), for clarity, only the temperature-associated lowest-V_G current peaks are extracted from the full I_D-V_G characteristics and are plotted in the V_G-temperature plane. These peaks successively appear with increasing temperature and are ascribed to tunneling via P donors with deeper ground-state energies. We cannot observe the current peaks of these deep donors at low temperatures (~15 K), since the tunneling rate is too small due to the high potential barriers. (The detectable current level in the present system is around $\sim 1 \times 10^{-14}$ A.) With increasing temperature, however, due to broadening of the Fermi-Dirac electron distribution in the reservoir,[18] as illustrated in Fig. 2(e), the tunneling rate is enhanced and the corresponding current peaks successively emerge, exceeding the detectable current level. It is found that, for the stub-channel FET, the last emerging current peak appears at $T \cong 100$ K [Fig. 2(d)], which is the highest temperature reported so far for single-dopant transistors operating in the single-electron-tunneling (SET) mode. Moreover, the SET feature survives as a prominent hump up to ~150 K, as shown by the thick I_D-V_G curve in Fig. 2(b). At high temperatures, above ~100 K, a number of SET peaks are significantly broadened and overlap each other, indicating a change from the Coulomb blockade mechanism to the resonant tunneling mechanism, primarily due to the reduction of the tunnel resistance.

In Fig. 3(c), we plot only the highest temperatures corresponding to the last emerging current peaks for stub-channel FETs as a function of channel width W. It is found that,

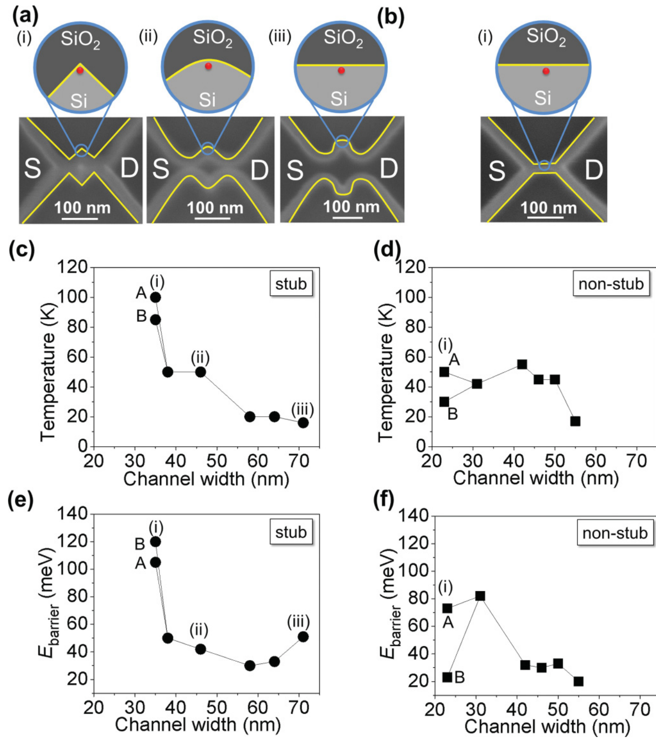

FIG. 3. (Color online) (a), (b) SEM images of device channels with different patterns [insets: sketches of a P donor at the edge of the channel, showing that the shape of the stub area changes from round to pointed hat as the channel width decreases, and the area ratio of SiO_2 to Si increases, as indicated by (iii), (ii), and (i) in (a)]. Temperature of emergence of the final peak for devices with a (c) stub channel and (d) non-stub channel. Each data point corresponds to a different device. Barrier height extracted for the peak corresponding to the lowest-energy P donor as a function of channel width for devices with a (e) stub channel and (f) non-stub channel.

with decreasing W, the highest operation temperature systematically increases. For the narrowest stub-channel devices ($W \cong 30$ nm), it is confirmed by two devices, A and B, that the last peaks emerge at high temperatures of $\sim$100 K. The main reason for this high temperature is an enhanced tunnel barrier height compared to bulk donors, which allows the efficient suppression of thermally activated transport even at such elevated temperatures. According to the dielectric confinement effect, it is most likely that the last emerging peaks correspond to P donors located near the edge of the stub structure, because screening of the donor potential will be diminished by the surrounding SiO_2. As shown in Fig. 3(a) by SEM images and illustrated in the insets as sketches of a P donor's environment, with decreasing W, the shape of the stub region changes from a round to pointed-hat shape, and the area ratio of SiO_2 to Si increases, leading to deeper donor states. For non-stub FETs [shown in Fig. 3(b)], the dependence of operation temperature on channel width has no systematic trend, as seen in Fig. 3(d). The scattering of the data is probably due to dopant position fluctuation with respect to the edge of the channel. For such non-stub FETs, all of the final peaks emerge at temperatures below 60 K.

Tunnel barrier heights ($E_{barrier}$) were extracted from Arrhenius plots of I_D for elevated temperatures ($T > 150$ K).[6] For a V_G value corresponding to a current peak, $E_{barrier}$ represents the energy difference between the donor's ground state and the potential barrier maximum along the source-drain direction, as illustrated in Fig. 2(e) (left panel). In Figs. 2(c) and 2(d), these extracted $E_{barrier}$ values are shown on top of each emerging current peak. Figures 3(e) and 3(f) plot $E_{barrier}$ values for the P donor responsible for the last observable peak, for stub- and non-stub-channel FETs, respectively. For stub FETs, as seen in Fig. 3(e), $E_{barrier}$ systematically depends on channel dimensions, increasing up to values of $\sim$120 meV by decreasing channel width. On the other hand, for non-stub FETs, $E_{barrier}$ does not exhibit a systematic dependence on channel dimensions, as observed from Fig. 3(f). Similarly to Figs. 3(c) and 3(d), this result is also ascribed to a deeper-energy P donor located near the edge of the stub channel, where dielectric confinement should be most prominent.[19–21]

The similarity between the behaviors of T and $E_{barrier}$ seen in Fig. 3 suggests that the tunnel barrier height is indeed the dominant factor for ensuring high-temperature tunneling operation. In Table I, temperatures reported in the literature for single-electron-tunneling operation in single-donor transistors are listed, together with the temperature reported in the present work. In the previous works, the temperature range of interest was below $\sim$15 K, where current peaks due to tunneling via individual donors could be systematically analyzed. In this work, we demonstrate single-electron-tunneling operation at high temperatures, which is important for practical applications.

For one of the narrowest stub-channel FETs, we measured the stability diagrams, i.e., I_D plots in V_D-V_G plane, for 20 K

TABLE I. Temperatures reported so far in the literature for single-electron tunneling in single-donor transistors. Device types and reported channel dimensions are also included for completeness. All previous studies have been carried out at low temperatures ($T < 15$ K). This work addresses a higher-temperature range ($T \cong 100$ K) for devices with a special channel design.

Reference	Device type	L (nm)	W (nm)	t (nm)	Reported temp. (K)
Sellier *et al.* (2006) (Ref. 6)	FinFET	60	385	60	4.2
Lansbergen *et al.* (2008) (Ref. 7)	FinFET	60	385	60	1.6
Pierre *et al.* (2010) (Ref. 8)	SOI-FET	30	50	20	12
Tabe *et al.* (2010) (Ref. 9)	Si FET	100	50	10	15
Tan *et al.* (2010) (Ref. 10)	Si FET	30	50	Bulk	0.1
Prati *et al.* (2011) (Ref. 11)	Si FET	50	116	Bulk	4.2
Fuechsle *et al.* (2012) (Ref. 12)	SOI-FET	20	108	Bulk	0.2
This work	Stub SOI-FET	140	25	2	100

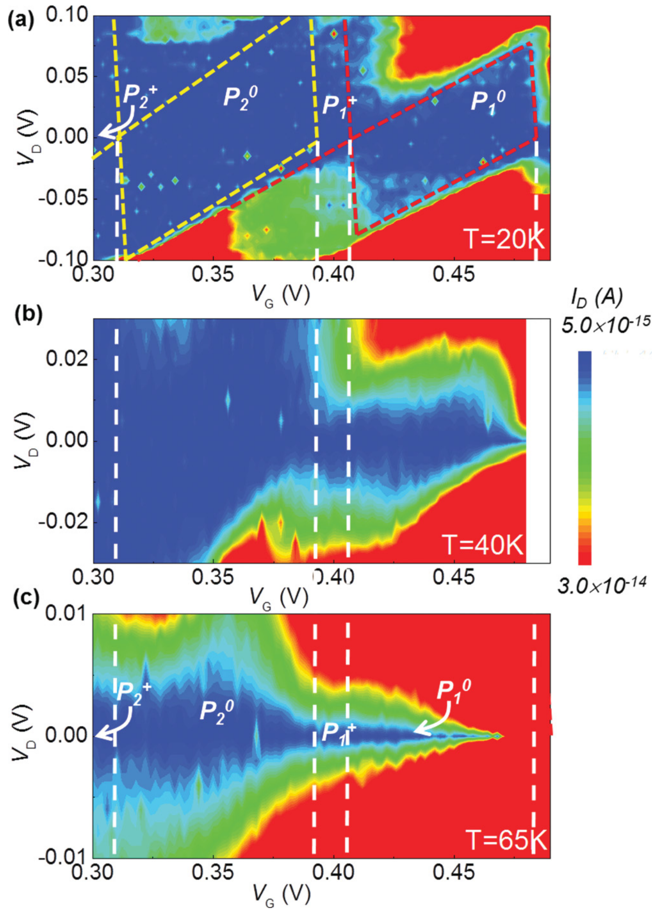

FIG. 4. (Color online) Stability diagrams, i.e., I_D plotted in V_D-V_G space, for one smallest stub-channel FET at different temperatures: (a) Lowest measurement temperature, $T = 20$ K (boundary lines are delineated based on the high-V_D regions and high-temperature data for the stable-charge regions corresponding to two donors: P_2, appearing at more negative V_G's, and P_1, clearly observed even at this low temperature), (b) intermediate temperature, $T = 40$ K, and (c) higher temperature, $T = 65$ K (V_D range is modified for visibility).

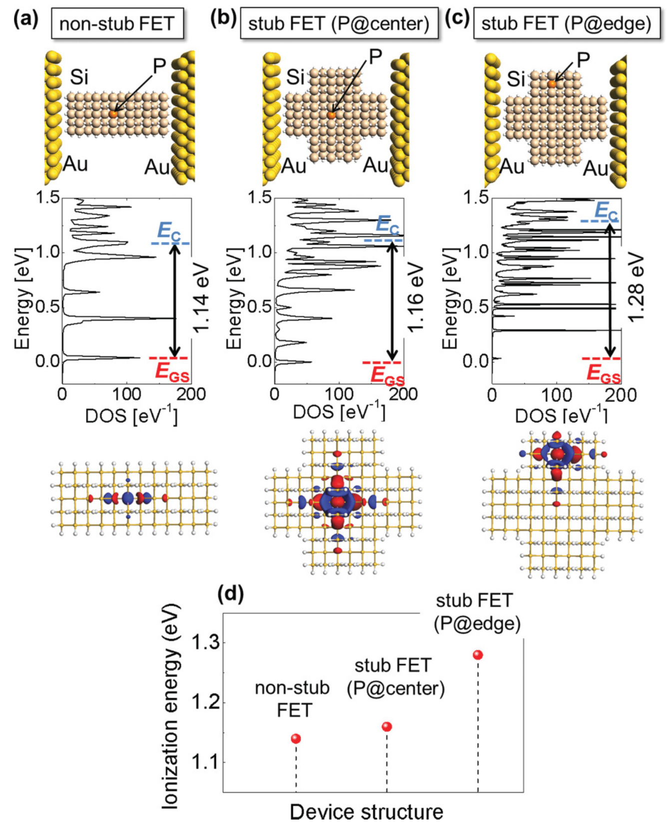

FIG. 5. (Color online) Atomistic *ab initio* simulations of donors in 1-nm-order nanostructures. Atomistic views of device structure (upper panels), density-of-states (DOS) spectra for energies near the conduction band edge (central panels), and electron wave function distribution in the donor's ground state (lower panels) for a (a) non-stub FET with a P donor centered, (b) stub FET with a P donor centered, and (c) stub FET with a P donor within the side region. (d) Ionization energy estimated from the DOS spectra for various device structures.

[Fig. 4(a)], 40 K [Fig. 4(b)], and 65 K [Fig. 4(c)]. At the lowest temperature, $T = 20$ K [Fig. 4(a)], a large no-current open region can be observed for $V_G < 0.42$ V and a closed Coulomb diamond is seen for $V_G \cong 0.42$–0.48 V; basically, these regions correspond to a phosphorus donor's charge states, $P_1{}^+$ and $P_1{}^0$, respectively. However, inside the open no-current region, based on the features seen at high V_D and at higher temperatures [Figs. 4(b) and 4(c)], another set of Coulomb diamonds can be outlined. This corresponds to the charge states of another P donor (P_2) with a deeper ground-state level compared to P_1. The boundaries of these diamonds are difficult to identify at low temperatures because of the current levels below our detection limit in the conduction regions. It can be seen, however, that the charging energy estimated from these diamonds is most likely large (>100 meV), which further justifies the observation of single-electron-tunneling features up to high temperatures. At $T = 40$ K (Fig. 4(b)), the stable-charge regions of P_1 are shrunken and modified, because of remarkable contribution of electrons thermally activated over the barrier. At 65 K [Fig. 4(c)], signatures of Coulomb blockade transport can be observed for the donor P_2 for $V_G \cong 0.32$–0.38 V; however, the shape and boundaries of these regions are distorted and obscured due to thermally activated transport. These regions correspond to the ionized state of the deep-energy donor ($P_2{}^+$) and, respectively, to its neutral (one-electron-captured) state ($P_2{}^0$). The lever-arm factor, $\alpha = C_G/C_\Sigma$, with $C_\Sigma = C_G + C_S + C_D$, evaluated from the low-temperature stability diagram, is about 0.8, which means that the P donor is more strongly coupled to the gate than to the source/drain leads. This is consistent with the model of a donor (P_2) located in the edge stub region, being more strongly wrapped by the SiO_2 layer. At 65 K [Fig. 4(c)], the Coulomb blockade regions for P_1 observed in Figs. 4(a) and 4(b) almost vanish, since thermally activated electrons can easily flow over the barrier.

The above experimental results describe single-electron-tunneling transport via individual P donors at elevated temperatures. The highest tunneling-transport temperature is achieved for the narrowest stub-channel FETs due to high tunnel barriers of donors in such structures. In order to examine the fundamental properties related to the electronic states of donors in nanoscale Si, we performed *ab initio* atomistic simulations for non-stub and stub nanostructures, as shown in the upper panels of Fig. 5. Due to the limitations of the

computational resources, only ∼2-nm-long and ∼1-nm-wide channels were simulated. This size is much smaller than that of the experimental devices, but, nevertheless, these simulations provide important insights for the donor states. The central panels in Fig. 5 show the density-of-states (DOS) spectra, focusing on the energy range close to the conduction band edge ($E > 0$ eV). The lowest DOS peak is ascribed to the ground state (E_{GS}) of the P donor, as confirmed by the *s*-orbital nature of the electron wave function. Higher-energy DOS peaks, with a dispersed distribution, can be ascribed to the excited states of the P donor and to Si-related states. The lower panels show the distribution of the electron wave function at the donor's ground-state energy (E_{GS}). It can be seen that the electron is strongly localized around the donor. The lowest unoccupied Si molecular orbital (LUMO), equivalent to the conduction band edge (E_C) for the Si structure, is identified as the energy level for which the wave function expands over the whole Si structure. The ionization energies (E_I) can be calculated as E_C-E_{GS} and are plotted in Fig. 5(d). For all structures, E_I is around 1 eV, which is more than 20 times larger than for bulk Si (45 meV). For stub-shaped channels, E_I generally increases as the P donor moves from the center towards the edge. The highest ionization energy, $E_I \cong 1.3$ eV, is obtained for the case of a donor located within the stub edge region.

Based on our preliminary estimations and predictions from literature,[19] ionization energy for P donors in such 1-nm-order structures can reach ∼1 eV. This enhancement should be sufficient to ensure tunneling operation even at room temperature. Precise position control of the dopant atoms becomes a key technique for reaching this goal. Single-ion implantation[7,22] is attractive because it makes use of CMOS-compatible technology. Another technique involves atomic manipulation by a scanning tunneling microscope (STM)[23] and has been recently used to fabricate a precisely controlled single-donor transistor.[12] In addition, appropriate engineering of the insulator/gate structure, for instance, by replacing the SiO_2 layer with a low-*k* insulator, could lead to a reduction in the screening effects of the electrodes on the donor potential,[20] which is expected to promote, as well, tunneling operation at higher temperatures.

In conclusion, we found that, in nanopatterned-channel transistors, single-electron tunneling via individual P donors is observed at elevated temperatures, above 100 K. This is due to an increase in the P donor's barrier height, in particular, for a donor located in the pointed-hat stub-channel transistors. For these devices, current peaks emerge at ∼100 K, with signatures of tunneling surviving up to ∼150 K. Atomistic *ab initio* simulations provide further insights into the electronic properties of individual donors in nanostructured channels. These results represent guidelines for the design of single-dopant devices operating at room temperature, paving the way for practical applications based on individual dopant atoms in Si nanodevices.

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[1] A. Asenov, IEEE Trans. Electron Devices **45**, 2505 (1998).
[2] B. E. Kane, Nature (London) **393**, 133 (1998).
[3] T. Shinada, S. Okamoto, T. Kobayashi, and I. Ohdomari, Nature (London) **437**, 1128 (2005).
[4] W. Kohn and J. M. Luttinger, Phys. Rev. **98**, 915 (1955).
[5] M. Taniguchi and S. Narita, Solid State Commun. **20**, 131 (1976).
[6] H. Sellier, G. P. Lansbergen, J. Caro, S. Rogge, N. Collaert, I. Ferain, M. Jurczak, and S. Biesemans, Phys. Rev. Lett. **97**, 206805 (2006).
[7] G. P. Lansbergen, R. Rahman, C. J. Wellard, I. Woo, J. Caro, N. Collaert, S. Biesemans, G. Klimeck, L. C. L. Hollenberg, and S. Rogge, Nat. Phys. **4**, 656 (2008).
[8] M. Pierre, R. Wacquez, X. Jehl, M. Sanquer, M. Vinet, and O. Cueto, Nat. Nanotechnol. **5**, 133 (2010).
[9] M. Tabe, D. Moraru, M. Ligowski, M. Anwar, R. Jablonski, Y. Ono, and T. Mizuno, Phys. Rev. Lett. **105**, 016803 (2010).
[10] K. Y. Tan, K. W. Chan, M. Möttönen, A. Morello, C. Yang, J. van Donkelaar, A. Alves, J.-M. Pirkkalainen, D. N. Jamieson, R. G. Clark, and A. S. Dzurak, Nano Lett. **10**, 11 (2010).
[11] E. Prati, M. Belli, S. Cocco, G. Petretto, and M. Fanciulli, Appl. Phys. Lett. **98**, 053109 (2011).
[12] M. Fuechsle, J. A. Miwa, S. Mahapatra, H. Ryu, S. Lee, O. Warschkow, L. C. L. Hollenberg, G. Klimeck, and M. Y. Simmons, Nat. Nanotechnol. **7**, 242 (2012).
[13] Y. Ono, K. Nishiguchi, A. Fujiwara, H. Yamaguchi, H. Inokawa, and Y. Takahashi, Appl. Phys. Lett. **90**, 102106 (2007).
[14] H. van Houten, C. W. J. Beenakker, and A. A. M. Staring, in *Single Charge Tunneling*, edited by H. Grabert and M. H. Devoret (Plenum, New York, 1991).
[15] M. Ligowski, D. Moraru, M. Anwar, T. Mizuno, R. Jablonski, and M. Tabe, Appl. Phys. Lett. **93**, 142101 (2008).
[16] M. Anwar, R. Nowak, D. Moraru, A. Udhiarto, T. Mizuno, R. Jablonski, and M. Tabe, Appl. Phys. Lett. **99**, 213101 (2011).
[17] D. Moraru, Y. Ono, H. Inokawa, and M. Tabe, Phys. Rev. B **76**, 075332 (2007).
[18] N. Y. Morgan, D. Abusch-Magder, M. A. Kastner, Y. Takahashi, H. Tamura, and K. Murase, J. Appl. Phys. **89**, 410 (2001).
[19] M. Diarra, Y.-M. Niquet, C. Delerue, and G. Allan, Phys. Rev. B **75**, 045301 (2007).
[20] M. Diarra, C. Delerue, Y. M. Niquet, and G. Allan, J. Appl. Phys. **103**, 073703 (2008).
[21] M. T. Björk, H. Schmid, J. Knoch, H. Riel, and W. Riess, Nat. Nanotechnol. **4**, 103 (2009).
[22] D. N. Jamieson, C. Yang, T. Hopf, S. M. Hearne, C. I. Pakes, S. Prawer, M. Mitic, E. Gauja, S. E. Anderssen, F. E. Hudson, A. S. Dzurak, and R. G. Clark, Appl. Phys. Lett. **86**, 202101 (2005).
[23] S. R. Schofield, N. J. Curson, M. Y. Simmons, F. J. Ruess, T. Hallam, L. Oberbeck, and R. G. Clark, Phys. Rev. Lett. **91**, 136104 (2003).