Superconducting Ga-overdoped Ge layers capped with SiO_2: Structural and transport investigations

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Superconducting Ga-rich layers in Ge are fabricated by Ga implantation through a thin SiO_2 cover layer. After annealing in a certain temperature window, Ga accumulation at the SiO_2/Ge interface is observed. However, no Ga-containing crystalline phases are identified. Thus it is suggested that the volatile Ga is stabilized in an amorphous mixture of all elements available at the interface. Electrical transport measurements reveal *p*-type metallic conductivity and superconducting transition. The superconducting properties of the samples with high Ga concentration at the interface change dramatically with etching the amorphous surface layer. A critical temperature of 6 K is measured before, whereas after etching it drops below 1 K. Therefore, one can conclude that the superconducting transport is based on two different layers: a Ga-rich amorphous phase at the interface and a heavily Ga-doped Ge layer. Finally, the comparison of the transport properties of Ga-rich Ge with those of Si demonstrates distinct differences between the interface layers and even the deeper-lying doped regions.

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I. INTRODUCTION

It has been one century ago that scientists observed the superconducting state of matter for the first time. Intensive research was performed to understand the fundamentals of this effect and to evaluate its potential for applications. Surprisingly, during the last decade heavily *p*-type doped elemental group-IV semiconductors like diamond,[1] silicon,[2] and germanium[3] turned out to line up in the list of superconducting materials. To observe superconductivity in these elemental semiconductors at ambient pressure, acceptor concentrations well above the metal-insulator transition (MIT) are necessary. Superconducting diamond with boron concentrations in the range of a few atomic percent and a critical temperature of about 4 K was first prepared by high-pressure high-temperature synthesis.[1] This process was soon replaced by chemical vapor deposition that allows for better control of the acceptor incorporation and crystal quality that enabled critical temperatures as high as 7 K.[4] Bustarret *et al.*[2] demonstrated that even the base material of today's semiconductor technology, silicon, could become superconducting when heavily doped with boron. Gas immersion laser doping (GILD) was applied to prepare superconducting layers with critical temperatures below 0.6 K. However, their attempt to fabricate superconducting Ge in the same way failed.[5] The most probable reason is that the boron acceptor is not well adapted to the germanium lattice and, therefore, most of the boron atoms remain electrically inactive in the case of supersaturation. Gallium is a more promising acceptor than boron and allows for higher doping levels in Ge.[6] Recently, superconductivity has been proven in Ga-doped Ge with critical temperatures between 0.3 and 1 K. These layers were produced by processing steps compatible to microelectronic technology, namely, ion implantation and short time annealing.[3,7,8]

In all cases mentioned above, the acceptor concentration exceeds the equilibrium solid solubility by far. Therefore the key question is whether dopant precipitation or segregation at grain boundaries[9,10] takes place during sample processing and how such effects influence the low-temperature transport properties. For instance, if the doping element or related phases are superconductors, the question arises as to whether the superconductivity originates from doping or cluster formation.[11] Therefore, the structural investigations focus on the presence of Ga clusters in the Ge matrix.[12] Even as it is challenging to detect Ga in Ge, because of similar atomic masses and spectroscopic properties, clusters with a size greater than 3 nm can clearly be excluded by cross-sectional transmission electron microscopy (XTEM) investigation. Nevertheless, it is reasonable to compare electrical properties of Ga-doped Ge with superconducting Ga layers embedded in a Si matrix. Therefore we used commercial Si wafers covered by 30 nm SiO_2. A superconducting Ga-rich layer at the SiO_2/Si interface was formed via high-fluence Ga ion implantation and subsequent rapid thermal annealing.[13,14] In contrast to Ga-doped Ge with critical temperatures below 1 K, the superconducting properties of these buried Ga-rich layers are comparable to amorphous Ga films with a critical temperature of about 7 K.[11,15–17] On one hand, this is a strong indication that the observed superconductivity in Ga-doped Ge is a real doping effect. On the other hand, the question arises as to whether it is also possible to create buried Ga-rich layers in Ge with critical temperatures in the range of 7 K. Then it is possible to study the behavior of Ga-rich phases in a Ge matrix, which is the next indispensable step for interpreting the superconductivity in Ga-doped Ge.[3,7,8,12–14]

In the present paper we investigate the feasibility of embedding superconducting layers with adjustable critical

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temperatures in Ge covered with SiO_2 within one implantation and annealing step. The role of the SiO_2/Ge interface for the electronic transport is of outstanding interest. It is inevitable because of the severe surface damage caused by ion implantation at room temperature into the bare surface.[18–23] Additionally, the SiO_2 prevents Ga outdiffusion during annealing and facilitates Ga accumulation. The stability and modification of the SiO_2 cover layer during processing is examined. We study in detail the Ga redistribution and the microstructure of the implanted layer system in dependence on the Ga fluence and annealing temperature. The effect of recoil atoms (Si, O, Ge) is considered, too. However, it is the main goal to check whether a superconducting Ga-rich interface layer with high critical temperature can be fabricated in Ge, as already demonstrated in Si.[13,14] Therefore, electrical transport measurements have been performed on samples before and after etching the SiO_2 cover layer. These results are correlated with microstructural investigations.

II. EXPERIMENTAL

Czochralski-grown, (100)-oriented Ge wafers from UMICORE were used as substrate. As Ga is an acceptor for Ge, the wafers are n-type (Sb-doped, $\rho > 10\ \Omega$ cm) in order to isolate the processed layer from the substrate by a pn junction. To protect the surface during implantation and subsequent annealing, a SiO_2 cover layer is sputter deposited on top. This cover layer causes the additional effect of recoil implantation of Si and O into the Ge layer during implantation.[24] To minimize this effect, we used 13- and 30-nm thin SiO_2 layers. Wafer heating above 100 °C was prevented by limiting the ion-beam current density to 0.5 $\mu A/cm^2$. After implantation of 2×10^{16} and 4×10^{16} cm^{-2} Ga with 100 keV, the surface structure was investigated by scanning electron microscopy (SEM) and atomic force microscopy (AFM). The final Ga depth distribution after implantation as well as the ion-mixing tails of recoiled atoms can be predicted by the dynamic simulation code TRIDYN.[25] As an example, the calculated atomic depth profiles for implantation of 4×10^{16} Ga cm^{-2} in Ge with 30 nm SiO_2 on top are shown in Fig. 1. The predicted maximum Ga concentration is about 8 and 13 at. % for fluences of 2×10^{16} and 4×10^{16} cm^{-2}, respectively.

For the following processing steps and investigations, the wafers were cut into pieces of 1×1 cm^2 size. Rapid thermal annealing[26] (RTA) in flowing Ar atmosphere was used to recrystallize the amorphous implanted layer and to activate the Ga acceptors. During annealing, Ga is incorporated into the lattice to create a highly doped layer and also Ga redistribution toward the SiO_2/Ge interface is expected. Former experiments have shown that RTA for 60 s at temperatures between 830 °C and 910 °C leads to the formation of highly doped layers with an onset of superconductivity at temperatures up to 1.4 K.[7]

A rough estimation of the Ga redistribution can be done using the results of Södervall et al..[27] They determined the diffusion coefficient D as a function of temperature as

$$D = 0.014 \cdot \exp\left(-3.3\ \mathrm{eV}/_{k_B T}\right) \frac{\mathrm{m}^2}{\mathrm{s}}, \tag{1}$$

where k_B represents the Boltzmann constant and T the temperature. For RTA, a diffusion length of 26 nm (830 °C) to 86 nm (910 °C) is calculated. This limited diffusion renders the possibility for Ga enrichment at the SiO_2/Ge interface without dramatic profile broadening that would hamper a high doping level in the implanted Ge.

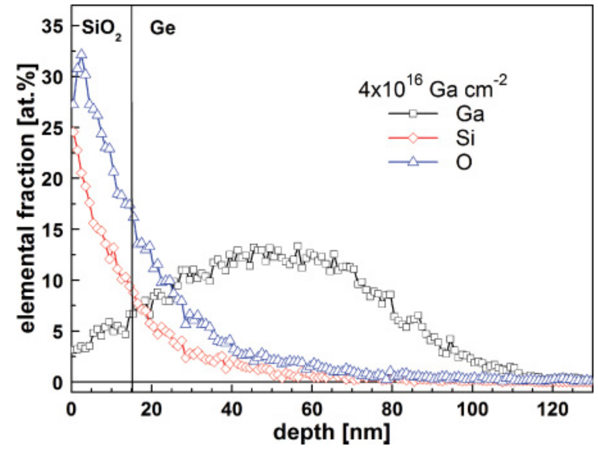

FIG. 1. (Color online) TRIDYN simulation of the elemental depth profiles after implantation of 100 keV, 4×10^{16} cm^{-2} Ga in Ge covered with 30 nm SiO_2. About 14 nm of this cover layer is removed due to sputtering. The SiO_2/Ge interface after implantation is indicated by a vertical line. Long-ranging tails of recoil atoms are formed.

The recrystallization behavior of the implanted layers was analyzed by Rutherford backscattering spectrometry (RBS/C) in random and channeling geometry with a 1.2 or 1.7 MeV He^+ beam. The lower He^+ beam energy enables a high depth resolution in the near-surface region, whereas the higher one allows characterizing thicker layers. In order to study the morphology and microstructure in more detail, high-resolution XTEM with an image-corrected FEI Titan 80-300 electron microscope was used. More information about the local composition was attained by energy-dispersive x-ray diffraction (EDX).

The depth distribution of the different elements in the SiO_2 capping layer and in the Ge substrate was studied by time-of-flight secondary ion mass spectrometry (ToF-SIMS). This tool has been demonstrated to be sensitive to the peculiar chemical arrangement of the elements under analysis providing important information about phase separation and cluster formation upon thermal treatment in the case of Si ions implanted in SiO_2.[28,29] In this work ToF-SIMS analysis was accomplished by means of an IONTOF IV instrument operating in positive or in negative mode to enhance the detection limits of the different elemental species. Sputtering was performed by rastering Ar^+ or Cs^+ ions at 1 keV over a 200×200 μm^2 area. Ga^+ ions at 25 keV were used for analysis by rastering the ion beam over a 50×50 μm^2 area. SIMS analyses feature a high sensitivity for low atomic concentrations and a dynamic detection range of several orders of magnitude. However, it is not a standard-free method, and due to matrix effects it requires a thorough interpretation when analyzing surfaces and interfaces.[30] This is the reason for supplementary Auger electron spectroscopy (AES) measurements. AES does not face the latter difficulties at interfaces, which is essential for our investigations.

Sheet resistance and Hall measurements in Van der Pauw geometry were performed with a commercial Hall-effect measurement system HMS 9709A from LakeShore. It allows for measurements at temperatures from 2 to 400 K. The excitation current and magnetic field are set to be 1 mA and 1 T, respectively. This setup was also used to characterize the magnetic field dependence of the superconducting state. In this case the current was reduced to 100 μA. To contact the sample to the setup, silver wires were pasted with silver glue on top. Additionally, linear four-point probe resistance measurements were performed at temperatures down to 150 mK. For this purpose the samples were mounted in a self-built adiabatic demagnetization cooler which was installed into a commercial 14 T-magnet/^{4}He-cryo system (PPMS, Quantum Design). To prevent heating of the sample and because of the rather low superconducting critical current density, a measurement current of 1–10 μA was used.

Former investigations on Ga-implanted Si have shown that a superconducting Ga-rich interface layer can be removed by etching the SiO_2 cover layer.[13,14] Thus, in the present investigations the electrical properties were characterized before and after etching the sample surface with diluted HF.

III. RESULTS AND DISCUSSION

A. Microstructure

1. *Surface degradation during implantation*

For the 13-nm SiO_2 cover layer a strong surface degradation is observed after implantation of 2 × 10^{16} cm^{-2} Ga, as shown in Fig. 2. There are circular, dendritelike structures randomly distributed on the sample surface. Each structure has a diameter of about 500 nm. Information on the topography of the structures is provided by contact-mode AFM. It turned out that SiO_2 breaks up and the underlying Ge rises up to the surface, creating in this way up to 30-nm-high cylinders. To understand this surface degeneration, one has to keep in mind that physical sputtering of the SiO_2 layer takes place and the underlying Ge lattice is heavily damaged during implantation. According to the TRIDYN simulation, about 7 nm of the originally 13-nm-thick SiO_2 layer are removed after implanting 2 × 10^{16} cm^{-2} Ga. Additionally, this fluence exceeds the threshold for amorphization[31] (1 × 10^{14} cm^{-2}) by far and can lead to void formation.[18–23] As the underlying Ge is intensively swelling due to implantation damage, the eroded SiO_2 cannot withstand the pressure anymore and breaks.[23,32] Using a thicker SiO_2 cover (30 nm), the sample surface remains smooth even after implantation of 4 × 10^{16} cm^{-2} Ga. As demonstrated by XTEM, the SiO_2 cover layer appears coherent and has a sharp interface. Its width is reduced by sputtering to about 18 nm. Thus, for further experiments we used 30-nm layers on top of the Ge wafers to protect them during implantation.

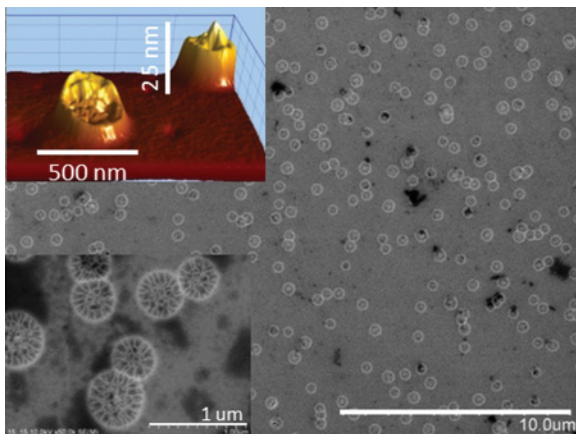

FIG. 2. (Color online) Surface structure investigated with SEM after implantation of (100) Ge covered with 13 nm SiO_2 with a Ga fluence of 2 × 10^{16} cm^{-2}. Randomly distributed, dendritelike structures having a diameter of about 500 nm occur on the surface. The upper inset shows the topography obtained by a detailed AFM measurement.

2. *Layer morphology*

Amorphous Ge recrystallizes at temperatures above 300 °C.[33] The evolution of the recrystallization with increasing annealing temperature was investigated by RBS/C and XTEM. The RBS results of some representative samples after etching the surface layer are shown in Fig. 3. The as-implanted channeling spectrum indicates a 100-nm broad, damaged layer after implantation with 2 × 10^{16} cm^{-2} Ga [Fig. 3(a)]. This thickness increases to 120 nm for 4 × 10^{16} cm^{-2} [Fig. 3(b)]. The channeling yield hits the random level, indicating that these layers are amorphous. The annealing behavior of the implanted layers clearly depends on the Ga fluence. For 2 × 10^{16} cm^{-2} Ga [Fig. 3(a)] and annealing at 850 °C the channeling spectrum decreases to the level of a single-crystalline sample (not shown here). This result confirms those of former investigations.[12] Obviously, recrystallization via solid phase epitaxy (SPE) occurred.[34] Upon closer inspection of the spectra, one can find two additional peaks for the samples annealed at 890 °C and 910 °C, indicating the presence of Si and O even after surface etching. As a consequence, the Ge edge is slightly shifted from channel 520 to 510, which is reasonable if the detected Si and O atoms are localized on the sample surface, indicating an incomplete oxide etching.

Figure 3(b) demonstrates the annealing behavior of samples implanted with 4 × 10^{16} cm^{-2} Ga. Solid phase epitaxial regrowth again seems the main mechanism for lattice reconstruction, but in contrast to the lower Ga fluence, residual damage remains after annealing at temperatures up to 870 °C. With further increase of the annealing temperature, these defects are also removed. Ga concentration and redistribution seem to be the key parameters of the recrystallization behavior. A high Ga concentration could disturb the epitaxial lattice reconstruction during SPE due to the formation of nucleation seeds in the amorphous layer. This is a well-known effect for dopants with a low melting temperature.[34] An increasing annealing temperature causes a decreasing Ga concentration (see below), i.e., an undisturbed epitaxial recrystallization.

More detailed information about the layer microstructure is provided by XTEM. The most important results of the samples implanted with 4 × 10^{16} cm^{-2} Ga before etching the surface are shown in Fig. 4. After annealing at a temperature of 830 °C, the Ge layer consists of a mixture of crystalline grains with different orientations [Fig. 4(a)]. These grains have a

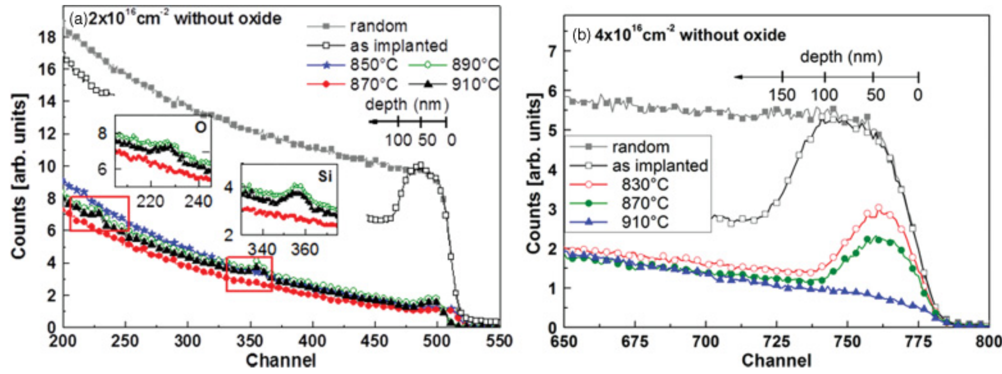

FIG. 3. (Color online) Results of the RBS/C analyses of samples implanted with a Ga fluence of (a) 2×10^{16} cm^{-2} (1.2 MeV He^+) and (b) 4×10^{16} cm^{-2} (1.7 MeV He^+) with depth scale for the implanted Ge layer. After implantation the layers are amorphous. Rapid thermal annealing leads to a single-crystalline layer structure. The inset shows the signal of some residual Si and O that is detected even after surface etching.

typical dimension of 50–100 nm depth, corresponding to the implanted layer thickness and lateral dimension of several tens to more than 100 nm. Some of the grains have the same orientation as the underlying substrate, indicating undisturbed SPE. According to literature[35] and the models for SPE presented therein, misoriented crystallites are mainly expected to be distorted by 54.7° from (100) because of a preferred growth in (111) orientation.[36] In fact, we could identify grains with such orientation. The XTEM investigations presented in Fig. 4(e) confirm complete epitaxial regrowth of the layer annealed at 890 °C. Figure 4(b) shows one grain boundary and the SiO_2/Ge interface in higher magnification. One would expect Ga precipitation, especially at grain boundaries and interfaces. However, as a main result, the analysis of these regions indicates a homogeneous crystal structure and no secondary phases or grain boundary covering.

The overview of Fig. 4(a) and detailed view in Fig. 4(b) indicate a linear chain of dark-appearing precipitates within the SiO_2 cover layer. High-resolution XTEM [Fig. 4(c)] reveals the crystalline structure of these spherical precipitates with a typical diameter of 4 nm embedded in the amorphous SiO_2. They are identified to be pure Ge clusters by measuring the lattice parameter. These clusters form because first, the SiO_2/Ge interface gets blurred due to ion-beam mixing (Fig. 1) and second, during annealing spinodal decomposition into SiO_2 and Ge takes place. A detailed description and model was developed by L. Röntzsch *et al.*.[37]

Upon closer review of the overview in picture Fig. 4(a), randomly distributed amorphous precipitates appear as bright spots in the implanted layer. They have a typical diameter of 3–15 nm [Fig. 4(d)] and mainly consist of O and Si from the mixing tails as measured by EDX. For 830 °C the precipitates were found at grain boundaries and noticeably, at 890 °C all precipitates are located in a depth of around 60–80 nm, which corresponds to the depth of the maximum energy deposited during Ga implantation. Therefore, oxygen accumulates at the grain boundaries because of the high defect density, as it is already predicted in Si.[38–40] Indeed, Scapellato *et al.*[41] observed GeO nanoclusters in O-implanted Ge in the depth with the highest energy deposition and therefore highest

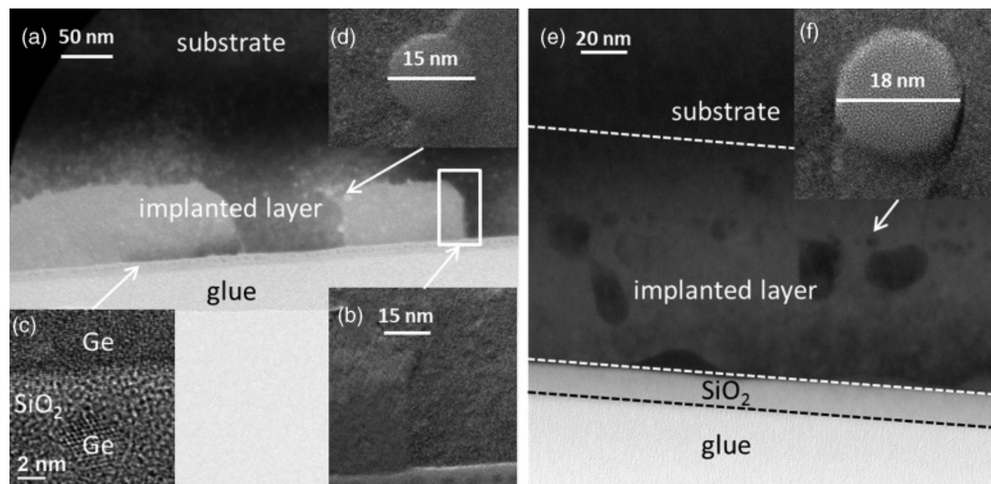

FIG. 4. High-resolution TEM images of samples implanted with 4×10^{16} cm^{-2} and RTA processed at (a) 830 °C as well as (e) 890 °C before etching the SiO_2 cover layer. (b) Homogeneous structure at the grain boundaries. (c) Crystalline Ge nanoclusters located in the SiO_2. (d) Amorphous precipitates located at grain boundaries contain mainly SiO_2. (f) The amorphous SiO_2 clusters are also present after RTA at 890 °C.

vacancy concentration. In our layers Si is also present, and the formation of $SiO_{x<2}$ clusters during annealing is chemically preferred against GeO due to the higher bond energy.[42]

3. Ga redistribution

Due to the high Ga concentrations well above the solid solubility limit, a strong redistribution during thermal processing is expected.[12] The SIMS data of samples implanted with 4×10^{16} cm^{-2} confirm Ga diffusion and loss. Comparing the results before and after annealing, the Ga concentration in the implanted layer decreases by 77% (not shown). Taking the calculated peak concentration of 13 at. % in the as-implanted state as reference, the signal corresponds to a remaining Ga concentration of 3 at. %. However, even this reduced concentration is well above the solid solubility limit of 1 at. % [Ref. 6], and therefore it could be assumed that the outweighing fraction of Ga is not incorporated into the lattice. With increasing annealing temperature the Ga concentration decreases further.

The ToF-SIMS spectra of unetched samples implanted with 4×10^{16} cm^{-2} Ga, shown in Fig. 5(a), indicate a pileup of Ga at the SiO_2/Ge interface. However, one has to be careful when interpreting SIMS signals at surfaces and interfaces because of the well-known matrix effects[30] that can change the SIMS signal by orders of magnitude, as illustrated, e.g., by the comparison of the Ge signals at the interface and in the bulk (not shown). An authentic signal in the Ge substrate is obtained at a depth of more than 15 nm.

After annealing the Ga concentration appears to be almost constant in the region from 20 to 70 nm below the SiO_2/Ge interface. The increasing annealing temperature causes increasing diffusion into the bulk. Of course, the diffusion coefficient given in the experimental part cannot explain the observed profiles. Obviously, it must be much higher than given above. Transient enhanced diffusion in amorphous Ge and charged defects in heavily doped Ge can facilitate the Ga redistribution.[43,44] Depending on the segregation coefficient also, the so-called snowplow effect should lead to an enhanced redistribution during SPE.[34] Furthermore, the SiO_2/Ge interface is an effective sink for Ga due to the affinity of Ga to react with O to form GaO, causing in this way an increasing diffusion.[45]

To get information on the real Ga concentration at the SiO_2/Ge interface, additional AES measurements shown in the inset of Fig. 5(a) were performed. It turned out that the Ga concentration at the interface after RTA at 870 °C is in the range of 60 at. %. Thus the Ga that is lost at a greater depth of the implanted layer accumulates at the interface. Ga accumulation is possible because its loss is hampered by the low diffusivity of Ga in SiO_2. Diffusion lengths at 830 °C and 910 °C can be extrapolated from high-temperature studies[46] to be 8 and 34 nm, respectively. This indicates a significant temperature dependence of the diffusivity. Obviously, the Ga concentration at the interface decreases to 7 at. % after annealing at 910 °C. Thus the Ga redistribution is a two-step process. First, the Ga accumulates at the interface and then depending on the annealing temperature, a certain amount diffuses through the cover layer.[45]

ToF-SIMS is a useful technique that can help to detect small clusters hidden in a matrix. The assumption is that the presence of clusters in the matrix causes an increasing signal of dimers, trimers, or other molecule ions in the sputtered material. Some results are shown in Fig. 5(b). For example, the Ge_2 and SiO_3 signals of the measured samples are shown. The Ge clusters in the SiO_2 cover layer are clearly mapped by the peak in the Ge_2 signal. In the substrate the amount of the sputtered Ge_2, of course, becomes constant. With TEM a localization of $SiO_{x<2}$ at a more defined depth was observed with increasing annealing temperature. This trend is also reproduced by the ToF-SIMS results in a sharpening of the SiO_3 profile. Probably, due to the weak tendency of Ga to form agglomerates, no Ga_2 signal was detected at all.[42] Thus the direct proof of tiny metallic Ga precipitates or films (<3 nm) seems to be extremely difficult.

The results of our microstructural investigations on the annealed samples can be summarized as follows. The implanted Ge layers are single crystalline with some spherical, amorphous SiO_x inclusions. Despite strong mixing effects, a sharp SiO_2/Ge interface is present after annealing. No secondary Ga-containing phases were found by XTEM and EDX analysis, neither in the implanted Ge layer nor at the SiO_2/Ge interface. This is strange, because depending on the annealing temperature, a strong Ga accumulation at the SiO_2/Ge interface occurs as indicated by AES measurements.

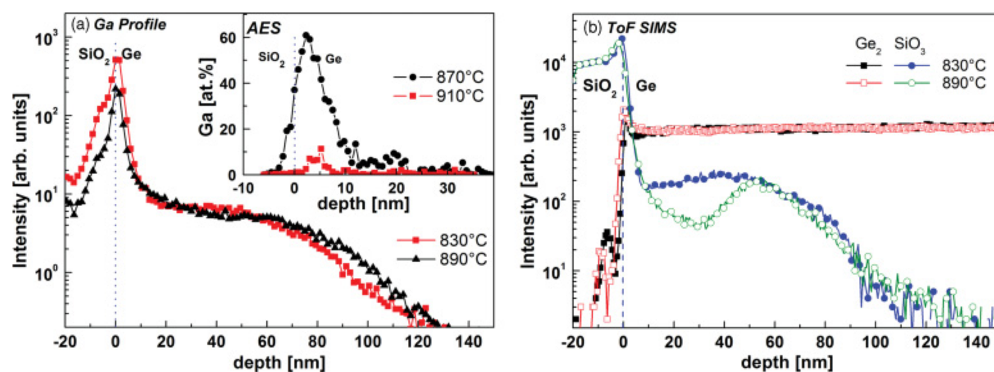

FIG. 5. (Color online) ToF-SIMS profiles of different elements for the samples implanted with 4×10^{16} cm^{-2} Ga. (a) Ga profiles with SiO_2 obtained by ToF-SIMS. To evaluate the Ga concentration at the SiO_2/Ge interface, additional AES measurements are shown in the inset. (b) Ge_2 and SiO_3 signal of the samples investigated by ToF-SIMS.

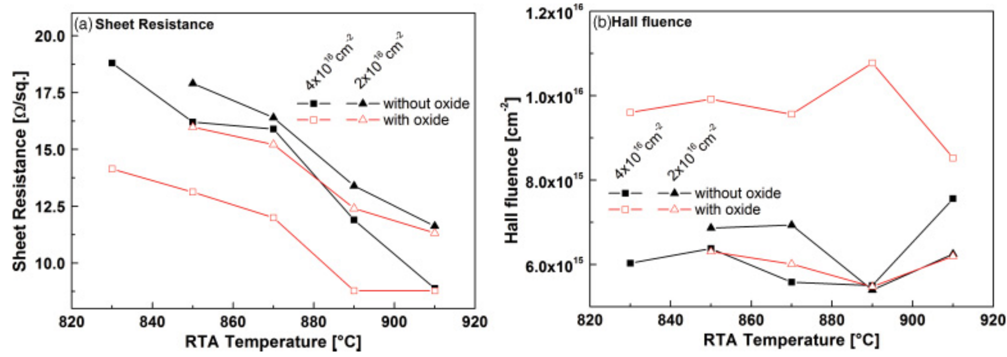

FIG. 6. (Color online) (a) Sheet resistance and (b) Hall fluence at a temperature of 10 K versus annealing temperature before and after surface etching for both implanted Ga fluences.

So one would expect the formation of a Ge:Ga-containing alloy or even pure Ga as a continuous layer or, at least, network of precipitates at the interface. If such a layer is very thin (<3 nm) and amorphous it is hardly detectable by XTEM and even EDX, because Ge and Ga have similar masses and electronic states. Additional AES measurements on samples without SiO_2 (not shown) indicate that the Ga-rich interface layer is removed during etching, as it was also observed for Si.[13,14]

B. Electrical transport in the normal conducting state

For electrical characterization, temperature-dependent resistance and Hall-effect measurements are performed. When interpreting the measured transport data, one has to consider that the prepared layers are on a conductive substrate. Unfortunately, the *pn* junction is not able to completely insulate the *p*-type Ga-doped layer from the *n*-type substrate, resulting in leakage currents through the substrate.[12] However, at low temperatures the low-doped substrate becomes insulating and the transport measurements only probe the Ga-implanted layer. Indeed, below 50 K the sheet resistance and "Hall fluence" is temperature independent. The latter represents the sheet carrier concentration and is determined as $1/(R_H q)$, with R_H the sheet Hall coefficient and q the elementary charge. Reference values for the normal conducting state, obtained at 10 K before and after surface etching, are shown in Figs. 6(a) and 6(b).

For both implanted Ga fluences the sheet resistance continuously decreases with increasing annealing temperature. Corresponding measurements of the Hall fluence [Fig. 6(b)] indicate no significant increase of the charge-carrier density with annealing temperature. Therefore the decreasing resistance can be attributed to less scattering of the charge carriers at lattice defects, i.e., to an increasing mobility. A high residual damage clearly reduces the mobility to 48 cm^2/Vs (4×10^{16} cm^{-2}, 850 °C). For 910 °C the carrier mobility increases to 83–86 cm^2/Vs, independent of the implanted Ga fluence.

Before etching the surface layer of the samples implanted with 4×10^{16} cm^{-2} (2×10^{16} cm^{-2}) Ga, the Hall fluence is $\sim 1 \times 10^{16}$ cm^{-2} (6×10^{15} cm^{-2}) and is almost independent of the RTA temperature [Fig. 6(b)]. In all cases, the Hall coefficient is positive, indicating hole conduction. Assuming a boxlike constant activation profile over the initially 120 nm (100 nm) amorphized Ge layer, a mean spatial hole concentration of 8.3×10^{20} cm^{-3} (6×10^{20} cm^{-3}) is estimated. The calculated values exceed the concentration of 2×10^{17} cm^{-3} that is needed for the MIT by far.[47] Consequently, the implanted layers behave metallic, as characterized by temperature-independent sheet resistance and Hall fluences (Fig. 7).

Upon surface etching only samples implanted with the high Ga fluence reveal significant changes of the transport properties. Their Hall fluence is nearly halved and the sheet resistance grows about 35%. Assuming a homogenously doped Ge layer, the changes in the Hall fluence would require an etching of about 40% of the conductive Ga-doped Ge layer. Since the Ge is resistant against HF etching,[48] these changes point to the formation of a highly conductive layer at the SiO_2/Ge interface. By applying a parallel conducting two-layer model, the Ga-rich interface layer has a sheet resistance of 53 Ω/sq, which is significantly lower than the value obtained for the Ga-rich layer in Si (∼1 kΩ/sq).[13,14] Due to the ion-beam mixing, this interface layer contains a high amount of Ga, Si, and O, and therefore could be removed by HF etching. The clear difference between the Hall fluences measured before and after etching shrinks with increasing annealing temperature. For the low Ga fluence it is suggested that the observed hole conduction is not dominated by a narrow interface layer because the obtained values are only little effected by surface etching. By correlating the transport properties with the AES spectra (compare Figs. 5 and 6), it turns out that the biggest increase of sheet resistance after surface etching is observed for the samples with the highest Ga concentration at the SiO_2/Ge interface. Therefore we can conclude that the Ga accumulation leads to a highly conductive layer at the interface.

Such Ga-rich interface layers even control the normal state and superconducting transport in Si covered with 30 nm SiO_2 as reported in a recent paper (a summary is given in Table I).[13,14] Due to the higher solid solubility,[6,49] the Ga-rich interface layer in Ge is embedded in a highly doped matrix. The solid solubility in Si is 1 order of magnitude lower and the Ga-rich interface layer is surrounded with a weak conducting matrix, causing a higher sheet resistance.

C. Superconducting state

Under the annealing conditions applied in this study, all unetched samples implanted with 4×10^{16} Ga cm^{-2} exhibit

TABLE I. Comparison of the low temperature properties of Ge and Si implanted with 4×10^{16} cm^{-2} Ga covered with SiO_2. Only samples showing a resistance drop of more than 10% and the onset at 6–7 K are considered.

Parameter	Ge:Ga	Si:Ga [13]
RTA Temperature	830–870 °C	600–700 °C
	Before etching	
R_{Sheet} @ 10 K	12–14 Ω/sq	1–6 kΩ/sq
T_C (onset)	~6 K	7 K
Transition width	>5 K	<2 K
$B_{c,\mathrm{per}}$	0.5 T	8 T
$B_{c,\mathrm{par}}$	0.8 T	14 T
	After etching	
R_{Sheet} @ 10 K	16–19 Ω/sq	~15 kΩ/sq
$T_{\mathrm{C\ onset}}$	<1 K	–

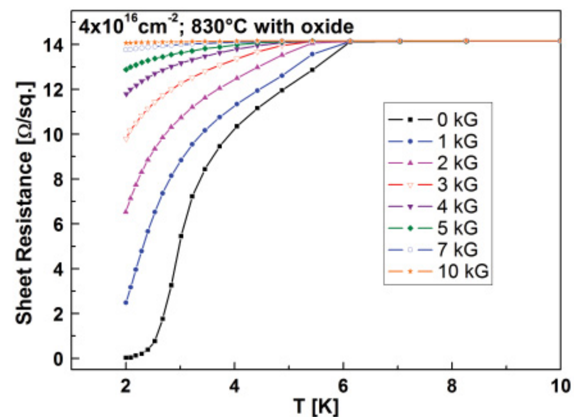

FIG. 8. (Color online) Temperature dependence of the sheet resistance for the 830 °C RTA-processed sample at different applied magnetic fields before surface etching.

a superconducting transition when cooling down, as shown in Figs. 7(a) and 8. The resistance starts to drop at 6 K, a critical temperature comparable with that of amorphous Ga layers.[11,15–17] The onset of superconductivity around 7 K has been observed for Ga-rich layers located at the SiO_2/Si interface in Ga-implanted Si.[13,14] This suggests that this high critical temperature is not a property of p-type doped Ge but might be related to a secondary phase consisting mainly of Ga.

A rather gradual decrease to zero resistance is obtained for samples annealed at 830 °C and 870 °C (Fig. 7). In the case of annealing at 910° there is only a small resistance drop at 6 K, as the residual resistance in the superconducting state is only slightly smaller than in normal conducting case (about 5%). Obviously, superconductivity deteriorates as the sample is annealed at higher temperatures. One can conclude from the AES measurement shown in Fig. 5 that this deterioration is correlated with the disappearance of the Ga-rich interface layer. A high residual resistance is expected when the interface layer breaks into superconducting islands, forming in this way a series circuit of superconducting and normal-state regions. If the width of the normal-state barriers between the superconducting regions is small enough, Cooper-pair tunneling may arise. It is known that the tunneling over varying distances depends on temperature and causes broad temperature ranges for the transition to the zero resistance state.[50–53]

In order to investigate this superconducting state of the samples implanted with 4×10^{16} cm^{-2} Ga in more detail, temperature-dependent sheet resistance measurements at different applied magnetic fields (one example is shown in Fig. 8) were performed. It turned out that the upper critical magnetic field perpendicular to the surface $B_{C2,\mathrm{per}}$ (10% drop at 2 K) is around 0.5 T. By using this critical field, a characteristic value of the superconducting state can be determined in the framework of standard theory.[54] Thus, the Ginzburg-Landau coherence length ξ_{GL} is estimated via $B_{C2,\mathrm{per}} = \Phi_0/(2\pi\xi_{\mathrm{GL}}^2)$ to be ~26 nm. In this equation $\Phi_0 = h/(2e)$ is the magnetic flux quantum with the Planck constant h and the elementary charge e. The coherence length is much larger than the 6 nm (corresponding to $B_{C2,\mathrm{per}} > 9$ T) obtained for Ga-rich layers in Si.[13,14] By applying a magnetic field in-plane the critical field $B_{C2,\mathrm{par}}$ increases to 0.8 T, as much less field expulsion enthalpy is needed. This anisotropy in the critical magnetic field implies that superconductivity occurs in a thin layer. This is contrary to, e.g., superconductivity constrained to spherical clusters where the critical magnetic field would be independent of field direction. As a considerable ratio $B_{C2,\mathrm{per}}/B_{C2,\mathrm{par}} = 0.6$ has been found for Ge:Ga and Si:Ga (Table I), too, this means that in both cases the superconducting layer thickness draws

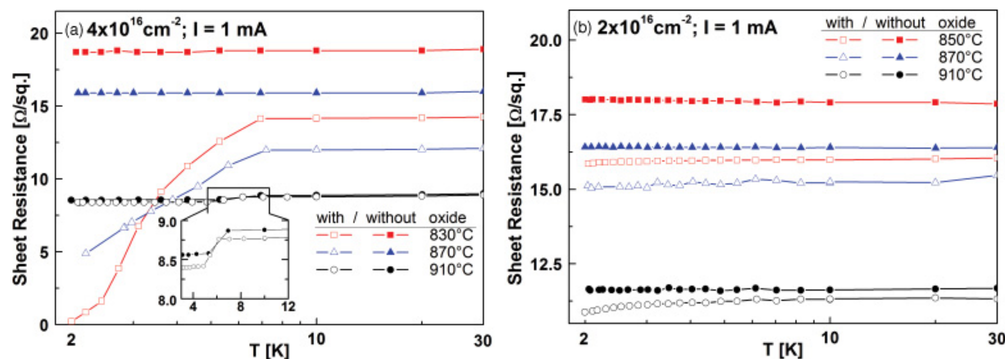

FIG. 7. (Color online) Temperature-dependent sheet resistance measurements before and after surface etching for implantation of (a) 4×10^{16} cm^{-2} and (b) 2×10^{16} cm^{-2}.

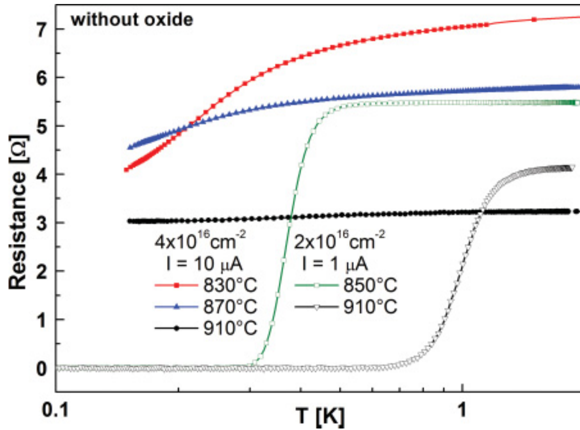

FIG. 9. (Color online) Low-temperature resistance measurements surface etching. Implantation of 4×10^{16} cm^{-2} and RTA between 830 °C and 870 °C leads to an intrinsic superconducting transition below 0.5 K. The low-dose samples show a sharp transition because of the high Ga concentration in the layer.

a restrictive influence on the out-of-plane ξ_{GL}, i.e., indicating that superconductivity in Ge:Ga must be located in a rather broad layer compared to Si:Ga.[54]

Another important parameter is the London penetration depth. It can be estimated, e.g., by calculating the superconducting carrier density from the critical current. In the present case the critical current density is in the order of several A/cm^2, which is more than 100 times smaller than found in the Ga-implanted SiO_2/Si layer stack and very challenging to investigate.[13,14] Another approach would be susceptibility measurements, where conclusions about a possible granularity could be done. However, due to the low volume fraction of the thin layers and the predicted high London penetration depth, it was not possible to detect a reliable signal. Therefore, we refrain from estimating the London penetration depth.

After surface etching, the superconducting transition at around 6 K has vanished [Fig. 7(a)]. This result confirms the idea of a thin superconducting interface layer with high critical temperature, which is now removed. However, some samples still show a decrease in resistance starting at lower temperatures, which may be explained by superconductivity in a lower-lying Ga-doped layer or by an imperfect etching of an interface layer. The corresponding critical temperatures (10% drop) have shifted to 0.46 and 0.28 K for annealing at 830 °C and 870 °C, respectively. These values are comparable to the critical temperatures of highly doped Ge layers, as will be shown below.[3,7,8]

In the samples implanted with 2×10^{16} cm^{-2} Ga, clear hints for the high-temperature transition are lacking [Fig. 7(b)]. In contrast to samples implanted with the high Ga fluence, the samples implanted with 2×10^{16} Ga cm^{-2} also do not substantially change their transport properties after surface etching. Thus, superconductivity, mostly observed at sub-Kelvin temperatures, can be attributed to the whole Ga-implanted layer, which is in correspondence to former works stating doping-induced superconductivity in Ga-doped germanium.[7,8] However, some samples exhibit a superconducting transition even at temperatures slightly higher than 1 K (Fig. 9 sample annealed at 910 °C). When exposed to high annealing temperatures, even low-dose samples may tend to form Ga-rich interface layers.[7] On the other hand, substitutional as well as interstitial Ga atoms may have a crucial influence on superconductivity and may alternatively account for the transition found at 1 K.[8] In addition, there is an evident qualitative difference in the transition behavior of the surface-etched samples implanted with the higher or lower Ga fluence. In the latter case the transition is sharp and complete, whereas the samples implanted with the higher fluence have a very gradual transition and very often, a high residual resistance.

From a microscopic point of view, superconductivity in doped Ge is supposed to depend not only on the hole concentration but on the phonon spectrum as well. The latter is influenced by the substitutional and interstitial Ga. Correlating the recent results to former investigations, Ga redistribution and dose loss during annealing depends on the implanted dose.[12] Therefore the different transition behavior and high residual resistance for 4×10^{16} cm^{-2} could be explained by the low residual Ga concentration.[55,56]

IV. CONCLUSION

It is feasible to fabricate thin superconducting Ga-rich layers with a critical temperature as high as 6 K via ion implantation of 4×10^{16} cm^{-2}, 100 keV Ga, and subsequent rapid-thermal annealing in the temperature range between 830 °C and 890 °C. They are sandwiched between a SiO_2 cover layer and heavily Ga-doped Ge. Although this critical temperature is comparable to recent observations for Ga-implanted Si with an SiO_2 cover layer, the transport properties differ. Critical fields and currents are substantially lower and the normal-state conductivity is much higher than in Si (Table I). When the surface layer is removed or the Ga fluence is lowered to 2×10^{16} cm^{-2}, the critical temperatures are shifted below 1 K, which can be related to superconducting Ga-doped Ge layers.

It turned out that 13-nm, thin SiO_2 layers are not able to protect the Ge surface during implantation. The SiO_2 cover layer is stable when increasing the thickness to 30 nm. After implantation, a 100–120-nm-thick amorphous layer has formed at the surface of the Ge wafer. To initiate recrystallization and Ga redistribution to the SiO_2/Ge interface, 60-s rapid thermal annealing in Ar atmosphere was applied.

All samples are single crystalline with less residual damage for the low Ga dose. With increasing RTA temperature the crystalline grains observed for 4×10^{16} cm^{-2} grow and fewer grain boundaries are observed. The RTA processing leads to a strong Ga redistribution to the SiO_2/Ge interface that seems to be necessary for SPE regrowth. Ga depth profiling reveals the presence of a Ga-rich layer at the SiO_2/Ge interface, but no Ga-containing phase could be detected by XTEM investigations. It seems to be an amorphous Ge:Ga alloy stabilized by O and Si impurities that is difficult to distinguish from the capping layer and can be removed by HF etching.

In summary, we can conclude that a highly conductive Ga-rich layer at the SiO_2/Ge interface is responsible for the superconducting state occurring above 1 K. The low critical magnetic fields of 0.5 T do not indicate a superconducting state driven by Ga clusters. This result correlates with the

structural investigation where all attempts to detect clusters failed. The different normal conducting transport properties and superconducting parameters imply a structural and/or chemical difference to the Ga-rich interface layers obtained in Si covered with SiO_2. After surface etching superconductivity below 1 K is observed in Ge but not for Si.

However, the superconducting properties of Ga-rich interface layers in Ge clearly differ from the parameters obtained for the Ga-doped Ge bulk. Especially the critical temperature is shifted to values comparable to amorphous Ga. Therefore, a certain amount of Ga-rich phases in Ga-doped Ge should lead to an onset of superconductivity around 6 K. It is also shown that the superconducting properties of doped Ge layers cannot be improved by implanting a higher Ga concentration due to the enhanced redistribution to the SiO_2/Ge interface.

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