Si intercalation/deintercalation of graphene on 6*H*-SiC(0001)

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The intercalation and deintercalation mechanisms of Si deposited on monolayer graphene grown on SiC(0001) substrates and after subsequent annealing steps are investigated using low-energy electron microscopy (LEEM), photoelectron spectroscopy (PES), and micro-low-energy electron diffraction (μ-LEED). After Si deposition on samples kept at room temperature, small Si droplets are observed on the surface, but no intercalation can be detected. Intercalation is revealed to occur at an elevated temperature of about 800 °C. The Si is found to migrate to the interface region via defects and domain boundaries. This observation may provide an answer to the problem of controlling homogeneous bi-/multilayer graphene growth on nearly perfect monolayer graphene samples prepared on SiC(0001). Likewise, Si penetrates more easily small monolayer graphene domains because of the higher density of domain boundaries. Upon annealing at 1000–1100 °C, formation of SiC on the surface is revealed by the appearance of a characteristic surface state located at about 1.5 eV below the Fermi level. A streaked μ-LEED pattern is also observed at this stage. The SiC formed on the surface is found to decompose again after annealing at temperatures higher than 1200 °C.

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I. INTRODUCTION

Graphene is one of the most advanced two-dimensional materials of today. The physical structure of graphene is fascinating as it behaves like a 2D crystal in which electrons travel up to micrometer distances without scattering. This makes it superior for transport properties and offers a high potential for technological applications.[1–7] However, for a large-scale integration of graphene-based nanoelectronics, band engineering and access to high-quality graphene sheets on a suitable substrate play equally important roles. SiC is a good substrate candidate since it is a robust wide band gap semiconductor and has a superior range of properties from inert to biocompatible and is excellently suited for high-temperature and high-power applications. Thanks also to the SiC composition, it is possible to sublimate Si atoms at high temperature and leave a single or few layers of graphene/graphite on top of the substrate. This, the so-called epitaxial graphene growth method, can be done either by annealing SiC substrate in vacuum[8] or in an ambient gas.[9–11] The latter method allowed us to achieve large and homogeneous monolayer graphene on SiC(0001) substrates.[12–14] However, depending on application, it is also crucial that bilayer or even multilayer graphene can be grown homogenously on the SiC surface as was obtained for the monolayer case. So far, no one has reported that a large and homogeneous bi- or multilayer graphene can be achieved in a controlled way from the sublimation technique. This is, however, surprising since this epitaxial method has been utilized for quite a number of years, but still many questions about graphene synthesis are unanswered. A solution to this problem may be revealed by investigating the transport behavior of Si atoms through layers of carbon.

In the present work, we have therefore made detailed studies of the transport of Si, specifically the intercalation and deintercalation mechanism for Si atoms deposited on monolayer and 0 ML graphene samples prepared by *ex situ* or *in situ* sublimation of SiC substrates. Results obtained from these graphene samples are presented and compared. Low-energy electron microscope (LEEM) and micro-low-energy electron diffraction (μ-LEED) were used to investigate the surface morphology of the graphene grown and the Si intercalation mechanism. Photoemission data were collected utilizing synchrotron radiation, which allowed high-energy resolution core level and valence band studies.

The results obtained are very interesting since Si is found not to intercalate defect-free graphene, especially the graphene grown by the *ex situ* method. This is distinctly different compared to H, Au, O, and Li, which have been reported to intercalate the graphene layer and at the same time the buffer layer underneath the graphene.[15–21] For the latter case, Li atoms create defects/cracks on the graphene layer and penetrate through those defects to the interface.[21] This is, however, not the case for the Si atoms, which are found to be much more gentle to the carbon layers and do not create any visible defects on the surface when the substrate temperature is kept below 1000 °C. Si intercalation is, however, found to be possible through the existing defect areas or domain boundaries of the graphene layer. Formation of SiC on the surface is observed after annealing at a temperature of 1000–1100 °C.

II. EXPERIMENT

The experiments were performed at two different beamlines at the MAX-lab synchrotron radiation national laboratory. Beamline I311 is equipped with a modified SX-700 monochromator, which provides light for two end stations. The first station is built around a large hemispherical Scienta electron analyzer, which operates at a base pressure of about 1×10^{-10} mbar. A total energy resolution determined by the operating parameter used, of less than 10 to 100 meV at a photon energy from 33 to 450 eV and of less than 300 meV at a photon energy from 600 to 750 eV were selected in the high-resolution photoelectron spectroscopy (PES) studies of the C 1*s*, Si 2*p* core levels and the valence bands reported below. The second station is equipped with a spectroscopic photoemission

and low-energy electron microscope (SPELEEM) instrument. This microscope has a spatial resolution better than 10 nm in the LEEM mode. This station was used for determining the morphology, surface structure, and thickness of the graphene samples. Additional angle-resolved photoemission (ARPES) was performed at beamline I4 at the same facility. This beamline is equipped with a SGM monochromator and a PHOIBOS 100 2D CCD Specs energy analyzer. A low angular dispersion (LAD) lens mode was selected that provided an acceptant angle of $\pm 7^{\circ}$.

The graphene samples were grown on nominally on-axis *n*-type 6H-SiC(0001) substrates with a mis-orientation error within 0.06°. The wafers were production grade *n*-type from SiCrystal with chemical and mechanical polishing on the Si face. The growth of homogeneous monolayer graphene on the 6H-SiC(0001) substrate was performed in two different ways. One was by the *ex situ* sublimation of SiC substrate in a furnace at a temperature of 2000 °C and at an ambient argon pressure of 1 atm.[10,12] The other way was by heating the sample *in situ* at a temperature of about 1300 °C for a few minutes at a base pressure of approximately 10^{-10} mbar. Both methods produced homogeneous carbon layers. The former method gives, however, much larger domains of graphene,[14] but mainly at monolayer thickness. An average of 1–3 ML of Si was then thermally deposited *in situ* on the graphene samples specified below. The substrate temperature was kept at room temperature and also at 800 °C during the Si deposition. The evolution of the Si intercalation with annealing temperature was investigated using PES and also live in front of the objective lens in the SPELEEM station.

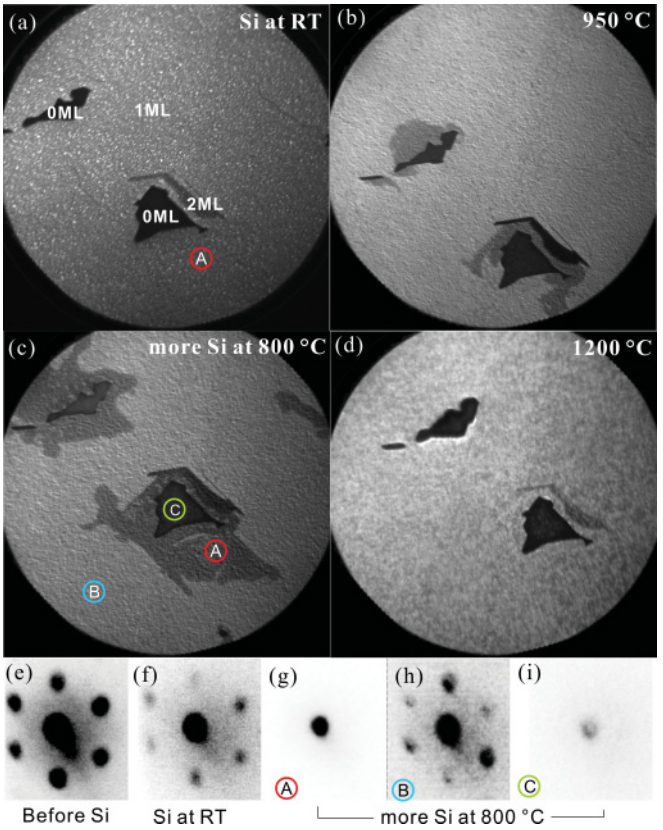

FIG. 1. (Color online) (a) LEEM image of an *ex situ* prepared monolayer graphene grown on SiC(0001) after Si deposition at room temperature, (b) after annealing to 950 °C, (c) more Si deposition at 800 °C, and (d) after annealing to 1200 °C. The same field of view of 20 μm was selected and the starting voltages are 5.2, 4.3, 4.5, and 3.1 eV, respectively. The μ-LEED patterns recorded using $E_{\mathrm{kin}} = 45$ eV from the (0, 1) graphene spot at (e) before, (f) after Si deposition at RT, and (g)–(i) after more Si deposition at 800 °C from the corresponding marked areas in the LEEM image (c).

III. RESULTS AND DISCUSSION

To investigate the intercalation mechanism of graphene, Si was deposited on the *ex situ* grown monolayer graphene sample. The sample was examined using LEEM and μ-LEED, after Si deposition and successive annealing, to identify the number of graphene layers and the morphology. These results are illustrated in Figs. 1(a)–1(i), respectively. It should be noted that a large and homogeneous monolayer graphene sample was typically used as the initial surface.[13,14] For navigation and illustration purposes, we chose to show an area that contains also 0 and 2 ML of graphene, as determined from recorded electron reflectivity curves. Directly after Si deposition (∼2 ML) at room temperature, a rougher surface morphology was detected, as revealed by the grainy appearance of the 1 ML area. However, no change in graphene thickness was observed at this stage, i.e., the majority coverage was still 1 ML graphene with some small areas with 0 ML (buffer layer) and 2 ML, as indicated in Fig. 1(a). This was also confirmed by the μ-LEED patterns in Figs. 1(e) and 1(f), which are focused on the (0, 1) graphene spot in the diffraction pattern. These patterns were collected from the 1 ML area marked "A" and reveal the graphene spot and the six surrounding buffer layer spots before and after Si deposition. Thus this indicates that no intercalation has happened at this stage. The buffer layer spots ($6\sqrt{3}$ spots) appear, however, a little bit fainter after Si deposition. This is suggested to be related to the presence of Si on the graphene surface. After annealing at 950 °C, Fig. 1(b), changes were clearly detected around the 0 ML islands. This was even more pronounced when a similar amount of Si was deposited on the substrate while keeping the substrate temperature at 800 °C, as displayed in Fig. 1(c). These new modified areas around the 0 ML islands are suggested to be areas where Si has penetrated to the interface and transformed the existing buffer layer to an addition graphene layer. This finding was confirmed by the μ-LEED pattern in Fig. 1(g), collected from the same area "A" as in Fig. 1(f) and indicating a vanishing of the $6\sqrt{3}$ spots. The same results were obtained using μ-PES and $I - V$ LEEM, by which no buffer layer component was possible to observe in the C 1*s* spectrum and the I-V curve showed two dips from these new modified areas. The diffraction pattern of area "B", Fig. 1(h), still shows the graphene and the buffer layer spots indicating that no intercalation has taken place there. Moreover, only the graphene spot, i.e., no buffer layer spots, was observed in the μ-LEED pattern collected from the island marked "C" in Fig. 1(i), which before Si deposition was a 0 ML island. After annealing, the sample at 1200 °C, these new gray modified areas can no longer be observed as seen in Fig. 1(d). From these observations, we suggest that the Si atoms go to the interface region through defect

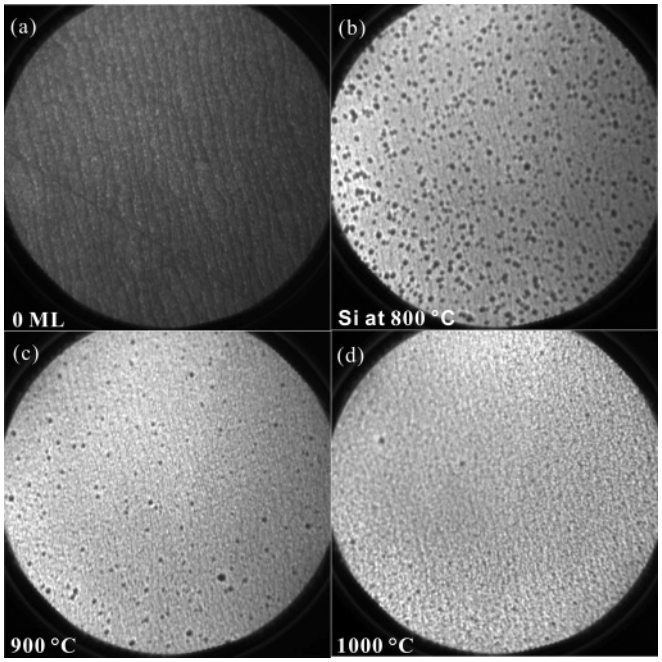

FIG. 2. (a) LEEM image of an *in situ* buffer layer grown on SiC(0001) before Si deposition, field of view (FOV) is 20 μm, (b) after Si deposition at 800 °C, FOV is 25 μm, (c)–(d) after annealing to 900 and 1000 °C, respectively, FOV is 25 μm. The starting voltages are 3.3, 0.5, 0.7, and 0.3 eV, respectively.

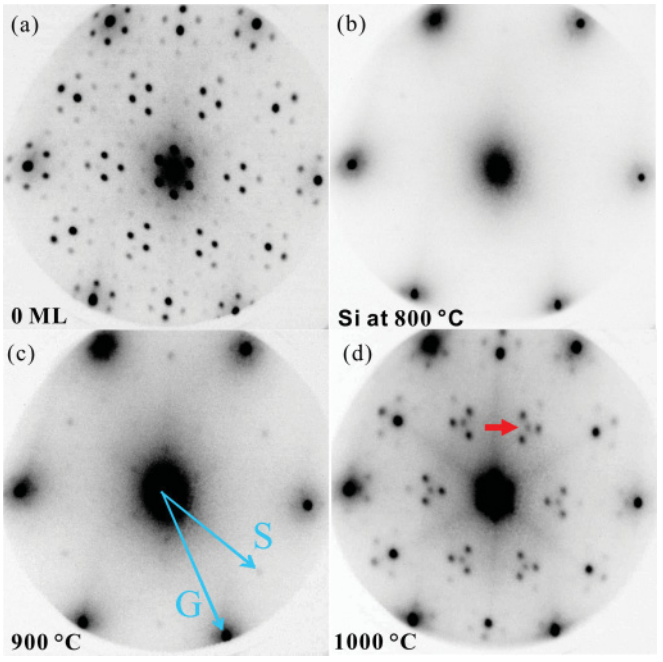

FIG. 3. (Color online) μ-LEED patterns recorded at $E_{kin} = 45$ eV from (a) 0 ML graphene, (b) after Si deposition at 800 °C, (c)-(d) after annealing to 900and 1000 °C, respectively. The arrow(s) in (c) indicate substrate (S) and graphene (G) spots, in (d) indicates the $\sqrt{3}$ spots.

areas/domain boundaries and propagate upon heating as long as there is Si on the surface. The possibility of Si penetration directly through the graphene monolayer can be excluded since the intercalated modified gray areas do not cover the whole sample surface. If the mechanism of incoming and outgoing Si atoms is similar (i.e., the penetration/intercalation of Si deposited on the surface and escape of Si atoms from the SiC substrate through the graphene during sublimation growth), these results may also hint the answer to the question why is it so difficult to make a large homogeneous bilayer graphene sheet by the sublimation method. This method is known to produce large homogeneous monolayer graphene sheets, which make it difficult for the Si atoms to escape from the sample to produce large homogeneous 2 ML graphene sheets. Support for this idea is offered by our observation that Si intercalation goes easier on *in situ* grown graphene samples, as presented next.

LEEM images of an *in situ* prepared graphene sample before, after Si deposition, and successive annealing are presented in Figs. 2(a)–2(d), respectively. From the C 1*s* core-level spectrum recorded before Si deposition, the graphene coverage was estimated to be about 0.3 of a monolayer, i.e., a carbon buffer layer (0 ML) and 1 ML islands covering about 30% of the surface. This was also confirmed by the μ-LEED pattern in Fig. 3(a), showing an intense $(6\sqrt{3}\times6\sqrt{3})$ R30° pattern. This sample was, however, as expected, homogeneously intercalated directly after Si deposition at 800 °C. The μ-LEED pattern then shows only a (1×1) pattern indicating that a full graphene layer has been created. However, small dark spots are visible on the surface directly after Si deposition those are reduced upon annealing, as illustrated in Figs. 2(b)–2(d), respectively. These dark spots become very bright in XPEEM images collected when setting the energy to the binding energy of pure Si. Therefore we can conclude that these dark spots originate from Si clusters on the surface after Si deposition. The corresponding μ-LEED patterns, in Figs. 3(c)–3(d), show that the SiC substrate spots and the $6\sqrt{3}$ buffer layer spots become visible after annealing at 900 °C and more pronounced at 1000 °C, respectively. More interestingly, faint streaks from the center to the SiC spots and also weak spots from a $(\sqrt{3}\text{x}\sqrt{3})$R30° reconstruction are visible in Fig. 3(d), i.e., after annealing at 1000 °C. The origin of these streaks and $\sqrt{3}$ spots is unclear at this stage but can indicate formation of islands of SiC on the surface, and is further discussed below. An intense $(6\sqrt{3}\times6\sqrt{3})$ R30° pattern, like the one in Fig. 3(a) was again observed after annealing the sample at 1300 °C.

Detailed high-resolution photoemission studies of the core levels and valence band were also performed. This graphene sample was prepared *in situ* and the sample was kept at room temperature during Si deposition. A series of C 1*s* spectra acquired at a photon energy of 600 eV before and after Si deposition plus successive annealing cycles is shown in Fig. 4(a). Applying a fitting procedure[22] showed that three components are required for producing good fits. These three components correspond to the bulk SiC (B), graphene (G), and interface buffer layer (I), respectively. From the G/B intensity ratio and a simple layer attenuation model, a graphene thickness of about 1 ML is estimated. The C 1*s* spectrum remains unchanged after Si deposition and annealing up to 600 °C. This confirms that there is no migration of Si atoms through the graphene and interface layers at these stages. Interestingly, after annealing the sample at 800 °C for only

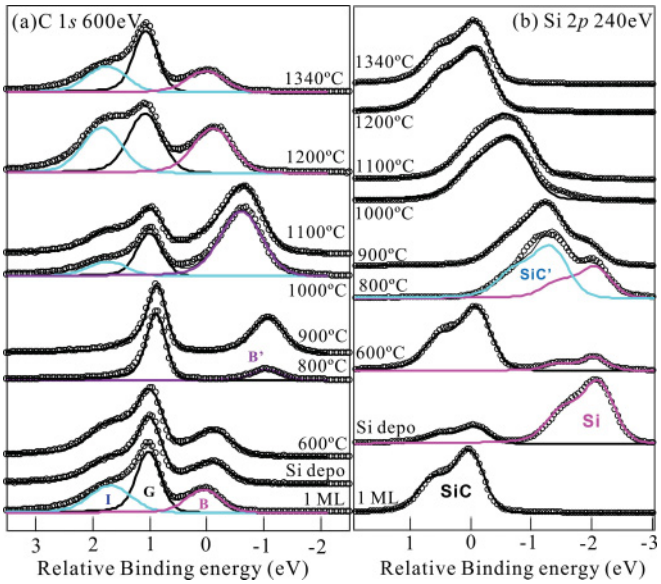

FIG. 4. (Color online) (a) C 1*s* spectra recorded using a photon energy of 600 eV from an *in situ* prepared monolayer graphene on SiC(0001), after Si deposition at RT and after successively annealing. (b) Si 2*p* spectra recorded using a photon energy of 240 eV from the similar sequence used in (a).

1 min, the interface component is significantly reduced and the G/B ratio is increased by almost a factor of two. This indicates a transformation of the buffer layer into an additional new graphene layer. At the same time, the B component (now labeled B') is also shifted by about 1 eV, which indicates a change of the coulomb charge environment in the interface region. Such a change of the dipole layer at the interface was earlier reported upon hydrogen and Li intercalations,[15–17,20,21] but the shifts were then found to be slightly different, i.e., about 0.7 and 2 eV, respectively. Upon further successive annealing at temperatures up to 1200 °C the G/B ratio is found to decrease, as seen Fig. 4(a). This indicates that the two graphene layers formed at 800–900 °C are now transformed back to buffer layer carbon and SiC, respectively. That the carbon buffer layer starts to form again is obvious from the reappearance of the buffer layer peak (I) at these annealing temperatures. It is, however, puzzling that the sum of the graphene and buffer layer signals versus the SiC signal, i.e., the (I+G)/B intensity ratio, has decreased compared to the initial surface. This suggests formation of SiC, which the increase in relative strength of the B signal also indicates, and we can at this stage only speculate/suggest that islands of SiC form on the surface when annealing at temperatures of 1000–1100 °C. After annealing at 1340 °C, the G/I and G/B ratios are fairly similar to the initial surface so the 1 ML graphene sample with a carbon buffer layer has been restored.

The Si 2*p* spectrum collected at a photon energy of 240 eV, before and after Si deposition and after annealing at the same successive temperatures, is shown in Fig 4(b). Similar trends are revealed in these spectra. Before Si deposition, the Si 2*p* spectrum exhibits one doublet with the Si $2p_{3/2}$ at a binding energy of 101.3 eV. This doublet originates from the SiC substrate. After Si deposition, another doublet (labeled Si) appears at a lower binding energy and corresponds to pure Si on the surface. From a simple layer attenuation model an average of 3 ML of Si can be estimated. This extra Si is found to reduce dramatically already after annealing at 600 °C. There is no indication of intercalation at this stage. After annealing at 800 °C the bulk SiC peak, now labeled SiC', is shifted by about 1.2 eV to lower binding energy confirming a change of the dipole layer at the interface by Si intercalation, as expected from the C 1*s* results. These findings also support the above LEEM and μ-LEED results that showed that the Si atoms intercalate directly when the sample temperature is kept at 800 °C during deposition, c.f., Figs. 1(c), 2(b), and 3(b). These results clearly show that a temperature of around 800 °C is crucial to activate Si diffusion/intercalation through defects/grain boundaries of graphene and buffer layer. After annealing at 1000 °C the bulk SiC peak is seen to shift back by ∼0.7 eV and to be slightly broader compared to the initial substrate peak. This broadening is also observed in the C 1*s* spectrum at the same annealing temperature. A Si 2*p* peak shape similar to the initial surface was obtained again already after annealing at 1200 °C. It should be noted that similar results were obtained from the different *ex situ* and *in situ* prepared graphene samples, although the core level results presented above were all from one of the *in situ* prepared samples. Similar results were also obtained after Si deposition at room temperature and annealing at 800 °C as after Si deposition with the sample at 800 °C.

Valence band spectra recorded after Si deposition and after successive annealing steps using a photon energy of 140 eV are shown in Fig. 5(a). Before and after Si deposition, a strong graphite-like C 2*s* derived feature appears at a binding energy

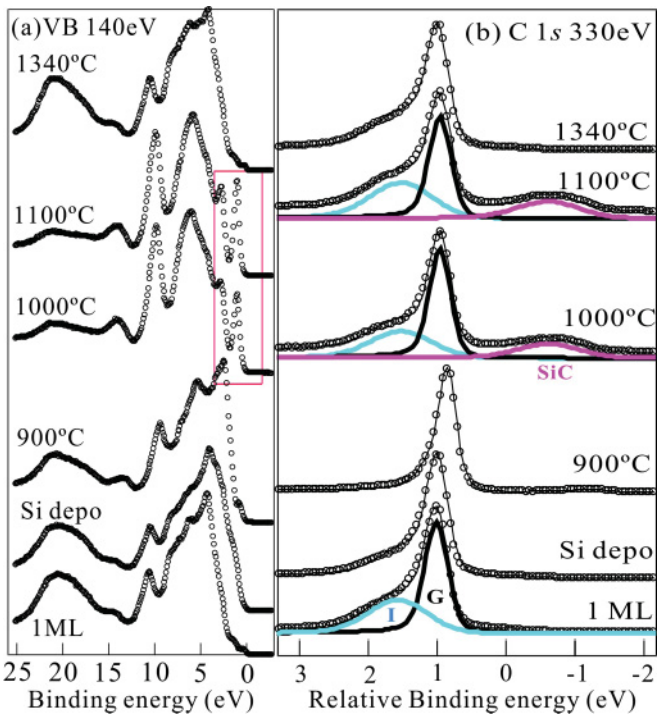

FIG. 5. (Color online) (a) Normal emission valence band spectra recorded at a photon energy of 140 eV after Si deposition at RT and after successive annealing. The red box indicates the surface state from SiC surface. (b) C 1*s* spectra recorded at a photon energy of 330 eV from the similar sequence.

around 20 eV and features originating from hybridization of C $2p$ and Si $3s + 3p$ states at binding energies between 2 and 12 eV. These features remain after annealing up to 900 °C, but the relative intensities are seen to change. After annealing the sample at 1000 and 1100 °C, the C $2s$ feature is significantly reduced in intensity and the shape of valence band spectrum has transformed from a graphite like shape to a more SiC-like valence band. Valence band spectra for the $(\sqrt{3}\times\sqrt{3})$R30° and $6\sqrt{3}\times6\sqrt{3}$R30° reconstructed SiC(0001) surfaces have been published earlier.[23,24] A characteristic for the $\sqrt{3}$ surface is the strong surface state[24] appearing at about 1.5 eV below the Fermi level, that is very sensitive to surface contamination and gas exposures. Since such a surface state is observed in the valence band spectrum collected after annealing at 1000 and 1100 °C, see Fig. 5(a), it can be concluded that SiC has formed on the surface. This was indicated by the C $1s$ spectra in Fig. 4(a) but is really confirmed by the C $1s$ spectra collected using photon energy of 330 eV shown in Fig. 5(b). At this photon energy, it is typically not possible to detect photoelectrons originating from the SiC substrate from a sample on which 1 ML of graphene has been grown, as demonstrated by the bottom curve in Fig. 5(b). In fact, the first three spectra from the bottom show no signal from SiC, illustrating that there is no SiC within the probing depth. However, after the sample is annealed at 1000 and 1100 °C, a weak peak is detectable at a very similar binding energy as where the bulk SiC normally is located. This illustrates that the SiC formed is located at the surface, i.e., within the uppermost surface layers. This extra peak disappears again, like the surface state does, after annealing at higher temperatures. These results also support the LEED results in Fig. 3(d) where $\sqrt{3}$ spots and weak streaks are observed in the (0,1) directions when referring to the SiC substrate diffraction spots. The streaklike features occur normally when features of short-range order are formed on the surface and therefore we suggest that the formation of SiC is in the form of small islands on the surface. This is in agreement with the observation concerning the C $1s$ spectrum, that the SiC peak becomes broader and has a higher relative intensity in this temperature range. The formation of SiC may also explain why formation of an ordered oxide, silicate, sometimes is observed, particularly after *ex situ* sublimation growth of graphene on the C-face SiC surface. The reason can be that either elemental Si remains on the surface or that SiC is formed. Since both are sensitive to oxygen, formation of an oxide on top of the graphene is then likely to result when the sample is exposed to air.

Angle-resolved photoemission (ARPES) spectra were collected at around the K point of the graphene Brillouin zone, using a photon energy of 33 eV, see Fig. 6. The initial monolayer graphene shows a single π-band crossing the Dirac point at an energy of ∼0.4 eV below the Fermi level, as displayed in Fig. 6(a). If a linear dispersion of the π band at around the Dirac point is assumed, a doping concentration of 1×10^{13} cm^{-2} can be estimated,[25] which corresponds to the electron transfer from the SiC substrate. No change of the π band is observed directly after Si deposition or annealing at temperatures below 800 °C, Fig. 6(b). After annealing the sample at 800 °C for one minute, the π band is split in two. This indicates the transformation of buffer layer carbon and 1 ML graphene into 2 ML graphene upon Si intercalation. A slight shift of the Dirac point toward the Fermi level is also observed at this temperature. Further annealing at 900 and 1000 °C, see Figs. 6(d)–6(e), results in a shift of the Dirac point to about

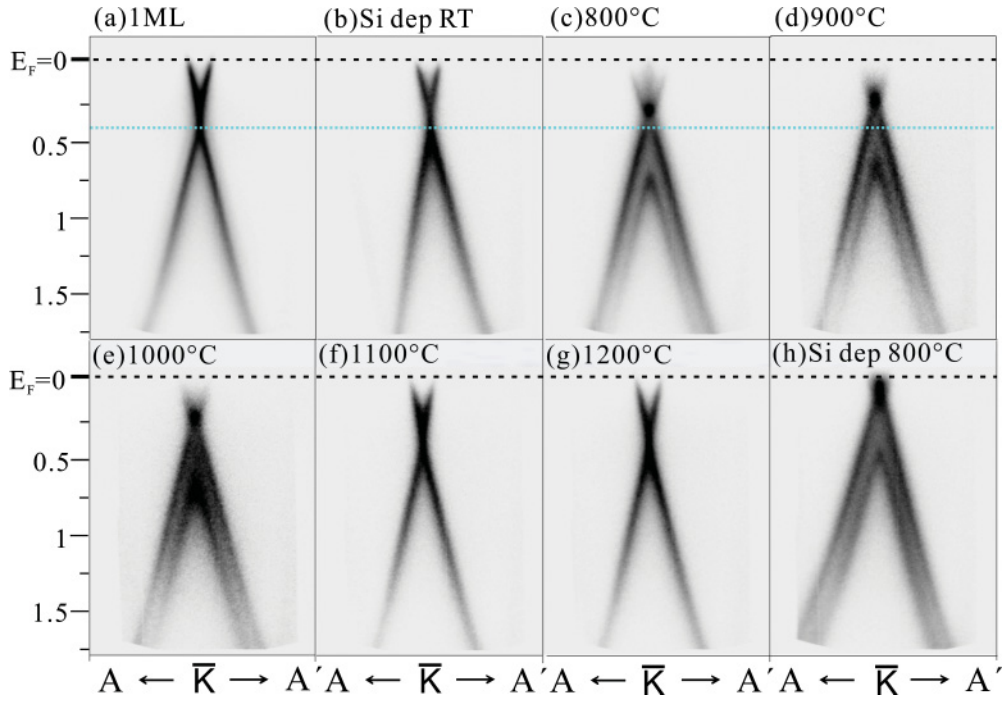

FIG. 6. (Color online) The π band around the K point recorded from (a) monolayer graphene, (b) after Si deposition at RT, and (c)–(g) after successive annealing to 800, 900, 1000, 1100, and 1200 °C, respectively. For comparison, the π band recorded after Si deposition at 800 °C for a longer time is also included in (h).

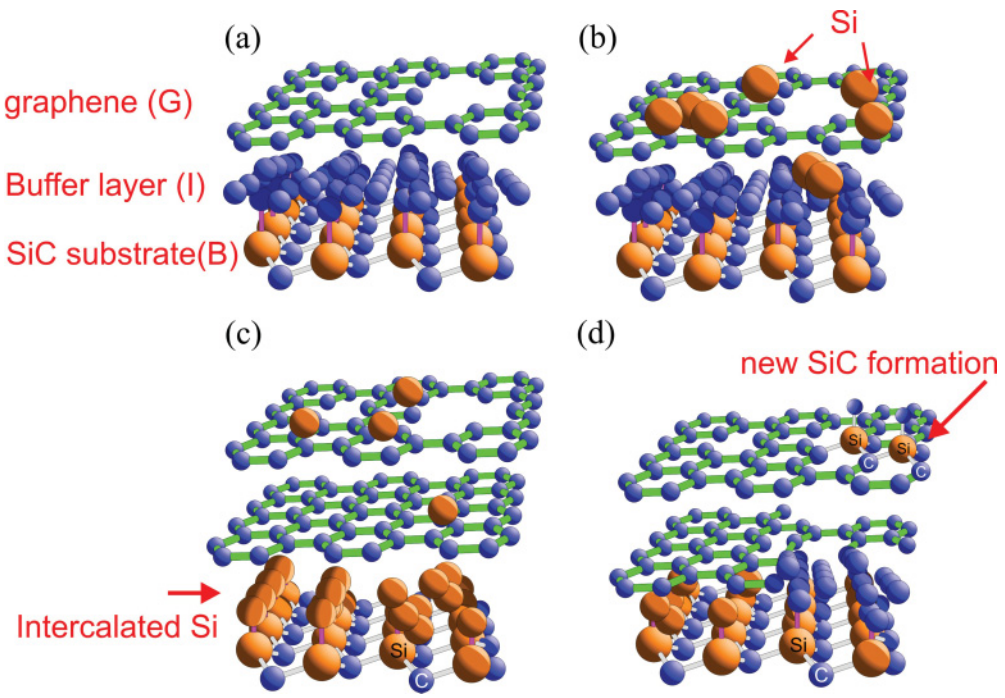

FIG. 7. (Color online) (a) A schematic structural model for monolayer graphene on the SiC(0001) substrate including a strongly bound ordered $(6\sqrt{3}\times 6\sqrt{3})$R30° carbon buffer layer at the interface and defects in the graphene sheet. (b) The structural model suggested after Si deposition at RT, (c) after annealing at ∼800 °C resulting in a Si intercalated layer and bilayer graphene and (d) after annealing at ∼1000 °C, when partial deintercalation and SiC formation on the surface has occurred.

0.2 eV below the Fermi level. After annealing at 1100 °C or higher, only one π band with the Dirac point at the initial position at ∼0.4 eV below the Fermi level is again possible to detect. In Fig. 6(h), the π-band structure obtained after Si deposition for about an hour on a sample kept at 800 °C is illustrated. A longer annealing and deposition time enhances, as expected, the intercalation process. The Dirac point in this case, see Fig. 6(h), is located very closely to the Fermi level indicating an essentially full suppression of the charge transfer from the substrate.

From our findings, we suggest a schematic structural model for the Si intercalation and deintercalation mechanisms as illustrated in Fig. 7. A monolayer graphene grown on a SiC(0001) substrate plus the ordered and strongly bound carbon buffer layer at the interface is displayed in Fig. 7(a). The holes in the graphene layer represent defect areas that can be regarded to describe 0 ML graphene areas like the ones observed in the LEEM image in Fig. 1(a). After silicon deposition at room temperature (RT), we suggest that most of the Si remains on top of the graphene layer or on top of the buffer layer, as illustrated in Fig. 7(b), since no intercalation was observed at RT. Upon annealing at about 800 °C, Fig. 7(c), Si was found to migrate through the existing defects in the graphene sheet and the buffer layer and consequently passivate the Si dangling bond at the SiC-buffer layer interface. This results in a silicon intercalation layer in between the SiC substrate and the two carbon layers and a decoupling of the buffer layer from the SiC substrate so it is transformed into a second graphene layer. The model thus explains the disappearance of the $6\sqrt{3}$ buffer layer spots in the LEED pattern [see Figs. 1(g) and 3(b)] and of the interface "I" component in the C 1*s* spectrum [see Fig. 4(a)], which both are characteristics of the strongly bound carbon buffer layer. It also explains the splitting of the single π band into the two π bands [see Figs. 6(c) and 6(h)] characterizing 2 ML of graphene. Upon annealing the sample at about 1000 °C, Si was found to gradually leave the interface region resulting in a partial deintercalation as demonstrated in Fig. 7(d). This was concluded from the re-appearance of the $6\sqrt{3}$ spots in the LEED pattern [see Fig. 3(d)] and of the interface component "I" in the C 1*s* spectrum [see Fig. 4(a)]. Apart from this, formation of SiC in the topmost surface layers is also illustrated in the model. This explains the appearance of the (1×1) SiC and also the $(\sqrt{3}\times\sqrt{3})$R30° diffraction spots in the LEED patterns in Figs. 3(c) and 3(d), respectively. The C 1*s* spectra in the Fig. 4(a) suggest the same since the SiC component increase in relative intensity after annealing at 1000–1100 °C. That SiC really was formed in the surface layer could be concluded from the SiC component detected in the most surface sensitive C 1*s* spectra shown in Fig. 5(b), i.e., at the photon energy of 330 eV, and from the observation of the $(\sqrt{3}\times\sqrt{3})$R30°-SiC surface state in the valence band spectra in Fig. 5(a), (red box).

That Si does not easily migrate/penetrate through the monolayer graphene sheet but through the buffer layer is quite apparent from the LEEM results shown in Fig. 1, but the reason for this is not clear. The chemical composition of the buffer layer should be very similar to the graphene layer since it can be transformed into a graphene sheet when there is no strong interaction with the substrate. However, a recent study[26] of the buffer layer has suggested it to contain a fairly high concentration of defects [hexagon-pentagon-heptagon ($H_{5,6,7}$) type

defects] compared to an ideal graphene layer. The existence of heptagon defects may allow for an easy migration/penetration of Si atoms through the buffer layer while this is difficult for a carbon layer without such defects. These findings may therefore explain a reason why the growth of defect-free, large and homogeneous bilayer graphene sheets is very tricky when the first nearly perfect graphene layer has formed.

IV. CONCLUSIONS

Detailed studies of the intercalation and de-intercalation mechanism for Si deposited on monolayer graphene samples prepared in different ways on SiC(0001) substrates are reported. The Si is observed not to be able to penetrate through monolayer graphene when the sample is kept at room temperature. Intercalation is revealed to occur at an elevated temperature of about 800 °C and then the Si atoms are found to migrate through the graphene at domain boundaries and likely other defect areas. This is different compared to recent findings concerning Li intercalation of monolayer epitaxial graphene on SiC,[20,21] where Li-based compounds were formed, which created defects/cracks on the surface that consequently allowed Li to penetrate the carbon layer already at room temperature. The relative inertness of Si in turn provides an explanation for the graphene growth mechanism on SiC surfaces since the Si involved in the process escapes from the substrate and leaves behind carbon atoms to form graphene. As far as the sublimation technique is concerned, it is a real challenge to control the uniformity of the second graphene layer when the first graphene layer is a nearly perfect sheet. The Si atoms are found to intercalate only when the substrate temperature is kept at around 800–900 °C, and not at lower temperatures. Intercalation of Si is also found to increase with time and to shift the Dirac point closer to the Fermi level. At higher annealing temperatures, 1000–1100 °C, formation of SiC on the sample surface is observed, which can induce oxide formation when the sample is exposed to air.

ACKNOWLEDGMENTS

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