Tunable thermal conductivity in defect engineered nanowires at low temperatures

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We measure the thermal conductivity (κ) of individual InAs nanowires (NWs), and find that it is three orders of magnitude smaller than the bulk value in the temperature range of 10–50 K. We argue that the low κ arises from the scattering of phonons in the random superlattice of twin defects oriented perpendicular to the axis of the NW. We observe a significant electronic contribution arising from the surface accumulation layer, which gives rise to the tunability of κ with the application of an electrostatic gate and a magnetic field. Our devices and measurements of κ at different carrier concentrations and magnetic field offer a means to study unique aspects of nanoscale thermal transport.

Thermal transport measurements on semiconducting nanowires (NWs) have attracted a lot of attention in the past few years. Measurements of thermal transport in nanostructures are important as they provide a platform to test the existing descriptions of phonons in confined structures and across complex interfaces,[1] and have the potential to result in technological applications as thermoelectric systems.[1–3] Different materials are benchmarked using the thermoelectric figure of merit $ZT = \frac{S^2 T}{\rho \kappa}$, where S is the Seebeck coefficient, ρ is the electrical resistivity, κ is the thermal conductivity, and T is the absolute temperature. ZT can be increased by appropriate engineering of the nanostructures. One of the ways to increase ZT is by reducing κ without degrading its electrical conductivity and its Seebeck coefficient.[4] As a result, an ideal thermoelectric material is a glass for phonons and is ordered for electronic transport. Recently, several theoretical models as well as experimental studies have been carried out in different semiconductor NWs such as Si, Ge, Bi_2Te_3, etc.[5–9] It is found that for Si NWs the value of κ is reduced by two orders of magnitude[5,8,9] as compared to bulk values, by tuning the roughness of the surface. III-V semiconductors are also known to be good thermoelectric materials, and theoretical studies suggest that InSb and InAs NWs are good candidates for better ZT.[10] InAs NWs have been studied extensively to probe their charge and spin transport.[11–13] An aspect of InAs NWs that makes studying their thermal transport—hitherto little explored[14,15]—of interest is the ability to tune the density of twin defects and polytypes along its length by varying the growth parameters.[16–20] Exploiting this control over the crystal structure can help synthesize defect-engineered NWs, whose lattices have aperiodic arrays of twins along their lengths that modify phonon behavior, with the electron transport affected[20] to a lesser extent. Such NWs satisfy the key criteria for a good thermoelectric material—localization of phonons with comparatively less localization of electrons.

In this Rapid Communication we explore the κ of suspended InAs NW field-effect transistors (FETs); the NWs have a high density of aperiodic twins and polytypes perpendicular to their axis.[16–18,20] Defects suppress κ_{ph} (the phonon contribution to κ), resulting in reduction of thermal conductivity

by three orders of magnitude from the bulk. Our method also has an advantage, which is to study κ as a function of carrier concentration without introducing additional impurities. We observe a significant change in the thermal conductivity with the application of a gate voltage, suggesting a finite electronic contribution, and we propose that this contribution comes from the conduction electrons at the surface accumulation layer which is inherent in low band-gap semiconductors such as InAs and InN.[21–23] To confirm the role of the electronic contribution, we apply a magnetic field and see considerable changes in the thermal conductivity.

The InAs NWs used to fabricate the devices in this work were grown in a metalorganic chemical vapor deposition (MOCVD) system using the vapor-liquid-solid (VLS) technique on a $\langle 111 \rangle B$-oriented GaAs substrate. NWs of 100–200 nm diameter were used in this experiment. Here, 10–12 μm long NWs were chosen for making four-probe suspended devices ($\sim$200 nm above the surface) on a 300-nm-thick, SiO_2 coated degenerately doped Si wafer, which serves as the back gate (such that the gate dielectric is a combination of vacuum and SiO_2—growth and device fabrication details are given in Ref. 24). Figure 1(a) shows the schematic of the device and the circuit for electrical and thermal measurements. Figure 1(b) shows a scanning electron microscope (SEM) image of a device. The gold electrodes provide mechanical support and Ohmic contacts with negligible contact resistance to the suspended NW, besides thermally anchoring it at four points to the bath temperature T_b. The electrical properties of the device are characterized as a function of gate voltage (V_g) and temperature before detailed thermal transport measurements are made. Figure 1(c) shows the resistance R of a typical device as a function of V_g at a fixed value of T_b. The n-type field-effect transistor (FET) behavior of the suspended NW devices is clearly seen. Figure 1(d) shows the evolution of R as a function of temperature T and also the corresponding linear fit in the temperature range 10–50 K.

High-resolution transmission electron microscopy (TEM) studies were used to characterize the microstructure of our NWs. Figure 2(a) shows a large-scale TEM image of a NW,
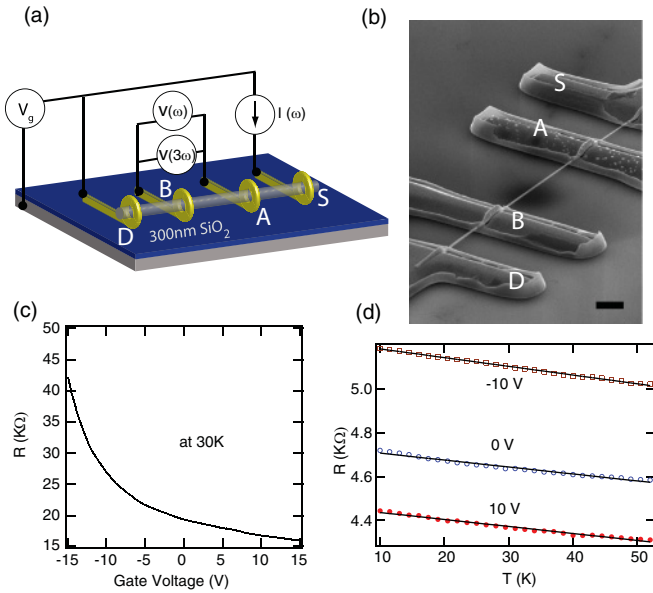
(a)

(b)

(c)

(d)

FIG. 1. (Color online) (a) Schematic of the four-probe suspended NW device and the circuit used for measuring electrical signals for both electrical and thermal transport. (b) A tilted scanning electron microscope image of a device showing the source (S) and drain (D) electrodes and voltage probes A and B. The scale bar corresponds to 1 μm. (c) Resistance as a function of gate voltage V_g at a bath temperature of 30 K for a typical device. (d) Resistance R as a function of temperature for a device at three different gate voltages V_g. The solid curves show linear fits to the data.
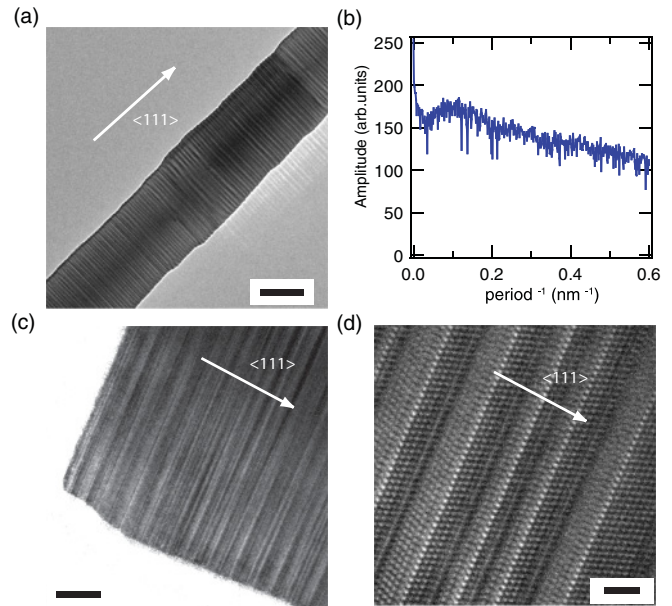
(a)

(b)

(c)

(d)

FIG. 2. (Color online) (a) TEM image of an InAs NW showing twin boundaries perpendicular to the axis of the NW. The scale bar is 50 nm. (b) Fourier amplitude of the intensity modulation along the length of the NW that shows no sharp peaks. (c) A closeup image showing the twin interfaces and the resulting zigzag surface roughness of the NWs. The scale bar is 10 nm. (d) TEM image showing the atomic fringes and the orientation of the twin boundaries and polytypes. The scale bar is 2 nm.

where we observe an aperiodic arrangement of the twin superlattice perpendicular to its axis. The fact that the lattice has defects but lacks a long-range periodicity is reflected in the Fourier amplitude [seen in Fig. 2(b)] that has no sharp peaks along the length of the NW. Figures 2(c) and 2(d) show a detailed view of the twins and polytypes.[16–18,20] The typical spacing of these defects is ∼3–5 nm. Once the electrical and structural characterization is done, we perform simultaneous thermal and electrical measurements.

One method of measuring the thermal properties of nanostructures uses a modification of the 3ω technique[25] for κ and specific-heat measurement. The modified 3ω technique[26–28] relies on fabricating suspended four-probe devices with the conducting NW serving both as a heater and a thermometer. The magnitude of $V(3\omega)$ can be related to κ (in the limit $\omega\gamma \to$ 0, where γ is the thermal time constant of the NW) as[26,27]

$$V(3\omega) = \frac{4(I(\omega))^3 R R' L}{\pi^4 \kappa A}, \quad (1)$$

where ω is the angular frequency of the ac current, $I(\omega)$ is its amplitude, R and R' are the resistance and the derivative of resistance with respect to temperature, respectively, L is the length of the NW between the two middle probes, and A is its cross section.[26,27] Figure 3(a) shows the schematic of the temperature profile along the length of the NW. For our devices, L is 2–4 μm and the thermal time constant γ can be estimated to be ∼10^{-5} s (details of the phase information of the 3ω signal in the limit of $\omega\gamma \to 0$ are given in Ref. 24).

To measure κ at each temperature value, we vary the current [$I(\omega)$] and obtain κ from the fitting of Eq. (1) to the

measured $V(3\omega)$ as a function of injected $I(\omega)$. Figure 3(b) shows the evolution of $V(3\omega)$ with $I(\omega)$ along with the cubic power-law relationship that is essential to ensure that the 3ω technique is applicable within the applied current regime (to eliminate other sources that can possibly show cubic scaling, see Ref. 24). As we vary the temperature, we also record the resistance. We determine R' from the derivative to the linear fit to the R-T plot [see Fig. 1(d)]. The variation of R with T becomes small and nonmonotonic above 50–60 K, and this is the reason we chose the temperature range of 10–50 K in our experiment. The phase of the 3ω signal is measured to be zero at all temperatures (see Ref. 24, Fig. S3). This procedure of fitting the power law given by Eq. (1) at each instance of the parameter space allows us to extract κ as a function of V_g and temperature. We have calibrated our technique using lithographically fabricated 170-nm-wide, 75-nm-thick gold NWs in the temperature range of our measurement and obtained a Lorenz number (L_0) of ∼2.4 × 10^{-8} W Ω K^{-2}, which is close to the L_0 for bulk gold[29] (see Ref. 24) which calibrates the measurement technique we have used.

Figure 3(c) shows the plot of measured κ as a function of temperature at two values of V_g. The overall magnitude of κ is ∼1000 times smaller than the bulk values (∼300 W/mK at 50 K; see Ref. 24, Fig. S15). This is a significant reduction in κ, and the measured value is similar to the minimum thermal conductivity model of Cahill et al.[30] (CWP model) based on the assumption that the material is highly disordered. A similar reduction in κ, beyond the CWP model, was also observed in disordered WSe$_2$, which is a layered structure.[31] Later we return to a model to understand this better. A similar
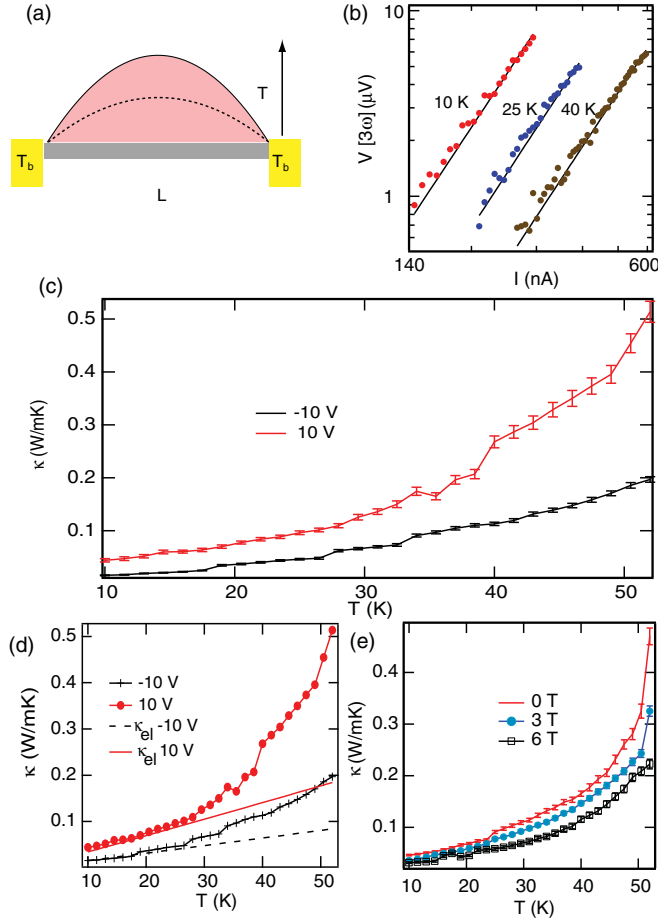
FIG. 3. (Color online) (a) The temperature profile along the length L of the NW with the red (light gray) shaded area indicating the amplitude of oscillations. (b) The measured $V(3\omega)$ signal as a function of the excitation current $I(\omega)$ for three different temperatures T. The solid line shows the fit to the cubic power law [Eq. (1)]. (c) Plot of κ as a function of temperature for two different gate voltages. (d) Measured κ as a function of temperature together with electronic contribution $\kappa_{\rm el}$. (e) Measured κ for the same device at three different magnetic fields as a function of the temperature at zero gate voltage.

evolution of κ is also observed at different values of V_g in all the measured devices (see Ref. 24, Figs. S11–S13).

Now we consider the effect of V_g on κ. It is clear that the electrical conductance of the semiconducting NW FET can be modified as a function of V_g [Fig. 1(c)]. However, the effect of electron density variation is not expected to affect κ in most semiconducting materials, as phonons are the dominant carriers of heat.[32] Direct calculation from electrical conductivity using the Wiedemann-Franz (WF) law gives a small value of the electronic contribution ($\kappa_{\rm el}$) which does not explain the variation we see with V_g (see Ref. 24). To understand the origin of large $\kappa_{\rm el}$, we have to first understand the material property of the InAs wire. It is well known that in InAs there is an accumulation of charge at the surface. The resultant downward band bending pins the surface Fermi level above the conduction-band minimum.[21–23] In a geometry where the surface-to-volume ratio is large, such as NWs, this surface accumulation charge (SAC) plays a major role in

the electrical transport. The SAC takes part in the electrical conduction and scatters due to roughness at the surface, which is also the reason for the low electron mobility in InAs NWs as compared to the bulk.[12,22] We have passivated our devices using $(NH_4)S_x$, but this passivation leads to further enhancement to the surface charge density ($\sim 10^{12}$ cm^{-2}) (Ref. 21) and consequently results in excellent Ohmic contacts. Figure 1(c) shows that our device is always in a conducting state throughout the gate range with a low resistance value, strongly suggesting the presence of the accumulation layer. To estimate the $\kappa_{\rm el}$ we have to consider the thickness of the layer of this SAC since it will reduce the effective cross-sectional area through which heat is transported by electrons. The electrons in the bulk and in the accumulation layer can be thought of as two parallel channels conducting heat, and we can define a effective layer thickness (t) to find out the actual $\kappa_{\rm el}$ from the WF law,

$$\kappa_{\rm el} = \frac{lT_bL_0}{\pi R\{r^2 - (r-t)^2\}} \quad (0 < t \leqslant r), \qquad (2)$$

where l and r are the length and radius of the wire, respectively, R is the electrical resistance at temperature T_b, and $L_0 = 2.45 \times 10^{-8}$ W Ω K^{-2} is the Lorenz number. We can get a rough estimate of t from the above equation by assuming that at the lowest temperature the phonon contribution ($\kappa_{\rm ph}$) is small and $\kappa_{\rm el} \sim \kappa$. For a NW of length 2.6 μm and radius 70 nm we get t from our data as ~ 20 and ~ 10 nm for applied gate voltages of -10 and $+10$ V, respectively. Now we use Eq. (2) to find $\kappa_{\rm el}$ for all T_b, and the result is plotted in Fig. 3(d). This estimated $\kappa_{\rm el}$ from a simplified picture captures the variation we see in our data with V_g. Another confirmation about this non-negligible $\kappa_{\rm el}$ comes from our magnetic field measurement. One way to suppress the electronic contribution is to apply a magnetic field,[32,33] as it will reduce the electronic mean free path for heat transport by deflecting the semiclassical trajectory of electrons. We have made measurements in magnetic fields up to 6 T and see a considerable reduction of the thermal conductivity [see Fig. 3(e)]. The magnetic field can affect phonons via the electron-phonon interaction; the
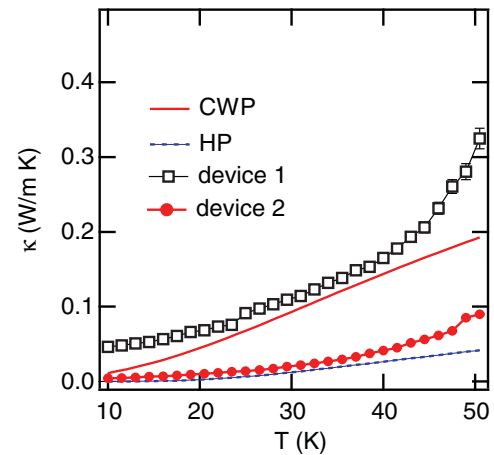

FIG. 4. (Color online) The plot of measured κ as a function of temperature of two different NW samples at 0 V_g, along with the predicted values from two models to understand the reduction in $\kappa_{\rm ph}$ for InAs NWs. Based on the CWP model of Cahill *et al.* (Ref. 30) and the HP model of Hopkins *et al.* (Ref. 41).

amount of change in κ_{ph}, however, is much smaller[34] than the effect we see in our measurement.

The total κ is small and it is important to understand the origin of reduction in κ_{ph}. It is clear from the structural analysis in Fig. 2 that our NWs have a high density of twins. The twin defects introduce additional interfaces and also cause the surface to be rough, with a typical roughness $\sim$2–3 nm. The heat conduction in the bulk is dominated by phonons whose mean free path λ_{mfp} is much larger than the spacing between defect planes throughout the temperature range of our measurements (see Ref. 24, Fig. S17). The average number of defect interfaces is $\sim$500 per μm—this makes the problem challenging to model comprehensively. However, previous experiments on ordered,[35,36] quasiperiodic superlattices,[37] and calculations with modulations of the superlattice[38,39] on a similar length scale $\ll\lambda_{mfp}$ suggest that suppression of κ takes place in such structures. Our devices have aperiodic interfaces [see Fig. 2(a)], and they are likely to attenuate a wide band of phonons. Additionally, modeling indicates that heat transport across grain boundaries can offer significant thermal impedance.[40] In order to understand the magnitude of the observed κ, we use a model by Hopkins *et al.*[41] (denoted as the HP model) which explicitly takes into account the role of interfaces for calculating minimum κ in layered materials. We have calculated the predicted values of the model of Cahill *et al.*[30] (denoted as the CWP model) and the HP model for InAs (see Ref. 24). There is a range of κ measured for devices made from different NW samples (see Ref. 24); data from two such devices at 0 V_g is shown in Fig. 4. Without introducing any free parameters, the predictions of the CWP and HP models result in values that are comparable to the range in κ measured in our experiments.

In summary, we demonstrate that thermal conductivity of InAs NWs with twin defects and polytypes is 1000 times smaller than the bulk values, which will make our devices suitable candidates for good thermoelectric materials. We show that the electronic contribution becomes significant due to the presence of surface charge accumulation. The ability to tune thermal conductivity electrostatically can lead to unique ways of probing heat transport in defect-engineered nanostructures, and possible device applications.

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