# Superconducting films fabricated by high-fluence Ga implantation in Si

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Ga-rich layers in Si were fabricated by 80 keV Ga implantation through a 30 nm $SiO_2$ cover layer and subsequent rapid thermal annealing for 60 s in a temperature range between 500 °C and 1000 °C. Fluences of $2\times10^{16}$ cm$^{-2}$ and $4\times10^{16}$ cm$^{-2}$, leading to Ga peak concentrations of 8 at. % and 16 at. %, are chosen. Residual damage in the implanted layers and the Ga distribution were investigated by Rutherford-backscattering spectrometry in combination with ion channeling, cross-sectional electron microscopy, and x-ray photoelectron spectroscopy. Temperature-dependent Hall-effect measurements were carried out in order to determine the electrical properties of the implanted layers. It is shown that annealing at temperatures up to 800 °C leads to the formation of polycrystalline layers containing random distributed amorphous clusters. At the $Si/SiO_2$ interface a dense and narrow band of Ga-rich clusters is observed. For $4\times10^{16}$ cm$^{-2}$ the amount of mobile Ga is higher than for $2\times10^{16}$ cm$^{-2}$ and an increase of the cluster density at the $Si/SiO_2$ interface was found. Due to the higher cluster density for $4\times10^{16}$ cm$^{-2}$ this interface layer can become superconducting below 7 K with critical fields exceeding 9 T at optimized annealing conditions. Critical currents are above 1 kA/cm$^2$ and therefore this seems to be a possible material system for future microelectronic applications. After annealing at 900 °C and above, the implanted layers are single crystalline and no amorphous precipitates were detected.

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## I. INTRODUCTION

Recently, it has been shown that heavily *p*-doped group-IV semiconductors like diamond, silicon, and germanium can become superconducting at low temperatures.[1–3] To get intrinsic superconducting layers with a relatively high critical temperature, it is a key challenge to generate high charge-carrier densities beyond the metal-insulator transition (MIT) and to prevent dopant precipitation.[4] In most cases the further increase of the carrier concentration is limited by the equilibrium solid solubility of the dopants. However, nonequilibrium doping techniques can help to overcome this threshold. Until now, gas immersion laser doping,[5] high-pressure high-temperature synthesis,[6] and ion implantation with subsequent annealing[3,7] have been successfully applied. Among these doping processes, only the latter one is fully compatible with microelectronic technology. Therefore ion-beam doping has the potential to quickly develop novel silicon or germanium based micro- or nanoelectronic devices reaching from a superconducting quantum interference device (SQUID) to a possible quantum computer.[8]

At present, intrinsic superconducting layers in Ga-doped germanium[7] and boron-doped silicon[9] achieve critical temperatures of 1 and 0.6 K, respectively. For microelectronic applications it is an advantage if the superconducting state is stable at least above liquid-helium temperature but at the moment it is not clear whether this could be reached without dopant clustering. The idea is to fabricate superconducting nanostructures with higher critical temperatures in semiconductors not only via doping but due to dopant precipitation.

The challenge is to find a suitable material system and processing technology to fabricate extrinsic superconducting microstructures. For this the implanted element should have a low solid solubility and favorable superconducting properties. All in all, Ga seems to be an ideal candidate for this task. It has a solid solubility of only 0.1 at. % in Si (Ref. 10) and various superconducting phases[11–13] including the most interesting amorphous state with a critical temperature of 8.5 K.[13] Ga shows a strong tendency to enrich and segregate at Si surfaces[14,15] or at Si-$SiO_2$ interfaces[16] after high-fluence implantation and subsequent annealing, forming in this way thin, Ga-rich films which might become superconducting. Furthermore, Ga is a shallow acceptor in Si with a critical concentration of $1.8\times10^{19}$ cm$^{-3}$ (0.036 at. %) for the metal-insulator transition.[17] Therefore semiconducting, normal-state metallic and superconducting regions in Si can be fabricated by Ga implantation.

In a recent paper[18] we reported about superconducting layers in Ga overdoped Si covered by a thin $SiO_2$ layer. Critical temperatures of 7 K and critical fields exceeding 9 T were found. Now a detailed study of the morphology and composition of the Ga implanted Si layers beneath the $SiO_2$ capping layer is presented and discussed in association with their electrical transport properties. The Ga redistribution and precipitation as well as the recrystallization behavior of the amorphous Si layer during rapid thermal annealing is investigated. The optimum preparation conditions necessary for the formation of superconducting layers in Ga implanted Si are determined.

 

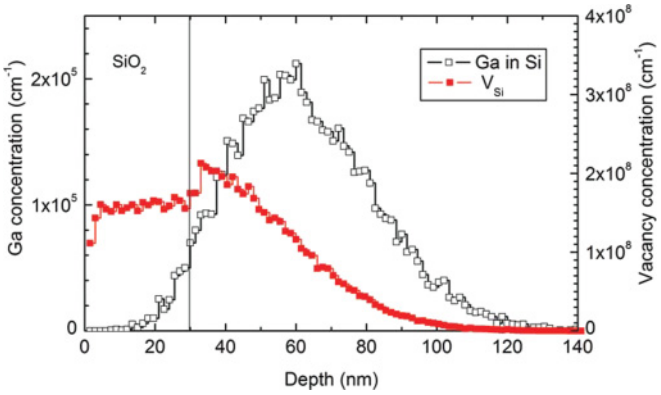


FIG. 1. (Color online) SRIM simulation of the gallium and vacancy distribution in a Si substrate with 30 nm $SiO_2$ cover layer implanted with 80 keV $Ga^+$. Multiplying the values with the fluence gives the volume concentrations.

## II. EXPERIMENT

The sample processing is carried out using 380-$\mu$m-thick Czochralski-grown *n*-type Si wafers with (100) orientation and a resistivity of about 1 k$\Omega$ cm. Before implantation, a 30 nm thick $SiO_2$ layer was deposited on top by sputtering to protect the surface during implantation and to prevent out-diffusion of the implanted Ga while annealing.

$Ga^+$ was implanted with an ion energy of 80 keV and fluences of $2\times10^{16}$ cm$^{-2}$ and $4\times10^{16}$ cm$^{-2}$. According to SRIM[19] simulations shown in Fig. 1, the implantation results in Gaussian-like Ga profiles in the Si substrate with peak concentrations of $4\times10^{21}$ cm$^{-3}$ (8 at. %) and $8\times10^{21}$ cm$^{-3}$ (16 at. %), respectively, located around 30 nm below the $Si/SiO_2$ interface. During implantation at room temperature, the beam current does not exceed 0.5 $\mu$A cm$^{-2}$ to prevent significant heating of the wafer. The critical energy density for amorphization of Si at room temperature is about $2\times10^{24}$ eV/cm$^3$, which corresponds to a damage of about $5\times10^{22}$ vacancies/cm$^3$ (one displacement per atom).[20] Therefore formation of amorphous layers with thicknesses of about 80 or 90 nm for the used two Ga fluences, respectively, are predicted by the SRIM simulation.

After the implantation step, wafers are cut into samples of $1 \times 1$ cm$^2$. To initiate recrystallization of the amorphous Si layers and precipitation of the implanted Ga, the samples were processed by rapid thermal annealing (RTA) for 60 s in flowing argon atmosphere at temperatures between 500 and 1000 °C.[21]

Rutherford-backscattering spectrometry in channeling geometry (RBS/C) as well as in random direction with a 1.2-MeV $He^+$ beam is used to determine the structure of the implanted silicon layer and the redistribution of Ga during annealing. For higher depth resolution, the angle between incident beam and detector is 70°. This leads to a quite high depth resolution of about 10 nm. A drawback of this glancing angle geometry is the fact that the element peaks in the spectrum are closer together. The further decrease of the ion energy or increase of the angle would lead to an overlap of the Ga, Si, and O peak. So the parameters chosen here lead to the best depth resolution where all peaks are well separated.

The chemical modification of Ga at the $Si/SiO_2$ interface is investigated by x-ray photoelectron spectroscopy (XPS). The measurements are done using a PHI 5600 CI (Physical Electronics) spectrometer equipped with a hemispherical electron analyzer using nonmonochromatized x-rays (Mg-$K\alpha$, 350 W) for excitation. Charging effects are minimized using a low energetic electron flood gun. To minimize chemical changes by ion mixing during ion sputtering, heavy $Xe^+$ ions at low energy (1.5 keV) are used.[22] To examine cluster distribution and size, high-resolution cross-section TEM analyses with an image-corrected FEI Titan 80-300 are performed.

For the electrical measurements, ohmic contacts are formed by sputtering of gold onto the corners of the samples and mounting silver wires with silver glue on top. A LakeShore HMS 9709 Hall measurement system is used. It allows for sheet-resistance and Hall-effect measurements in Van der Pauw geometry in a temperature range between 2 and 400 K. Excitation current and magnetic field are chosen to be 1 mA and 1 T (up to 9 T are possible), respectively.

## III. RESULTS AND DISCUSSION

### A. Microstructural characterization

#### *1. Damage, polycrystallization and segregation*

The RBS/C investigations of the as-implanted samples show in the Si part of the spectra damage peaks [Figs. 2(a) and 3(a)] touching the random level. This reveals complete layer amorphization of a certain surface region, whereas the amorphous layer widths are found in good agreement with the SRIM predictions to be 80 nm [Fig. 2(a)] and 100 nm [Fig. 3(a)] for $2\times10^{16}$ cm$^{-2}$ and $4\times10^{16}$ cm$^{-2}$, respectively. The high yield in the aligned spectra between channels 350 and 380 indicates an enhanced dechannelling of He ions in a damaged region located between the amorphous layer and crystalline substrate. After annealing at temperatures up to 800 °C, the amorphous Si peak in the RBS spectra shows only few differences [see Figs. 2(a) and 3(a)], the signal in the highly damaged region behind the amorphous layer decreases. Although after annealing the signal in the aligned spectra is as high as the random level, one has to keep in mind that amorphous Si layers should not be stable at these annealing temperatures. One can expect that these layers are crystallized during annealing.[14] Obviously, ion channeling is completely blocked due to the polycrystalline structure of the layer with randomly oriented grains. It is well known that silicon layers implanted with high Ga fluences ($>1\times10^{16}$ cm$^{-2}$) become polycrystalline after thermal treatment at around 500 °C (Refs. 14 and 15). A model that is also discussed for In-implanted Si can explain this behavior:[23] Due to the statistical character of the implantation doping, Ga-rich regions arise. According to the phase diagram, these Ga-rich areas have a significantly lower melting temperature than pure Si. As a result, epitaxial crystallization of the amorphous layer is prevented by these liquid regions and polycrystallization takes place. Furthermore, besides melting it is possible that polycrystallization takes place in the amorphous layer due to enhanced solid-phase nucleation in Ga-rich regions.

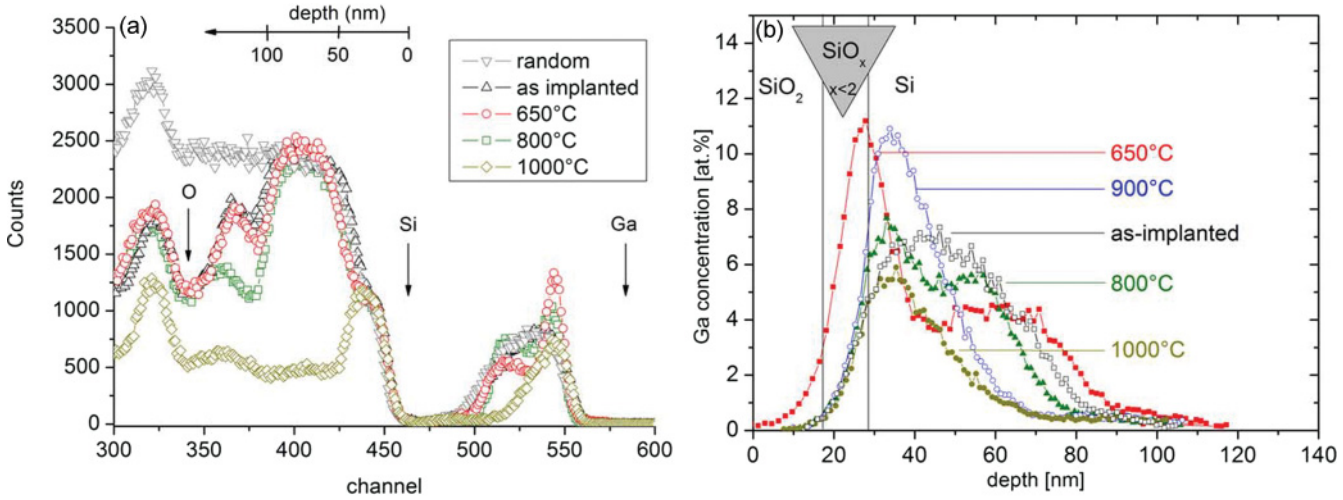


FIG. 2. (Color online) Results of the RBS/C analyses of samples implanted with a Ga fluence of $2\times10^{16}$ cm$^{-2}$. (a) RBS/C spectra with depth scale for the implanted Si layer. After implantation, the layer is amorphous and gets polycrystalline during annealing at temperatures up to 800 °C. RTA with at least 900 °C leads to SPE growth of the layer. (b) Ga depth distribution calculated with RUMP[24] whereas for the profile calculation, the random spectra (not shown) are used. The ion-beam mixing during implantation results in a $SiO_x$ transition region.

Up to an annealing temperature of 750 °C, a strong segregation of Ga atoms is observed [see Figs. 2(a) and 3(a)] around channel 550. This behavior seems to be independent of the implanted Ga fluence and only the amplitude of the signal is different. It cannot be excluded that the real Ga distribution is narrower, and has a higher peak concentration than indicated by RBS because of the limited depth resolution. Consequently, the calculations of the Ga profiles with the analysis software RUMP,[24] shown in Figs. 2(b) and 3(b), give only a lower limit of the corresponding Ga concentration. The calculated maximum concentration amounts to 11 at. % ($2\times10^{16}$ cm$^{-2}$) and 18 at. % ($4\times10^{16}$ cm$^{-2}$). The simulations also indicate that it is difficult to define a clear position of the Si/$SiO_2$ interface and that the highest Ga concentrations are located in a $SiO_x$ ($x < 2$) environment. After the polycrystallization, and nearly independent of the implanted fluence, a Ga concentration of 5–7 at. % is found deeper in the implanted layer [Figs. 2(b) and 3(b)]. This leads to the assumption that during polycrystallization a certain amount of Ga is solved in the grains and the rest is located at grain boundaries. It can be supposed that fast diffusion of Ga along the grain boundaries causes the peak at the Si/$SiO_2$ interface. Consequently, after polycrystallization in the layers implanted with $4\times10^{16}$ cm$^{-2}$, more Ga is located at the grain boundaries and can diffuse to the Si/$SiO_2$ interface, leading to a higher Ga peak.

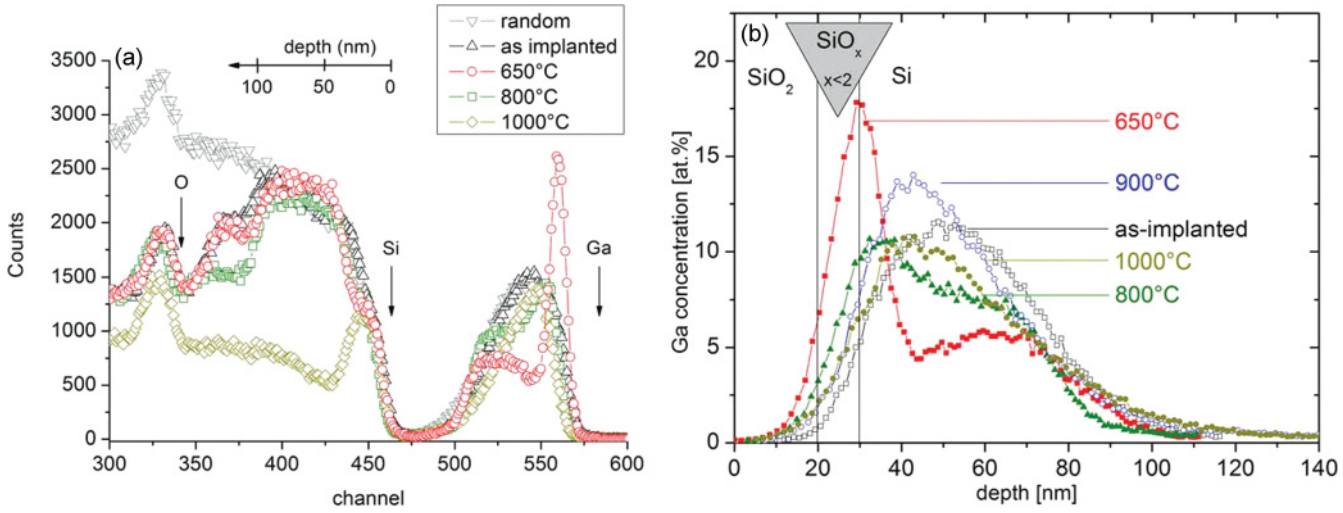


FIG. 3. (Color online) Results of the RBS/C analyses of samples implanted with a Ga fluence of $4\times10^{16}$ cm$^{-2}$. (a) RBS/C spectra with depth scale for the implanted Si layer. After implantation, the layer is amorphous and becomes polycrystalline during annealing at temperatures up to 800 °C. RTA with at least 900 °C leads to SPE growth of the layer. (b) Ga depth distribution calculated with RUMP[20] whereas for the profile calculation, the random spectra (not shown) are used. The ion-beam mixing during implantation results in a $SiO_x$ transition region.

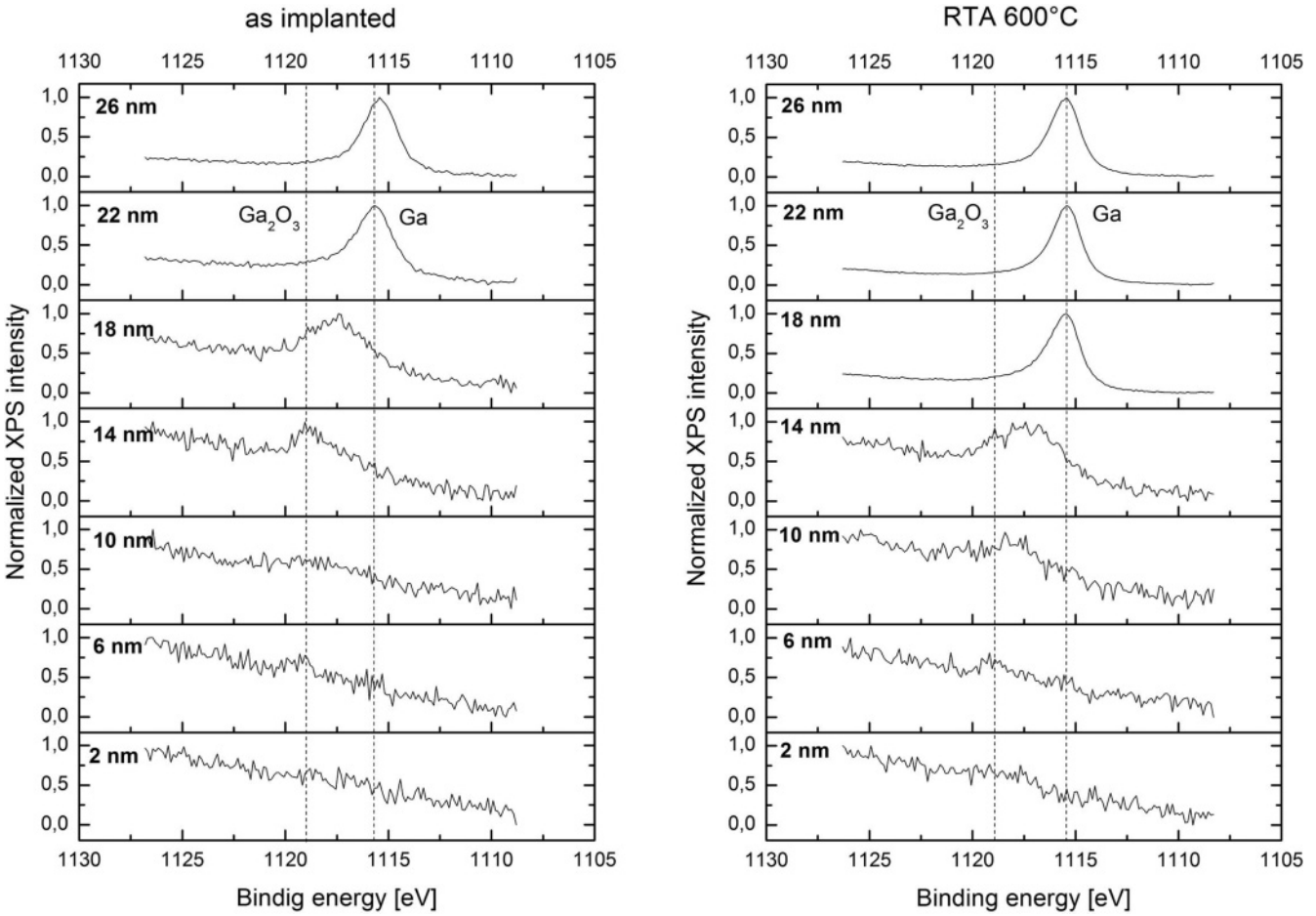


FIG. 4. The results of XPS analyses of an as-implanted and a superconducting sample annealed at 600 °C. For both samples the Ga peak is shifted due to Ga oxidation in the transition region between the $SiO_2$ and Si.

### *2. Ga oxidation and cluster composition*

It is known from literature that bombardment of Ga implanted Si with low-energy oxygen ions during secondary ion mass spectroscopy (SIMS) or reactive ion etching (RIE) can lead to Ga segregation in the near surface region due to the oxidation of Ga.[25,26] As reported by Yokota *et al.*,[16] Ga accumulates in a thin native-oxide film (2.5 nm) on top of Ga-implanted silicon during annealing up to 700 °C. At higher temperatures, Ga is lost by evaporation. During high-fluence ion implantation, as reported in the present paper, a strong ion-beam mixing at the $Si/SiO_2$ interface takes place and therefore Ga could be oxidized.

The depth-dependent XPS measurements shown in Fig. 4 confirm that Ga is oxidized at the $Si/SiO_2$ interface. At the bottom of the picture the spectra measured for the $SiO_2$ surface is shown. For depth profiling $Xe^+$ sputtering is used to erode the $SiO_2$ cover layer. The presented spectra are measured in depth steps of 4 nm and show the transition from the $SiO_2$ cover layer to the Si substrate. For pure Ga, the 2*p* peak is located at a binding energy of 1116 eV. The peak shift to higher energies observed in the interface region indicates Ga oxidation. The binding energy of the most stable oxide ($Ga_2O_3$) amounts to 1119 eV. As found in XPS measurements, O is also present in the implanted Si layer but no measurable amount of Ga is oxidized in this region. It should be noted that Ga oxidation occurs already during implantation as revealed by the XPS spectra of the as-implanted sample. There is no hint that the oxidized Ga concentration increases after annealing. As a consequence, the oxidized Ga is fixed at the interface and cannot diffuse through $SiO_2$ during annealing at temperatures below 900 °C.

In order to study details of the layer microstructure and composition, cross-section transmission electron microscopy (XTEM) investigations in combination with energy dispersive x-ray spectroscopy (EDX) were performed. The amorphous layer formed after implantation appears to be completely homogeneous. There is no indication of any crystalline inclusions in the amorphous layer. After annealing at 650 °C (Fig. 5), the implanted layer is mainly polycrystalline but contains randomly distributed amorphous precipitates. An EDX analysis (two examples are shown in Fig. 6) reveals differences in the composition of precipitates. Precipitates located at the interface contain up to 21 at. % Ga as well as 15 at. % O and 64 at. % Si. Therefore the oxidized Ga detected by XPS should not correspond to these clusters and is located within the $SiO_2$. These Ga-rich precipitates form a dense and narrow band (10 nm) at the $Si/SiO_2$ interface. Some precipitates can also be identified in deeper regions.

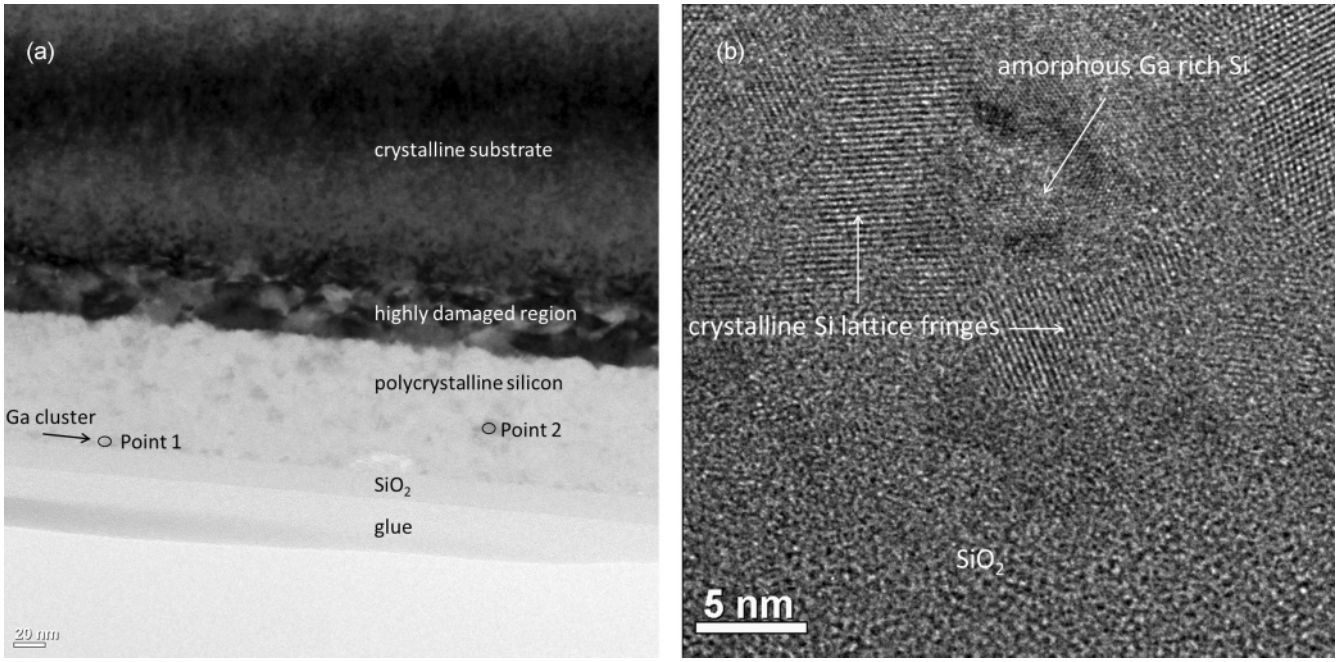


FIG. 5. (a) XTEM micrograph of the samples revealing the layered structure after ion implantation and subsequent annealing at 650 °C. The polycrystalline Si layer contains random distributed amorphous precipitates. (b) Detail of the Si/$SiO_2$ interface showing Si polycrystals interrupted by amorphous Ga-rich clusters.

They contain about 94 at. % Si, 3 at. % O, and only 3 at. % Ga. It was not possible to detect a closed cluster network by cross section or plane-view TEM. Especially with plane-view TEM it is difficult to look through the $SiO_2$ cover layer.

### 3. *Solid-phase epitaxial growth*

After annealing at 900 °C and above, the aligned RBS signal in the former amorphous layer (channel region ≈380-420) reduces significantly, indicating that the layers are single crystalline. As examples, in Figs. 2 and 3 the corresponding spectra obtained for the samples prepared with different Ga fluences and annealed at 1000 °C are presented. This behavior can be explained by the time lag needed for nucleation and melting in Ga-rich regions where polycrystallization starts. If solid-phase epitaxial growth (SPE) occurs before melting or nucleation takes place, the resulting layers become single crystalline. The time required for SPE regrowth of the heavily Ga-doped Si layer is less than that of virgin silicon,[27] which in turn is about 0.03 s at 900 °C. This means that Ga redistribution after SPE growth during annealing for 60 s is restricted to Ga diffusion in single-crystalline material. The total diffusion length of Ga in single-crystalline Si at 900 °C can be calculated with the corresponding diffusion coefficient[28] to be only about 3 nm.

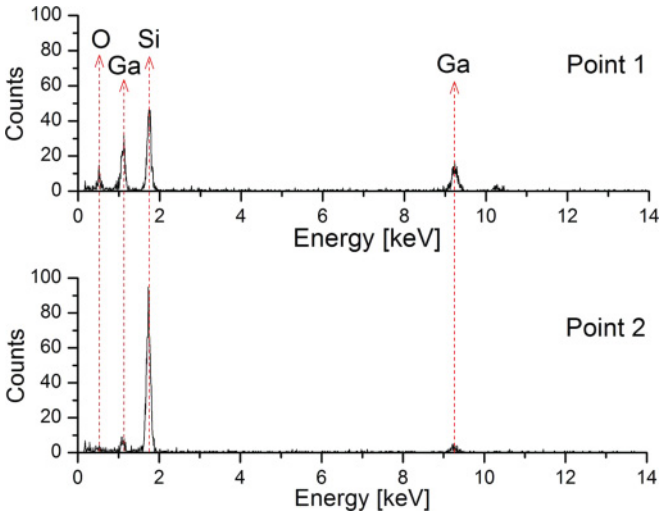


FIG. 6. (Color online) EDX spectra of two amorphous clusters marked in Fig. 5(a). The cluster at the Si/$SiO_2$ interface (point 1) contains 21 at. % Ga, 15 at. % O, and 64 at. % Si. In contrast to that, the cluster deeper in the layer (point 2) contains only 3 at. % Ga, 3 at. % O, but 94 at. % Si.

The redistribution of the implanted Ga profile observed for the samples implanted with $2\times10^{16}$ $cm^{-2}$ and annealed with 900–1000 °C [Fig. 2(b)] can be explained by the so-called snow-plow effect that is described by an effective segregation coefficient.[29] The snow-plow effect takes place if the solid solubility of the implanted element in the amorphous phase ($c_{amorph}$) is higher than in the crystalline ($c_{cryst}$) one and the diffusion velocity ($v_{Ga}$) of Ga is higher than the velocity of the SPE ($v_{SPE}$) front.[29] About 45% of implanted Ga is lost after annealing at 1000 °C. For the higher Ga fluence, the snow-plow effect does not occur and the Ga profile after annealing is nearly equal to the as-implanted one [Fig. 3(b)]. Obviously, the SPE front moves faster than Ga can diffuse in this case. The enhanced SPE growth rate can be explained due to the fact that higher dopant concentrations generate more electrically charged defects at the crystalline-amorphous interface.[30] In this case, 28% of implanted Ga is lost after annealing at 1000 °C due to out-diffusion. As a summary, the relations of

TABLE I. The snow-plow effect occurs if the quotient of the solid solubility of the dopant in single-crystalline ($c_{cryst}$) and amorphous ($c_{amorph}$) state is below 1. Furthermore, the diffusion velocity of the dopant in the amorphous phase ($v_{Ga}$) has to be higher than the solid-phase epitaxial regrowth velocity ($v_{SPE}$). This is the case for the samples implanted with $2\times10^{16}$ cm$^{-2}$ Ga. As high dopant concentrations enhance SPE regrowth the snow-plow effect does not occur in the samples implanted with $4\times10^{16}$ cm$^{-2}$.

| Fluence | $2\times10^{16}$ cm$^{-2}$ | $4\times10^{16}$ cm$^{-2}$ |
|---|---|---|
| Solubility ratio | $\frac{c_{cryst}}{c_{amorph}} < 1$ | $\frac{c_{cryst}}{c_{amorph}} < 1$ |
| Velocity ratio | $\frac{v_{SPE}}{v_{Ga}} < 1$ | $\frac{v_{SPE}}{v_{Ga}} > 1$ |

the solubilities and velocities for the two implanted fluences is presented in Table I.

### B. Electrical characterization

#### 1. *Sheet resistance and Ga activation*

In Fig. 7(a) the sheet resistances of samples implanted with lower Ga fluence ($2\times10^{16}$ cm$^{-2}$) and subsequently annealed at temperatures from 550 to 900 °C are shown as a function of measurement temperature. Obviously, annealing at 550 °C is not adequate for Ga-acceptor activation above the critical concentration of $1.8\times10^{19}$ cm$^{-3}$ for the metal-insulator transition.[17] As expected for a doped semiconductor, the resistance increases with decreasing temperature. All samples annealed with at least 600 °C show an almost temperature-independent sheet resistance [Fig. 7(a)], which indicates metallic conductivity. Leakage currents into the semiconducting substrate contribute to the sheet resistances

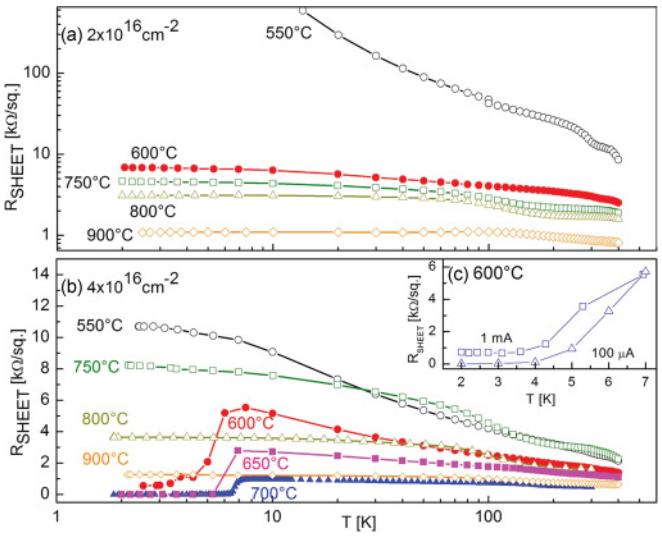


FIG. 7. (Color online) The sheet resistances of Si samples implanted with a Ga fluence of (a) $2\times10^{16}$ cm$^{-2}$ and (b) $4\times10^{16}$ cm$^{-2}$ after RTA as a function of temperature. Leakage currents into the substrate influence the sheet resistance at higher temperatures. The actual sheet resistance of the Ga-doped layers is given by the low-temperature values. In the inset (c) the excitation current dependence of the residual resistance for the sample annealed at 600 °C is shown.

measured at higher temperatures. Below 50 K, charge carriers in the silicon substrate freeze out and the actual sheet resistance of the heavily Ga-doped layer is measured. The sample annealed at 550 °C has a sheet resistance of $6\times10^5$ Ω/sq (at 20 K). After annealing at 600 °C, the sheet resistance drops down to 6 kΩ/sq (at 10 K) and decreases further to 1 kΩ/sq (at 10 K) with increasing annealing temperature to 900 °C.

The sheet resistance of the samples implanted with a fluence of $4\times10^{16}$ cm$^{-2}$ first strongly decreases with increasing annealing temperature down to 1 kΩ/sq (700 °C) but jumps up to 7.5 kΩ/sq at 750 °C [Fig. 7(b)]. This nonmonotonic behavior saturates at a value that is similar to the one obtained for the sample implanted with $2\times10^{16}$ cm$^{-2}$. Even a further increase of the annealing temperature cannot reduce the sheet resistance below those obtained for the samples implanted with the lower fluence. As the RBS spectra show, the samples annealed up to 750 °C contain a Ga-rich layer at the Si/SiO$_2$ interface. It can be supposed that this interface layer dominates the electrical transport in the samples implanted with $4\times10^{16}$ cm$^{-2}$ Ga and is responsible for the superconducting transition observed at a critical temperature of about 7 K.

In order to investigate the electrically active Ga concentration in dependence of the annealing temperature, Hall-effect measurements were performed. For annealing temperatures below 750 °C, the Hall voltage is very noisy and therefore could not be analyzed. But also for the samples annealed at higher temperatures a reliable interpretation of the Hall effect is difficult. The implanted layers are prepared on a conductive substrate and leakage currents could strongly influence the results above 50 K as shown in Fig. 8. Furthermore, the layers contain Ga-rich clusters and it is not clear how they influence the electrical parameters. Therefore one has to be cautious with the correlation between the Hall coefficient $R_H$ and the carrier concentration. The Hall sheet concentration is calculated from the sheet Hall coefficient $R_H$ and the elementary charge $q$ as $1/(qR_H)$. In all samples a

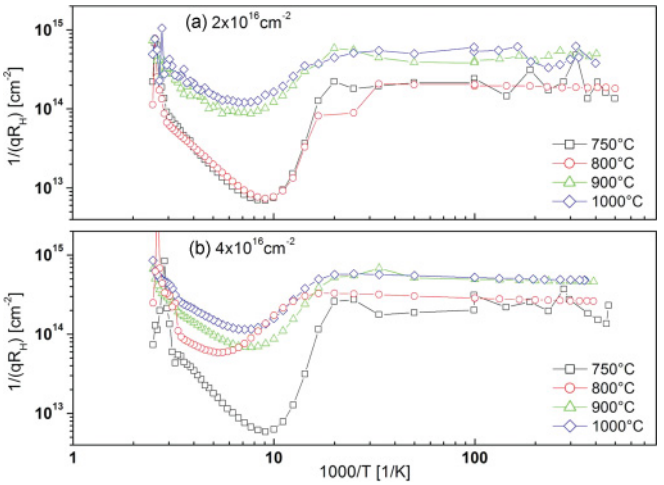


FIG. 8. (Color online) Hall sheet concentration as a function of the inverse temperature for samples annealed between 750 and 1000 °C. There are no significant differences between the samples implanted with (a) $2\times10^{16}$ cm$^{-2}$ and (b) $4\times10^{16}$ cm$^{-2}$ Ga. The samples annealed at 750 and 800 °C are polycrystalline. Annealing with 900 and 1000 °C leads to single-crystalline layers.

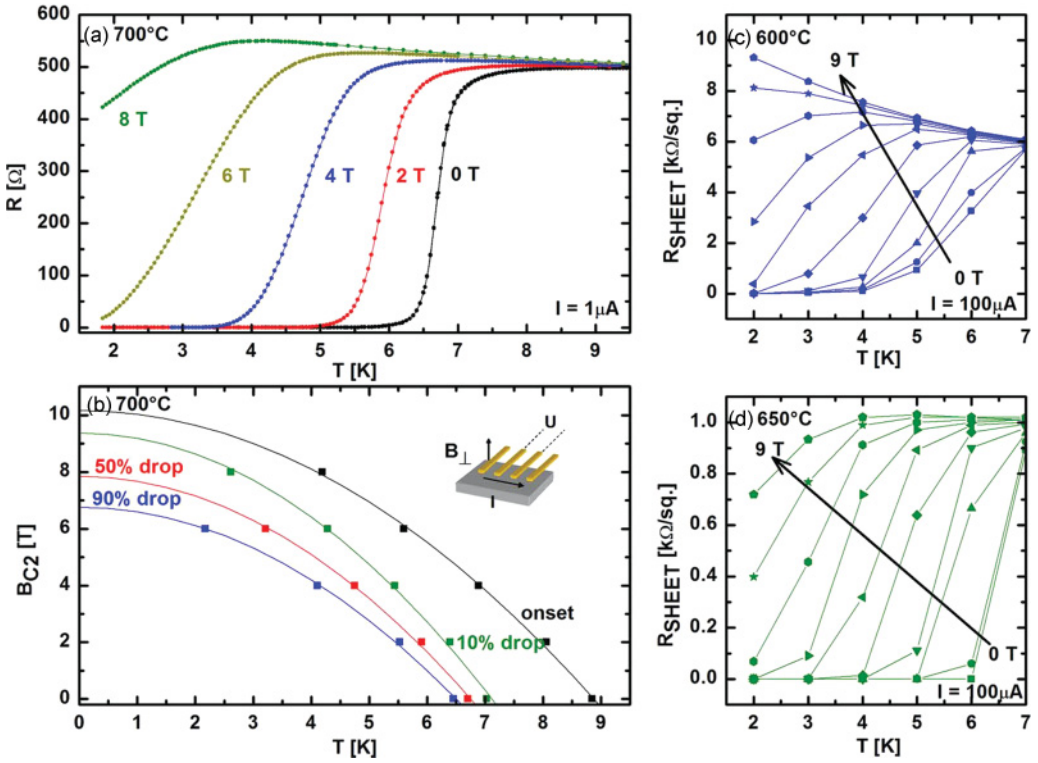


FIG. 9. (Color online) (a) Superconducting transition of the sheet resistance at various magnetic fields applied perpendicular to the surface for the sample annealed at 700 °C. (b) Critical magnetic fields perpendicular to the sample surface at different temperatures for the sample shown in (a). The lines are BCS-like parabolic fits and show a clear broadening of the transition region with increasing magnetic field. (c) Scan of the superconducting transition for the sample annealed at 600 °C. The excitation current is chosen to be 100 $\mu$A and the field is increased in steps of 1 T. (d) Measurement equal to (c) for the sample annealed at 650 °C.

positive Hall coefficient was measured which indicates *p*-type conductivity. The low-temperature Hall sheet concentrations are temperature independent, as expected for metallic conduction. Interestingly, the values obtained for the two Ga fluences are very similar and depend only on the annealing temperature. The low-temperature Hall sheet concentrations are in the range between $1.5\times10^{14}$ and $5\times10^{14}$ cm$^{-2}$ and correspond to mean hole concentrations between $1.5\times10^{19}$ and $5\times10^{19}$ cm$^{-3}$, respectively, if a 100-nm-thick homogenous, conductive layer is assumed. This is well above the threshold concentration for the MIT and in the range of the solid solubility limit (0.1 at. %) for Ga in Si but much less than the Ga concentration in the layer measured by RBS. Obviously, most of the Ga atoms do not act as acceptors. When comparing the Hall concentrations with the implanted Ga fluences the apparent activation is below 1.3%.

### 2. *Superconducting state*

All samples implanted with $4\times10^{16}$ cm$^{-2}$ Ga and annealed between 600 and 700 °C show a low sheet resistance and become superconducting at temperatures below (7.02 ± 0.01) K (using a 90% residual-resistance criterion), as mentioned above. A variation of the sheet resistance from 5 kΩ/sq (600 °C) to 1 kΩ/sq (700 °C) does not perceptibly influence $T_c$. The low-temperature sheet resistance measured at various magnetic fields applied perpendicular to the surface of the samples annealed at 600–700 °C is shown in Fig. 9. In comparison to the superconducting samples annealed at higher temperatures, annealing at 600 °C leads to a width of transition that is much broader [Fig. 9(c)]. For this sample, the residual resistance in the superconducting state also depends on the excitation current and changes from 0.7 Ω/sq (100 $\mu$A) to 716 Ω/sq (1 mA) as can be seen from [Fig. 7(c)]. In addition, the samples annealed at 650 and 700 °C exhibit a very sharp transition in current-voltage characteristics with critical currents of around 2 mA at 2 K. The temperature-dependent critical magnetic fields perpendicular to the surface of the sample annealed at 700 °C are summarized in Fig. 9(b). Especially the out-of-plane critical fields follow a typical parabolic behavior.[31] A parabolic fit estimates a maximum critical field perpendicular to the layer of $B_{c2,\mathrm{per}}$ $(T = 0) \approx 9.4$ T. This allows for a derivation of the Ginzburg-Landau coherence length $\xi_{\mathrm{GL}}$ ~6 nm via $B_{c2,\mathrm{per}} = \Phi_0 / 2\pi\ {\xi_{\mathrm{GL}}}^2$. Thus with $B_{c2,\mathrm{par}}$ $(T = 0)$ ≈14 T the approximation of a superconducting layer thickness $d = (6^{0.5}\Phi_0)\ /(\pi\ \xi_{\mathrm{GL}}B_{c2,\mathrm{par}}) \sim 20$ nm can be done and $6^{0.5}$ is a correction factor for thin-plate geometry.[32] This result is reasonable if we assume the Ga precipitates to be the origin of superconductivity. For an estimation of the London penetration depth, ${\lambda_{\mathrm{L}}}^2 = m/\mu_0 n_S e^2$, the superconducting carrier density, $n_s = (j_c 3\pi 3^{0.5}\xi_{\mathrm{GL}}m)/(eh)$, has to be calculated first. For simplification, $m$ as the bare and not the effective mass is used. As given above, the critical current is about 2 mA and the superconducting layer has a width of $d \sim 20$ nm. That

ends up with $j_c \sim 1$ kA/cm$^2$ and $n_s \sim 8.4\times10^{15}$ cm$^{-3}$, which leads to $\lambda_L \sim 58$ $\mu$m. The strong type-II superconductivity of the layers is indicated by a Ginzburg-Landau parameter $\kappa_{GL} = \lambda_L / \xi_{GL} \sim 10^4$. The high in-plane critical fields originate from the fact that the layer thickness $d$ is much smaller than $\lambda_L$ and thus the field needs much less expulsion enthalpy in parallel geometry. That is why the in-plane critical fields are even equal to the simplest approximation of the Pauli limit[33] $B_{Pauli} = 1.84\ T_c\ [T/K] \approx 12.9$ T.

### 3. *Localization of the superconducting layer*

The superconducting region is expected to be located at the Ga-rich Si/SiO$_2$ interface layer, because of the thin film and type-II character of superconductivity. To prove that superconductivity can indeed be attributed to Ga precipitates, surface etching and subsequent resistivity as well as RBS measurements have been performed for the superconducting sample annealed at 650 °C. The latter reveal that the Ga-rich layer has been successfully removed. In Fig. 10, the Ga distribution before and after etching the SiO$_2$ cover layer is shown. For better comparison, the calculated profile before etching has been shifted by the SiO$_2$ thickness. After SiO$_2$ etching, the RBS spectra indicate no Ga-rich layer anymore. The Ga distribution at greater depths has not changed after etching and still confirms a peak concentration of 7 at. %. Furthermore, after etching, the sheet resistance thus increases (Fig. 10) from 960 Ω/sq to 16.3 kΩ/sq (values at a temperature of 10 K) and no superconductivity is observed anymore. In a parallel conduction model, the Ga-rich interface layer has a resistance of 1020 Ω/sq and it dominates the electrical properties of the samples. It is possible to use the same model for the sheet Hall coefficient.[34] Before etching it is 960 cm$^2$/C and changes to 14 862 cm$^2$/C. In this simple model the interface layer has a sheet Hall coefficient of 1025 cm$^2$/C. This corresponds to a carrier sheet concentration of

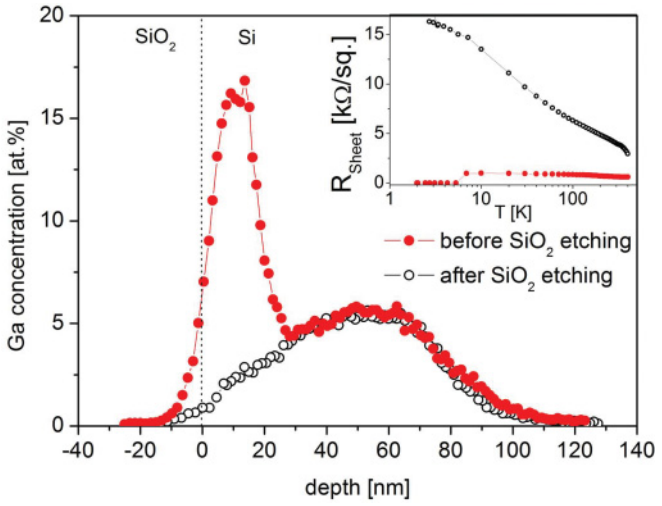


FIG. 10. (Color online) Depth distribution of Ga before and after etching of the SiO$_2$ cover layer, as calculated from the RBS random spectra. Depth zero corresponds to the surface of the Si substrate. For better comparison the profile before etching has been shifted by the value of the SiO$_2$ thickness. The inset shows the temperature-dependent sheet resistance of the sample before and after etching.

$6\times10^{15}$ cm$^{-2}$, supposing that the layer is laterally homogeneous and the electrical transport is mediated by one carrier type. Since the Hall coefficient is positive the charge carriers are holes. But if the low sheet resistance and superconductivity is explained by a pure Ga layer, the charge carriers should be electrons.[35]

The appearance of the observed superconductivity due to the high Ga concentration at the Si/SiO$_2$ interface is supported by the investigations of Jaeger *et al.*[36] They found that Ga films become superconducting only, if their normal-state low-temperature sheet resistance is below 6 kΩ/sq. A possible explanation of this threshold is also given by Jaeger *et al.*[37] The normal conducting sheet resistance of thin Ga films differs strongly with the substrates on which they are deposited, that means on the chemical environment. Nevertheless, it seems that the superconducting transition is independent of the film thickness on different substrates and only the normal conducting sheet resistance is the important parameter.[38] For the superconducting samples under investigation containing a Ga-rich interface layer, this scattering-induced threshold fits well to our observations [Fig. 7(b)]. It has to be taken into account that superconductivity with comparable critical magnetic fields is also observed for Ga clusters in porous glasses (pore size 4–7 nm).[11] It has been shown that in granular superconductors the grains can couple by weak Josephson junctions.[39] As already shown by Hagel *et al.*[40] the superconducting transition behavior of crystalline cluster compounds containing Ga clusters depend on normal conductive properties. The investigations of Hagel demonstrate that the superconducting properties get weaker if the normal-state resistance increases even if the transition temperature remains the same. As mentioned above, for the samples under investigation the Ga-rich interface layer influences the normal conductive properties. With increasing annealing temperature the sheet resistance decreases. The sample annealed at 600 °C has the highest sheet resistance and the lowest superconducting critical fields and current. It seems that in this sample the superconducting clusters are more weakly coupled than in the other ones. There could be two reasons for this. Either the Ga-rich clusters are smaller or the cluster density in the layer is lower. In both cases the average distance between them should be higher, which results in a weaker coupling.

Nevertheless, these clusters are responsible for the superconductivity. In contrast to the intrinsic superconductivity observed in Ga-doped Ge,[3] the critical temperature only slightly differs from that of bulk Ga phases. Only parameters like critical current or critical magnetic fields depend on the annealing temperature, as expected for extrinsic cluster compound superconductivity.[11,40,41]

## IV. CONCLUSION

Ga-rich layers are fabricated by heavy-ion implantation through a SiO$_2$ capping layer in standard microelectronics Si wafers. The high Ga fluences of $2\times10^{16}$ and $4\times10^{16}$ cm$^{-2}$ cause amorphization of the implanted Si layer. To initiate Ga redistribution and crystallization, 60-s RTA in flowing Ar and temperatures between 500 and 1000 °C are used.

The Ga located at the $Si/SiO_2$ interface is oxidized even after implantation. For both implantation fluences, annealing at temperatures below 900 °C leads to polycrystalline layers containing precipitates. The high density of precipitates at the $Si/SiO_2$ interface contains more Ga (21 at. %) than the precipitates deeper in the layer (3 at. %) because of the fast diffusion of Ga along the grain boundaries. After annealing at 600–700 °C, the Ga-rich interface layer dominates the transport properties of the samples implanted with $4\times10^{16}$ $cm^{-2}$. That causes a relatively low normal-state sheet resistance (1 kΩ/sq at 700 °C) and superconductivity with a critical temperature of 7 K. Out-of-plane critical fields of 9.4 T are achieved. Even if the superconducting properties fit well to values obtained for thin Ga films and Ga clusters, one has to keep in mind that the precipitates observed here contain a high amount of Si (64 at. %) and O (15 at. %).

At annealing temperatures $\geqslant$ 900 °C, solid phase epitaxial growth of the implanted layer without Ga precipitation occurs. For samples implanted with a Ga fluence of $2\times10^{16}$ $cm^{-2}$, the snow-plow effect takes place and a significant Ga redistribution is observed. Samples implanted with $4\times10^{16}$ $cm^{-2}$ show much less Ga redistribution. In both cases the electrical active Ga concentration is only in the range of $5\times10^{19}$ $cm^{-3}$, which is much less than the implanted peak concentrations but in the range of the equilibrium solid solubility of Ga in Si.

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